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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	54770
Number of Logic Elements/Cells	150000
Total RAM Bits	10907648
Number of I/O	284
Number of Gates	-
Voltage - Supply	0.9V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 100°C (TJ)
Package / Case	780-BBGA, FCBGA
Supplier Device Package	780-FBGA, FC (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/intel/10cx150yf780e5g

Table 2. Maximum Allowed Overshoot During Transitions for Intel Cyclone 10 GX Devices

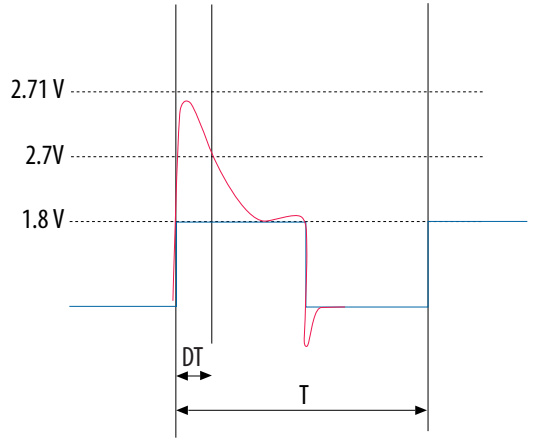
This table lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage of device lifetime. The LVDS I/O values are applicable to the VREFP_ADC and VREFN_ADC I/O pins.

Symbol	Description	Condition (V)		Overshoot Duration as % at T_J = 100°C	Unit
		LVDS I/O (7)	3 V I/O		
V_i (AC)	AC input voltage	2.50	3.80	100	%
		2.55	3.85	42	%
		2.60	3.90	18	%
		2.65	3.95	9	%
		2.70	4.00	4	%
		> 2.70	> 4.00	No overshoot allowed	%

For an overshoot of 2.5 V, the percentage of high time for the overshoot can be as high as 100% over a 10-year period. Percentage of high time is calculated as ([delta T]/T) × 100. This 10-year period assumes that the device is always turned on with 100% I/O toggle rate and 50% duty cycle signal.

(7) The LVDS I/O values are applicable to all dedicated and dual-function configuration I/Os.

Figure 1. Intel Cyclone 10 GX Devices Overshoot Duration



Recommended Operating Conditions

This section lists the functional operation limits for the AC and DC parameters for Intel Cyclone 10 GX devices.

Recommended Operating Conditions

Table 3. Recommended Operating Conditions for Intel Cyclone 10 GX Devices

This table lists the steady-state voltage values expected from Intel Cyclone 10 GX devices. Power supply ramps must all be strictly monotonic, without plateaus.

Symbol	Description	Condition	Minimum (8)	Typical	Maximum (8)	Unit
V_{CC}	Core voltage power supply	—	0.87	0.9	0.93	V
V_{CCP}	Periphery circuitry and transceiver fabric interface power supply	—	0.87	0.9	0.93	V
V_{CCPGM}	Configuration pins power supply	1.8 V	1.71	1.8	1.89	V
		1.5 V	1.425	1.5	1.575	V

continued...

(8) This value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

Symbol	Description	Condition	Minimum (8)	Typical	Maximum (8)	Unit
V_I (11)(12)	DC input voltage	3 V I/O	–0.3	—	3.3	V
		LVDS I/O	–0.3	—	2.19	V
V_O	Output voltage	—	0	—	V_{CCIO}	V
T_J	Operating junction temperature	Extended	0	—	100	°C
		Industrial	–40	—	100	°C
t_{RAMP} (13)	Power supply ramp time	Standard POR	200 µs	—	100 ms	—
		Fast POR	200 µs	—	4 ms	—

Related Information

I/O Standard Specifications on page 15

Transceiver Power Supply Operating Conditions

Table 4. Transceiver Power Supply Operating Conditions for Intel Cyclone 10 GX Devices

Symbol	Description	Condition	Minimum (14)	Typical	Maximum (14)	Unit
$V_{CCT\_GXB[L1][C,D]}$	Transmitter power supply	Chip-to-chip ≤ 12.5 Gbps Or	1.0	1.03	1.06	V

continued...

(8) This value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

(11) The LVDS I/O values are applicable to all dedicated and dual-function configuration I/Os.

(12) This value applies to both input and tri-stated output configuration. Pin voltage should not be externally pulled higher than the maximum value.

(13) t_{ramp} is the ramp time of each individual power supply, not the ramp time of all combined power supplies.

(14) This value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

Parameter	Symbol	Condition	V_{CCIO} (V)										Unit
			1.2		1.5		1.8		2.5		3.0		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Bus-hold, low, overdrive current	I_{ODL}	0 V < V_{IN} < V_{CCIO}	—	125	—	175	—	200	—	300	—	500	µA
Bus-hold, high, overdrive current	I_{ODH}	0 V < V_{IN} < V_{CCIO}	—	–125	—	–175	—	–200	—	–300	—	–500	µA
Bus-hold trip point	V_{TRIP}	—	0.3	0.9	0.38	1.13	0.68	1.07	0.70	1.7	0.8	2	V

OCT Calibration Accuracy Specifications

If you enable on-chip termination (OCT) calibration, calibration is automatically performed at power up for I/Os connected to the calibration block.

Table 7. OCT Calibration Accuracy Specifications for Intel Cyclone 10 GX Devices

Calibration accuracy for the calibrated on-chip series termination (R_S OCT) and on-chip parallel termination (R_T OCT) are applicable at the moment of calibration. When process, voltage, and temperature (PVT) conditions change after calibration, the tolerance may change.

Symbol	Description	Condition (V)	Resistance Tolerance		Unit
			–E5, –I5	–E6, –I6	
25-Ω and 50-Ω R_S	Internal series termination with calibration (25-Ω and 50-Ω setting)	V_{CCIO} = 1.8, 1.5, 1.2	± 15	± 15	%
34-Ω and 40-Ω R_S	Internal series termination with calibration (34-Ω and 40-Ω setting)	V_{CCIO} = 1.5, 1.25, 1.2	± 15	± 15	%
		V_{CCIO} = 1.35	± 20	± 20	%
48-Ω, 60-Ω, 80-Ω, and 120-Ω R_S	Internal series termination with calibration (48-Ω, 60-Ω, 80-Ω, and 120-Ω setting)	V_{CCIO} = 1.2	± 15	± 15	%
240-Ω R_S	Internal series termination with calibration (240-Ω setting)	V_{CCIO} = 1.2	± 20	± 20	%
30-Ω R_T	Internal parallel termination with calibration (30-Ω setting)	V_{CCIO} = 1.5, 1.35, 1.25	–10 to +40	–10 to +40	%
34-Ω, 48-Ω, 80-Ω, and 240-Ω R_T	Internal parallel termination with calibration (34-Ω, 48-Ω, 80-Ω, and 240-Ω setting)	V_{CCIO} = 1.2	± 15	± 15	%

continued...

Symbol	Description	Condition (V)	Resistance Tolerance		Unit
			–E5, –I5	–E6, –I6	
40-Ω, 60-Ω, and 120-Ω R_T	Internal parallel termination with calibration (40-Ω, 60-Ω, and 120-Ω setting)	V_{CCIO} = 1.5, 1.35, 1.25, 1.2	–10 to +40	–10 to +40	%
		V_{CCIO} = 1.2 (17)	± 15	± 15	%
80-Ω R_T	Internal parallel termination with calibration (80-Ω setting)	V_{CCIO} = 1.2	± 15	± 15	%

Related Information

I/O Standards Support in Intel Cyclone 10 GX Devices

OCT Without Calibration Resistance Tolerance Specifications

Table 8. OCT Without Calibration Resistance Tolerance Specifications for Intel Cyclone 10 GX Devices

This table lists the Intel Cyclone 10 GX OCT without calibration resistance tolerance to PVT changes.

Symbol	Description	Condition (V)	Resistance Tolerance		Unit
			–E5, –I5	–E6, –I6	
25-Ω and 50-Ω R_S	Internal series termination without calibration (25-Ω and 50-Ω setting)	V_{CCIO} = 3.0, 2.5	± 40	± 40	%
		V_{CCIO} = 1.8, 1.5, 1.2	± 50	± 50	%
34-Ω and 40-Ω R_S	Internal series termination without calibration (34-Ω and 40-Ω setting)	V_{CCIO} = 1.5, 1.35, 1.25, 1.2	± 50	± 50	%
48-Ω and 60-Ω R_S	Internal series termination without calibration (48-Ω and 60-Ω setting)	V_{CCIO} = 1.2	± 50	± 50	%
120-Ω R_s	Internal series termination without calibration (120-Ω setting)	V_{CCIO} = 1.2	± 50	± 50	%
100-Ω R_D	Internal differential termination (100-Ω setting)	V_{CCIO} = 1.8	± 35	± 40	%

(17) Only applicable to POD12 I/O standard.

I/O Standard	$V_{IL(DC)}$ (V)		$V_{IH(DC)}$ (V)		$V_{IL(AC)}$ (V)	$V_{IH(AC)}$ (V)	V_{OL} (V)	V_{OH} (V)	I_{OL} (21) (mA)	I_{OH} (21) (mA)
	Min	Max	Min	Max	Max	Min	Max	Min		
SSTL-12/ SSTL-12 Class I, II	—	V_{REF} – 0.10	V_{REF} + 0.10	—	V_{REF} – 0.15	V_{REF} + 0.15	0.2 × V_{CCIO}	0.8 × V_{CCIO}	—	—
HSTL-18 Class I	—	V_{REF} –0.1	V_{REF} + 0.1	—	V_{REF} – 0.2	V_{REF} + 0.2	0.4	V_{CCIO} – 0.4	8	–8
HSTL-18 Class II	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.2	V_{REF} + 0.2	0.4	V_{CCIO} – 0.4	16	–16
HSTL-15 Class I	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.2	V_{REF} + 0.2	0.4	V_{CCIO} – 0.4	8	–8
HSTL-15 Class II	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.2	V_{REF} + 0.2	0.4	V_{CCIO} –0.4	16	–16
HSTL-12 Class I	–0.15	V_{REF} – 0.08	V_{REF} + 0.08	V_{CCIO} + 0.15	V_{REF} – 0.15	V_{REF} + 0.15	0.25 × V_{CCIO}	0.75 × V_{CCIO}	8	–8
HSTL-12 Class II	–0.15	V_{REF} – 0.08	V_{REF} + 0.08	V_{CCIO} + 0.15	V_{REF} – 0.15	V_{REF} + 0.15	0.25 × V_{CCIO}	0.75 × V_{CCIO}	16	–16
HSUL-12	—	V_{REF} – 0.13	V_{REF} + 0.13	—	V_{REF} – 0.22	V_{REF} + 0.22	0.1 × V_{CCIO}	0.9 × V_{CCIO}	—	—
POD12	–0.15	V_{REF} – 0.08	V_{REF} + 0.08	V_{CCIO} + 0.15	V_{REF} – 0.15	V_{REF} + 0.15	(0.7 – 0.15) × V_{CCIO}	(0.7 + 0.15) × V_{CCIO}	—	—

Differential SSTL I/O Standards Specifications

Table 15. Differential SSTL I/O Standards Specifications for Intel Cyclone 10 GX Devices

I/O Standard	V_{CCIO} (V)			$V_{SWING(DC)}$ (V)		$V_{SWING(AC)}$ (V)		$V_{IX(AC)}$ (V)		
	Min	Typ	Max	Min	Max	Min	Max	Min	Typ	Max
SSTL-18 Class I, II	1.71	1.8	1.89	0.25	V_{CCIO} + 0.6	0.5	V_{CCIO} + 0.6	$V_{CCIO}/2$ – 0.175	—	$V_{CCIO}/2$ + 0.175
SSTL-15 Class I, II	1.425	1.5	1.575	0.2	(22)	$2(V_{IH(AC)} – V_{REF})$	$2(V_{REF} – V_{IL(AC)})$	$V_{CCIO}/2$ – 0.15	—	$V_{CCIO}/2$ + 0.15

continued...

(21) To meet the I_{OL} and I_{OH} specifications, you must set the current strength settings accordingly. For example, to meet the SSTL15CI specification (8 mA), you should set the current strength settings to 8 mA. Setting at lower current strength may not meet the I_{OL} and I_{OH} specifications in the datasheet.

Switching Characteristics

This section provides the performance characteristics of Intel Cyclone 10 GX core and periphery blocks for extended grade devices.

Transceiver Performance Specifications

Transceiver Performance for Intel Cyclone 10 GX Devices

Table 18. Transmitter and Receiver Data Rate Performance

Symbol/Description	Condition	Datarate	Unit
Chip-to-Chip (29)	Maximum data rate V_{CCR_GXB} = V_{CCT_GXB} = 1.03 V	12.5	Gbps
	Maximum data rate V_{CCR_GXB} = V_{CCT_GXB} = 0.95 V	11.3	Gbps
	Minimum Data Rate	1.0 (30)	Gbps
Backplane	Maximum data rate V_{CCR_GXB} = V_{CCT_GXB} = 1.03 V	6.6	Gbps
	Minimum Data Rate	1.0 (30)	Gbps

Table 19. ATX PLL and Fractional PLL (fPLL) Performance

Symbol/Description	Condition	Frequency	Unit
Supported Output Frequency	Maximum Frequency	6.25	GHz
	Minimum Frequency	500	MHz

(29) Chip-to-chip links are applications with short reach channels.

(30) Intel Cyclone 10 GX transceivers can support data rates down to 125 Mbps with over sampling. You must create your own over sampling logic.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_{DLOCK}	Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays)	—	—	—	1	ms
t_{PLL_PSERR}	Accuracy of PLL phase shift	—	—	—	±50	ps
t_{ARESET}	Minimum pulse width on the areset signal	—	10	—	—	ns
t_{INCCJ} (54)(55)	Input clock cycle-to-cycle jitter	F_{REF} ≥ 100 MHz	—	—	0.15	UI (p-p)
		F_{REF} < 100 MHz	—	—	750	ps (p-p)
t_{OUTPJ_DC}	Period jitter for dedicated clock output	F_{OUT} ≥ 100 MHz	—	—	175	ps (p-p)
		F_{OUT} < 100 MHz	—	—	17.5	mUI (p-p)
t_{OUTCCJ_DC}	Cycle-to-cycle jitter for dedicated clock output	F_{OUT} ≥ 100 MHz	—	—	175	ps (p-p)
		F_{OUT} < 100 MHz	—	—	17.5	mUI (p-p)
t_{OUTPJ_IO} (56)	Period jitter for clock output on the regular I/O	F_{OUT} ≥ 100 MHz	—	—	600	ps (p-p)
		F_{OUT} < 100 MHz	—	—	60	mUI (p-p)
t_{OUTCCJ_IO} (56)	Cycle-to-cycle jitter for clock output on the regular I/O	F_{OUT} ≥ 100 MHz	—	—	600	ps (p-p)
		F_{OUT} < 100 MHz	—	—	60	mUI (p-p)
$t_{CASC\_OUTPJ\_DC}$	Period jitter for dedicated clock output in cascaded PLLs	F_{OUT} ≥ 100 MHz	—	—	175	ps (p-p)
		F_{OUT} < 100 MHz	—	—	17.5	mUI (p-p)

Related Information

Memory Output Clock Jitter Specifications on page 43
Provides more information about the external memory interface clock output jitter specifications.

(54) A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source with jitter < 120 ps.

(55) F_{REF} is f_{IN}/N, specification applies when $N = 1$.

(56) External memory interface clock output jitter specifications use a different measurement method, which are available in Memory Output Clock Jitter Specification for Intel Cyclone 10 GX Devices table.

Table 33. Memory Block Performance Specifications for Intel Cyclone 10 GX Devices

Memory	Mode	Performance			
		–E5, –I5	–E6	–I6	Unit
MLAB	Single port, all supported widths (×16/×32)	570	490	490	MHz
	Simple dual-port, all supported widths (×16/×32)	570	490	490	MHz
	Simple dual-port with the read-during-write option set to **Old Data**, all supported widths	400	330	330	MHz
	ROM, all supported width (×16/×32)	570	490	490	MHz
M20K Block	Single-port, all supported widths	625	530	510	MHz
	Simple dual-port, all supported widths	625	530	510	MHz
	Simple dual-port with the read-during-write option set to **Old Data**, all supported widths	470	410	410	MHz
	Simple dual-port with ECC enabled, 512 × 32	410	360	360	MHz
	Simple dual-port with ECC and optional pipeline registers enabled, 512 × 32	520	470	470	MHz
	True dual port, all supported widths	600	480	480	MHz
	ROM, all supported widths	625	530	510	MHz

Temperature Sensing Diode Specifications

Internal Temperature Sensing Diode Specifications

Table 34. Internal Temperature Sensing Diode Specifications for Intel Cyclone 10 GX Devices

Temperature Range	Accuracy	Offset Calibrated Option	Sampling Rate	Conversion Time	Resolution
–40 to 100°C	±5°C	No	1 MHz	< 5 ms	10 bits

Related Information

Transfer Function for Internal TSD

Provides the transfer function for the internal TSD.

Periphery Performance Specifications

This section describes the periphery performance, high-speed I/O, and external memory interface.

Actual achievable frequency depends on design and system specific factors. Ensure proper timing closure in your design and perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

High-Speed I/O Specifications

Table 37. High-Speed I/O Specifications for Intel Cyclone 10 GX Devices

When serializer/deserializer (SERDES) factor J = 3 to 10, use the SERDES block.

For LVDS applications, you must use the PLLs in integer PLL mode.

You must calculate the leftover timing margin in the receiver by performing link timing closure analysis. You must consider the board skew margin, transmitter channel-to-channel skew, and receiver sampling margin to determine the leftover timing margin.

The Intel Cyclone 10 GX devices support the following output standards using true LVDS output buffer types on all I/O banks:

- True RSDS output standard with data rates of up to 360 Mbps
- True mini-LVDS output standard with data rates of up to 400 Mbps

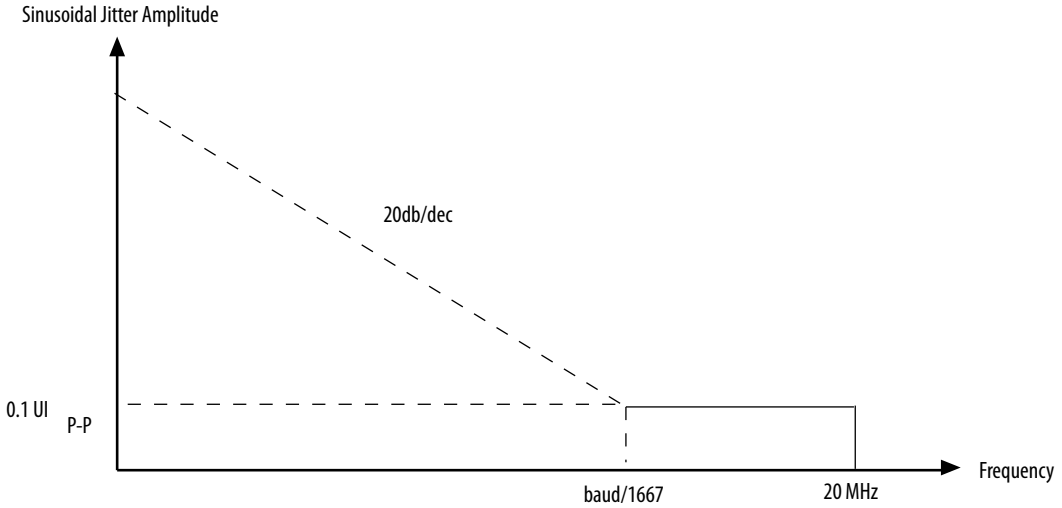
Symbol	Condition	–E5, –I5			–E6, –I6			Unit
		Min	Typ	Max	Min	Typ	Max	
f_{HSCLK_in} (input clock frequency) True Differential I/O Standards	Clock boost factor W = 1 to 40 (57)	10	—	700	10	—	625	MHz
f_{HSCLK_in} (input clock frequency) Single Ended I/O Standards	Clock boost factor W = 1 to 40 (57)	10	—	625	10	—	525	MHz
f_{HSCLK_OUT} (output clock frequency)	—	—	—	700 (58)	—	—	625 (58)	MHz

continued...

(57) Clock Boost Factor (W) is the ratio between the input data rate and the input clock rate.

(58) This is achieved by using the PHY clock network.

Figure 4. LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specifications for a Data Rate Less than 1.4 Gbps



Memory Standards Supported by the Hard Memory Controller

Table 40. Memory Standards Supported by the Hard Memory Controller for Intel Cyclone 10 GX Devices

This table lists the overall capability of the hard memory controller. For specific details, refer to the External Memory Interface Spec Estimator.

Memory Standard	Rate Support	Speed Grade	Ping Pong PHY Support	Maximum Frequency (MHz)	
				I/O Bank	3 V I/O Bank
DDR3 SDRAM	Half rate	–5	Yes	533	225
			—	533	225
		–6	Yes	466	166
			—	466	166
	Quarter rate	–5	Yes	933	450
			—	933	450
		–6	Yes	933	333

continued...

DQS Logic Block Specifications

Table 42. DQS Phase Shift Error Specifications for DLL-Delayed Clock (t_{DQS_PSERR}) for Intel Cyclone 10 GX Devices

This error specification is the absolute maximum and minimum error.

Symbol	Performance (for All Speed Grades)	Unit
t_{DQS_PSERR}	5	ps

Memory Output Clock Jitter Specifications

Table 43. Memory Output Clock Jitter Specifications for Intel Cyclone 10 GX Devices

The clock jitter specification applies to the memory output clock pins clocked by an I/O PLL, or generated using differential signal-splitter and double data I/O circuits clocked by a PLL output routed on a PHY clock network as specified. Intel recommends using PHY clock networks for better jitter performance.

The memory output clock jitter is applicable when an input jitter of 10 ps peak-to-peak is applied with bit error rate (BER) 10^{-12}, equivalent to 14 sigma.

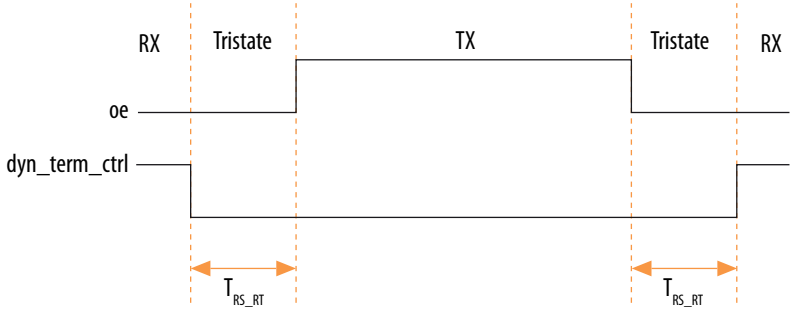
Protocol	Parameter	Symbol	Data Rate (Mbps)	Min	Max	Unit
DDR3	Clock period jitter	$t_{JIT(per)}$	1,866	–40	40	ps
	Cycle-to-cycle period jitter	$t_{JIT(cc)}$	1,866	–40	40	ps
	Duty cycle jitter	$t_{JIT(duty)}$	1,866	–40	40	ps

OCT Calibration Block Specifications

Table 44. OCT Calibration Block Specifications for Intel Cyclone 10 GX Devices

Symbol	Description	Min	Typ	Max	Unit
OCTUSRCLK	Clock required by OCT calibration blocks	—	—	20	MHz
T_{OCTCAL}	Number of OCTUSRCLK clock cycles required for R_S OCT /R_T OCT calibration	> 2000	—	—	Cycles
$T_{OCTSHIFT}$	Number of OCTUSRCLK clock cycles required for OCT code to shift out	—	32	—	Cycles
T_{RS_RT}	Time required between the `dyn_term_ctrl` and `oe` signal transitions in a bidirectional I/O buffer to dynamically switch between R_S OCT and R_T OCT	—	2.5	—	ns

Figure 5. Timing Diagram for on oe and dyn_term_ctrl Signals



Configuration Specifications

This section provides configuration specifications and timing for Intel Cyclone 10 GX devices.

POR Specifications

Power-on reset (POR) delay is defined as the delay between the time when all the power supplies monitored by the POR circuitry reach the minimum recommended operating voltage to the time when the nSTATUS is released high and your device is ready to begin configuration.

Table 45. Fast and Standard POR Delay Specification for Intel Cyclone 10 GX Devices

POR Delay	Minimum	Maximum	Unit
Fast	4	12 (68)	ms
Standard	100	300	ms

Related Information

MSEL Pin Settings
Provides more information about POR delay based on MSEL pin settings for each configuration scheme.

(68) The maximum pulse width of the fast POR delay is 12 ms, providing enough time for the PCIe hard IP to initialize after the POR trip.

Table 47. DCLK-to-DATA[] Ratio for Intel Cyclone 10 GX Devices

You cannot turn on encryption and compression at the same time for Intel Cyclone 10 GX devices.

Configuration Scheme	Encryption	Compression	DCLK-to-DATA[] Ratio (r)
FPP (8-bit wide)	Off	Off	1
	On	Off	1
	Off	On	2
FPP (16-bit wide)	Off	Off	1
	On	Off	2
	Off	On	4
FPP (32-bit wide)	Off	Off	1
	On	Off	4
	Off	On	8

FPP Configuration Timing when DCLK-to-DATA[] = 1

Note: When you enable decompression or the design security feature, the DCLK-to-DATA[] ratio varies for FPP ×8, FPP ×16, and FPP ×32. For the respective DCLK-to-DATA[] ratio, refer to the DCLK-to-DATA[] Ratio for Intel Cyclone 10 GX Devices table.

Table 48. FPP Timing Parameters When the DCLK-to-DATA[] Ratio is 1 for Intel Cyclone 10 GX Devices

Use these timing parameters when the decompression and design security features are disabled.

Symbol	Parameter	Minimum	Maximum	Unit
t_{CF2CD}	nCONFIG low to CONF_DONE low	480	1,440	ns
t_{CF2ST0}	nCONFIG low to nSTATUS low	320	960	ns
t_{CFG}	nCONFIG low pulse width	2	—	µs
t_{STATUS}	nSTATUS low pulse width	268	3,000 (70)	µs
t_{CF2ST1}	nCONFIG high to nSTATUS high	—	3,000 (71)	µs

continued...

(70) This value is applicable if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.

Symbol	Parameter	Minimum	Maximum	Unit
t_{CF2CK} (72)	nCONFIG high to first rising edge on DCLK	3,010	—	µs
t_{ST2CK} (72)	nSTATUS high to first rising edge of DCLK	10	—	µs
t_{DSU}	DATA[] setup time before rising edge on DCLK	5.5	—	ns
t_{DH}	DATA[] hold time after rising edge on DCLK	0	—	ns
t_{CH}	DCLK high time	0.45 × 1/f_{MAX}	—	s
t_{CL}	DCLK low time	0.45 × 1/f_{MAX}	—	s
t_{CLK}	DCLK period	1/f_{MAX}	—	s
f_{MAX}	DCLK frequency (FPP ×8/×16/×32)	—	100	MHz
t_{CD2UM}	CONF_DONE high to user mode (73)	175	830	µs
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period	—	—
t_{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t_{CD2CU} + (600 × CLKUSR period)	—	—

Related Information

FPP Configuration Timing
Provides the FPP configuration timing waveforms.

(71) This value is applicable if you do not delay configuration by externally holding the nSTATUS low.

(72) If nSTATUS is monitored, follow the t_{ST2CK} specification. If nSTATUS is not monitored, follow the t_{CF2CK} specification.

(73) The minimum and maximum numbers apply only if you chose the internal oscillator as the clock source for initializing the device.

Related Information

- PS Configuration Timing on page 50
- AS Configuration Timing
  Provides the AS configuration timing waveform.

DCLK Frequency Specification in the AS Configuration Scheme

Table 51. DCLK Frequency Specification in the AS Configuration Scheme

This table lists the internal clock frequency specification for the AS configuration scheme.

The DCLK frequency specification applies when you use the internal oscillator as the configuration clock source.

The AS multi-device configuration scheme does not support DCLK frequency of 100 MHz.

You can only set 12.5, 25, 50, and 100 MHz in the Intel Quartus Prime software.

Parameter	Minimum	Typical	Maximum	Intel Quartus Prime Software Settings	Unit
DCLK frequency in AS configuration scheme	5.3	7.5	9.7	12.5	MHz
	10.5	15.0	19.3	25.0	MHz
	21.0	30.0	38.5	50.0	MHz
	42.0	60.0	77.0	100.0	MHz

PS Configuration Timing

Table 52. PS Timing Parameters for Intel Cyclone 10 GX Devices

Symbol	Parameter	Minimum	Maximum	Unit
t_{CF2CD}	nCONFIG low to CONF_DONE low	480	1,440	ns
t_{CF2ST0}	nCONFIG low to nSTATUS low	320	960	ns
t_{CFG}	nCONFIG low pulse width	2	—	µs
t_{STATUS}	nSTATUS low pulse width	268	3,000 (78)	µs
t_{CF2ST1}	nCONFIG high to nSTATUS high	—	3,000 (79)	µs

continued...

Table 54. Configuration Bit Stream Sizes for Intel Cyclone 10 GX Devices

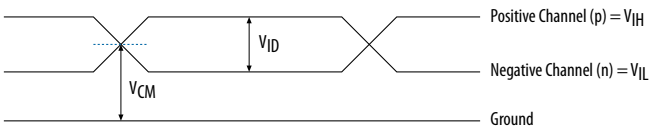
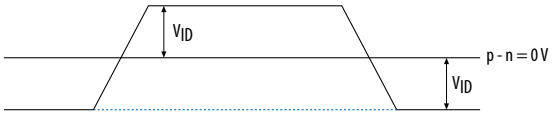
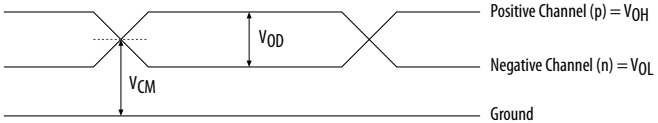
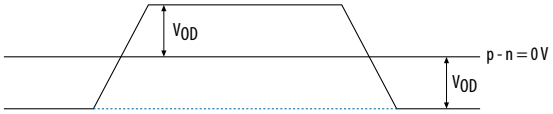
Use this table to estimate the file size before design compilation. Different configuration file formats, such as a hexadecimal file (`.hex`) or tabular text file (`.ttf`) format, have different file sizes.

For the different types of configuration file and file sizes, refer to the Intel Quartus Prime software. However, for a specific version of the Intel Quartus Prime software, any design targeted for the same device has the same uncompressed configuration file size.

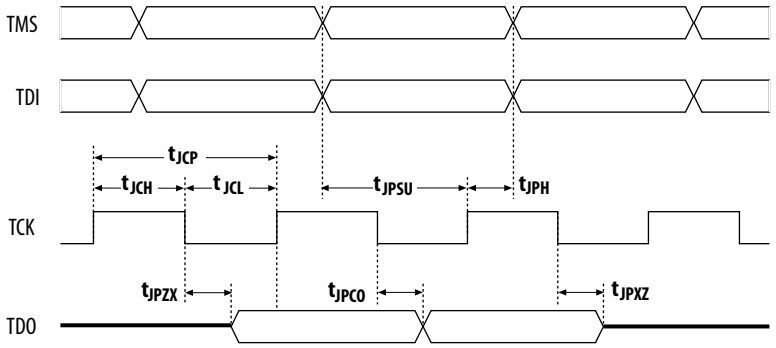
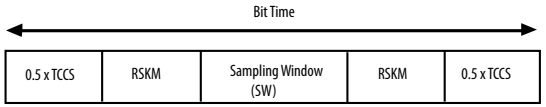
I/O configuration shift register (IOCSR) is a long shift register that facilitates the device I/O peripheral settings. The IOCSR bit stream is part of the uncompressed configuration bit stream, and it is specifically for the Configuration via Protocol (CvP) feature.

Uncompressed configuration bit stream sizes are subject to change for improvements and optimizations in the configuration algorithm.

Variant	Product Line	Uncompressed Configuration Bit Stream Size (bits)	IOCSR Bit Stream Size (bits)	Recommended EPCQ-L Serial Configuration Device
Intel Cyclone 10 GX	GX 085	81,923,582	2,507,264	EPCQ-L256 or higher density
	GX 105	81,923,582	2,507,264	EPCQ-L256 or higher density
	GX 150	81,923,582	2,507,264	EPCQ-L256 or higher density
	GX 220	81,923,582	2,507,264	EPCQ-L256 or higher density

Term	Definition
	Single-Ended Waveform  **Differential Waveform**  Transmitter Output Waveforms **Single-Ended Waveform**  **Differential Waveform** 
f_{HSCLK}	I/O PLL input clock frequency.
f_{HSDR}	High-speed I/O block—Maximum/minimum LVDS data transfer rate (f_{HSDR} = 1/TUI), non-DPA.
$f_{HSDRDPA}$	High-speed I/O block—Maximum/minimum LVDS data transfer rate ($f_{HSDRDPA}$ = 1/TUI), DPA.
J	High-speed I/O block—Deserialization factor (width of parallel data bus).
JTAG Timing Specifications	JTAG Timing Specifications:

continued...

Term	Definition
	
R_L	Receiver differential input discrete resistor (external to the Intel Cyclone 10 GX device).
Sampling window (SW)	Timing Diagram—the period of time during which the data must be valid in order to capture it correctly. The setup and hold times determine the ideal strobe position in the sampling window, as shown: 
Single-ended voltage referenced I/O standard	The JEDEC standard for the SSTL and HSTL I/O defines both the AC and DC input signal values. The AC values indicate the voltage levels at which the receiver must meet its timing specifications. The DC values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. After the receiver input has crossed the AC value, the receiver changes to the new logic state. The new logic state is then maintained as long as the input stays beyond the DC threshold. This approach is intended to provide predictable receiver timing in the presence of input waveform ringing. Single-Ended Voltage Referenced I/O Standard

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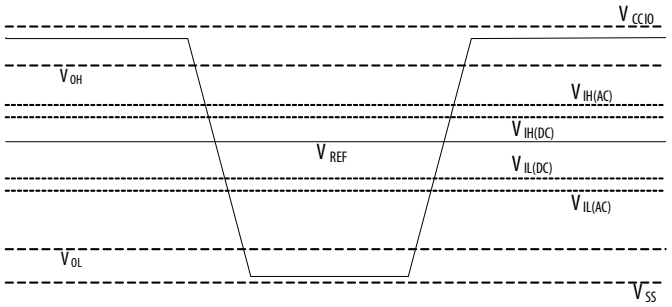
Term	Definition
	
t_C	High-speed receiver/transmitter input and output clock period.
TCCS (channel-to-channel-skew)	The timing difference between the fastest and slowest output edges, including the t_{CO} variation and clock skew, across channels driven by the same PLL. The clock is included in the TCCS measurement (refer to the Timing Diagram figure under SW in this table).
t_{DUTY}	High-speed I/O block—Duty cycle on high-speed transmitter output clock.
t_{FALL}	Signal high-to-low transition time (80–20%)
t_{INCCJ}	Cycle-to-cycle jitter tolerance on the PLL clock input
t_{OUTPJ_IO}	Period jitter on the GPIO driven by a PLL
t_{OUTPJ_DC}	Period jitter on the dedicated clock output driven by a PLL
t_{RISE}	Signal low-to-high transition time (20–80%)
Timing Unit Interval (TUI)	The timing budget allowed for skew, propagation delays, and the data sampling window. (TUI = 1/(Receiver Input Clock Frequency Multiplication Factor) = t_C/w).
$V_{CM(DC)}$	DC Common mode input voltage.
V_{ICM}	Input Common mode voltage—The common mode of the differential signal at the receiver.
V_{ID}	Input differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the receiver.
$V_{DIF(AC)}$	AC differential input voltage—Minimum AC input differential voltage required for switching.
$V_{DIF(DC)}$	DC differential input voltage— Minimum DC input differential voltage required for switching.
V_{IH}	Voltage input high—The minimum positive voltage applied to the input which is accepted by the device as a logic high.

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