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Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	54770
Number of Logic Elements/Cells	150000
Total RAM Bits	10907648
Number of I/O	284
Number of Gates	-
Voltage - Supply	0.9V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	780-BBGA, FCBGA
Supplier Device Package	780-FBGA, FC (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/intel/10cx150yf780i5g

Contents

Intel® Cyclone® 10 GX Device Datasheet

This datasheet describes the electrical characteristics, switching characteristics, configuration specifications, and I/O timing for Intel® Cyclone® 10 GX devices.

Intel Cyclone 10 GX devices are offered in extended and industrial grades. Extended devices are offered in –E5 (fastest) and –E6 speed grades. Industrial grade devices are offered in the –I5 and –I6 speed grades.

Related Information

Intel Cyclone 10 GX Device Overview
Provides more information about the densities and packages in the Intel Cyclone 10 GX devices.

Electrical Characteristics

The following sections describe the operating conditions and power consumption of Intel Cyclone 10 GX devices.

Operating Conditions

Intel Cyclone 10 GX devices are rated according to a set of defined parameters. To maintain the highest possible performance and reliability of the Intel Cyclone 10 GX devices, you must consider the operating requirements described in this section.

Absolute Maximum Ratings

This section defines the maximum operating conditions for Intel Cyclone 10 GX devices. The values are based on experiments conducted with the devices and theoretical modeling of breakdown and damage mechanisms. The functional operation of the device is not implied for these conditions.

Caution: Conditions outside the range listed in the following table may cause permanent damage to the device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse effects on the device.

Symbol	Description	Condition	Minimum [8]	Typical	Maximum [8]	Unit
		1.2 V	1.14	1.2	1.26	V
V_{CCERAM}	Embedded memory power supply	0.9 V	0.87	0.9	0.93	V
V_{CCBAT} [9]	Battery back-up power supply (For design security volatile key register)	1.8 V	1.71	1.8	1.89	V
		1.2 V	1.14	1.2	1.26	V
V_{CCPT}	Power supply for programmable power technology and I/O pre-driver	1.8 V	1.71	1.8	1.89	V
V_{CCIO}	I/O buffers power supply	3.0 V (for 3 V I/O only)	2.85	3.0	3.15	V
		2.5 V (for 3 V I/O only)	2.375	2.5	2.625	V
		1.8 V	1.71	1.8	1.89	V
		1.5 V	1.425	1.5	1.575	V
		1.35 V	(10)	1.35	(10)	V
		1.25 V	1.19	1.25	1.31	V
		1.2 V	(10)	1.2	(10)	V
V_{CCA_PLL}	PLL analog voltage regulator power supply	—	1.71	1.8	1.89	V
V_{REFP_ADC}	Precision voltage reference for voltage sensor	—	1.2475	1.25	1.2525	V

continued...

(8) This value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

(9) If you do not use the design security feature in Intel Cyclone 10 GX devices, connect V_{CCBAT} to a 1.5-V to 1.8-V power supply. Intel Cyclone 10 GX power-on reset (POR) circuitry monitors V_{CCBAT}. Intel Cyclone 10 GX devices do not exit POR if V_{CCBAT} is not powered up.

(10) For minimum and maximum voltage values, refer to the I/O Standard Specifications section.

Symbol	Description	Condition	Minimum (14)	Typical	Maximum (14)	Unit
		Backplane ≤ 6.6 Gbps				
		Chip-to-chip ≤ 11.3 Gbps	0.92	0.95	0.98	V
$V_{CCR\_GXB[L1][C,D]}$	Receiver power supply	Chip-to-chip ≤ 12.5 Gbps Or Backplane ≤ 6.6 Gbps	1.0	1.03	1.06	V
		Chip-to-chip ≤ 11.3 Gbps	0.92	0.95	0.98	V
V_{CCH_GXBL}	Transceiver output buffer power supply	—	1.710	1.8	1.890	V

Related Information

- Transceiver Performance for Intel Cyclone 10 GX Devices on page 21
- Intel Cyclone 10 GX Pin Connection Guidelines

DC Characteristics

Supply Current and Power Consumption

Intel offers two ways to estimate power for your design—the Excel-based Early Power Estimator (EPE) and the Intel Quartus® Prime Power Analyzer feature.

Use the Excel-based EPE before you start your design to estimate the supply current for your design. The EPE provides a magnitude estimate of the device power because these currents vary greatly with the usage of the resources.

The Intel Quartus Prime Power Analyzer provides better quality estimates based on the specifics of the design after you complete place-and-route. The Power Analyzer can apply a combination of user-entered, simulation-derived, and estimated signal activities that, when combined with detailed circuit models, yield very accurate power estimates.

(14) This value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

Switching Characteristics

This section provides the performance characteristics of Intel Cyclone 10 GX core and periphery blocks for extended grade devices.

Transceiver Performance Specifications

Transceiver Performance for Intel Cyclone 10 GX Devices

Table 18. Transmitter and Receiver Data Rate Performance

Symbol/Description	Condition	Datarate	Unit
Chip-to-Chip (29)	Maximum data rate V_{CCR_GXB} = V_{CCT_GXB} = 1.03 V	12.5	Gbps
	Maximum data rate V_{CCR_GXB} = V_{CCT_GXB} = 0.95 V	11.3	Gbps
	Minimum Data Rate	1.0 (30)	Gbps
Backplane	Maximum data rate V_{CCR_GXB} = V_{CCT_GXB} = 1.03 V	6.6	Gbps
	Minimum Data Rate	1.0 (30)	Gbps

Table 19. ATX PLL and Fractional PLL (fPLL) Performance

Symbol/Description	Condition	Frequency	Unit
Supported Output Frequency	Maximum Frequency	6.25	GHz
	Minimum Frequency	500	MHz

(29) Chip-to-chip links are applications with short reach channels.

(30) Intel Cyclone 10 GX transceivers can support data rates down to 125 Mbps with over sampling. You must create your own over sampling logic.

Symbol/Description	Condition	Min	Typ	Max	Unit
Input Reference Clock Frequency (CMU PLL)		61	—	800	MHz
Input Reference Clock Frequency (ATX PLL)		100	—	800	MHz
Input Reference Clock Frequency (fPLL PLL)		25 (32) / 50	—	800	MHz
Rise time	20% to 80%	—	—	400	ps
Fall time	80% to 20%	—	—	400	ps
Duty cycle	—	45	—	55	%
Spread-spectrum modulating clock frequency	PCIe	30	—	33	kHz
Spread-spectrum downspread	PCIe	—	0 to –0.5	—	%
On-chip termination resistors	—	—	100	—	Ω
Absolute V_{MAX}	Dedicated reference clock pin	—	—	1.6	V
	RX pin as a reference clock	—	—	1.2	V
Absolute V_{MIN}	—	–0.4	—	—	V
Peak-to-peak differential input voltage	—	200	—	1600	mV
V_{ICM} (AC coupled)	V_{CCR_GXB} = 0.95 V	—	0.95	—	V
	V_{CCR_GXB} = 1.03 V	—	1.03	—	V
V_{ICM} (DC coupled)	HCSL I/O standard for PCIe reference clock	250	—	550	mV
Transmitter REFCLK Phase Noise (622 MHz) (33)	100 Hz	—	—	–70	dBc/Hz
	1 kHz	—	—	–90	dBc/Hz

continued...

(32) 25 MHz is for HDMI applications only.

(33) To calculate the REFCLK phase noise requirement at frequencies other than 622 MHz, use the following formula: REFCLK phase noise at f (MHz) = REFCLK phase noise at 622 MHz + 20*log(f/622).

Table 25. Receiver Specifications

Symbol/Description	Condition	Min	Typ	Max	Unit
Supported I/O Standards	—	High Speed Differential I/O, CML , Differential LVPECL , and LVDS(35)			
Absolute V_{MAX} for a receiver pin (36)	—	—	—	1.2	V
Absolute V_{MIN} for a receiver pin (37)	—	-0.4	—	—	V
Maximum peak-to-peak differential input voltage V_{ID} (diff p-p) before device configuration	—	—	—	1.6	V
Maximum peak-to-peak differential input voltage V_{ID} (diff p-p) after device configuration	V_{CCR_GXB} = 0.95 V	—	—	2.4	V
	V_{CCR_GXB} = 1.03 V	—	—	2.0	V
Minimum differential eye opening at receiver serial input pins (38)	—	50	—	—	mV
Differential on-chip termination resistors	85-Ω setting	—	85 ± 30%	—	Ω
	100-Ω setting	—	100 ± 30%	—	Ω
V_{ICM} (AC and DC coupled) (39)	V_{CCR_GXB} = 0.95 V	—	600	—	mV
	V_{CCR_GXB} = 1.03 V	—	700	—	mV

continued...

(35) CML, Differential LVPECL, and LVDS are only used on AC coupled links.

(36) The device cannot tolerate prolonged operation at this absolute maximum.

(37) The device cannot tolerate prolonged operation at this absolute minimum.

(38) The differential eye opening specification at the receiver input pins assumes that Receiver Equalization is disabled. If you enable Receiver Equalization, the receiver circuitry can tolerate a lower minimum eye opening, depending on the equalization level.

(39) Intel Cyclone 10 GX devices support DC coupling to other Intel Cyclone 10 GX devices and other devices with a transmitter that has matching common mode voltage.

Symbol/Description	Condition	Min	Typ	Max	Unit
	100-Ω setting	—	100 ± 20%	—	Ω
V_{OCM} (AC coupled)	V_{CCT_GXB} = 0.95 V	—	450	—	mV
	V_{CCT_GXB} = 1.03 V	—	500	—	mV
V_{OCM} (DC coupled)	V_{CCT_GXB} = 0.95 V	—	450	—	mV
	V_{CCT_GXB} = 1.03 V	—	500	—	mV
Rise time (45)	20% to 80%	20	—	130	ps
Fall time (45)	80% to 20%	20	—	130	ps
Intra-differential pair skew	TX V_{CM} = 0.5 V and slew rate setting of SLEW_R5 (46)	—	—	15	ps

Table 27. Typical Transmitter V_{OD} Settings

Symbol	V_{OD} Setting	V_{OD}-to-V_{CCT_GXB} Ratio
V_{OD} differential value = V_{OD}-to-V_{CCT_GXB} ratio x V_{CCT_GXB}	31	1.00
	30	0.97
	29	0.93
	28	0.90
	27	0.87
	26	0.83
	25	0.80
	24	0.77
	23	0.73
	22	0.70

continued...

(45) The Intel Quartus Prime software automatically selects the appropriate slew rate depending on the design configurations.

(46) SLEW_R1 is the slowest and SLEW_R5 is the fastest. SLEW_R6 and SLEW_R7 are not used.

Core Performance Specifications

Clock Tree Specifications

Table 29. Clock Tree Performance for Intel Cyclone 10 GX Devices

Parameter	Performance (All Speed Grades)	Unit
Global clock, regional clock, and small periphery clock	644	MHz
Large periphery clock	525	MHz

PLL Specifications

Fractional PLL Specifications

Table 30. Fractional PLL Specifications for Intel Cyclone 10 GX Devices

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{IN}	Input clock frequency	—	30	—	800 (49)	MHz
f_{INPFD}	Input clock frequency to the phase frequency detector (PFD)	—	30	—	700	MHz
f_{CASC_INPFD}	Input clock frequency to the PFD of destination cascade PLL	—	30	—	60	MHz
f_{VCO}	PLL voltage-controlled oscillator (VCO) operating range	—	6	—	12.5	GHz
$t_{EINDUTY}$	Input clock duty cycle	—	45	—	55	%
f_{OUT}	Output frequency for internal global or regional clock	—	—	—	644	MHz
$f_{DYCONFIGCLK}$	Dynamic configuration clock for `reconfig_clk`	—	—	—	100	MHz

continued...

(49) This specification is limited by the I/O maximum frequency. The maximum achievable I/O frequency is different for each I/O standard and is depends on design and system specific factors. Ensure proper timing closure in your design and perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_{LOCK}	Time required to lock from end-of-device configuration or deassertion of `pll_powerdown`	—	—	—	1	ms
t_{DLOCK}	Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays)	—	—	—	1	ms
f_{CLBW}	PLL closed-loop bandwidth	—	0.3	—	4	MHz
t_{PLL_PSERR}	Accuracy of PLL phase shift	—	—	—	50	ps
t_{ARESET}	Minimum pulse width on the `pll_powerdown` signal	—	10	—	—	ns
t_{INCCJ} (50)(51)	Input clock cycle-to-cycle jitter	$F_{REF} \geq 100$ MHz	—	—	0.13	UI (p-p)
		$F_{REF} < 100$ MHz	—	—	650	ps (p-p)
t_{OUTPJ} (52)	Period jitter for clock output	$F_{OUT} \geq 100$ MHz	—	—	600	ps (p-p)
		$F_{OUT} < 100$ MHz	—	—	60	mUI (p-p)
t_{OUTCCJ} (52)	Cycle-to-cycle jitter for clock output	$F_{OUT} \geq 100$ MHz	—	—	600	ps (p-p)
		$F_{OUT} < 100$ MHz	—	—	60	mUI (p-p)
dK_{BIT}	Bit number of Delta Sigma Modulator (DSM)	—	—	32	—	bit

Related Information

Memory Output Clock Jitter Specifications on page 43
Provides more information about the external memory interface clock output jitter specifications.

(50) A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source with jitter < 120 ps.

(51) F_{REF} is f_{IN}/N, specification applies when $N = 1$.

(52) External memory interface clock output jitter specifications use a different measurement method, which are available in Memory Output Clock Jitter Specification for Intel Cyclone 10 GX Devices table.

Table 33. Memory Block Performance Specifications for Intel Cyclone 10 GX Devices

Memory	Mode	Performance			
		–E5, –I5	–E6	–I6	Unit
MLAB	Single port, all supported widths (×16/×32)	570	490	490	MHz
	Simple dual-port, all supported widths (×16/×32)	570	490	490	MHz
	Simple dual-port with the read-during-write option set to **Old Data**, all supported widths	400	330	330	MHz
	ROM, all supported width (×16/×32)	570	490	490	MHz
M20K Block	Single-port, all supported widths	625	530	510	MHz
	Simple dual-port, all supported widths	625	530	510	MHz
	Simple dual-port with the read-during-write option set to **Old Data**, all supported widths	470	410	410	MHz
	Simple dual-port with ECC enabled, 512 × 32	410	360	360	MHz
	Simple dual-port with ECC and optional pipeline registers enabled, 512 × 32	520	470	470	MHz
	True dual port, all supported widths	600	480	480	MHz
	ROM, all supported widths	625	530	510	MHz

Temperature Sensing Diode Specifications

Internal Temperature Sensing Diode Specifications

Table 34. Internal Temperature Sensing Diode Specifications for Intel Cyclone 10 GX Devices

Temperature Range	Accuracy	Offset Calibrated Option	Sampling Rate	Conversion Time	Resolution
–40 to 100°C	±5°C	No	1 MHz	< 5 ms	10 bits

Related Information

Transfer Function for Internal TSD

Provides the transfer function for the internal TSD.

Symbol		Condition	–E5, –I5			–E6, –I6			Unit
			Min	Typ	Max	Min	Typ	Max	
Transmitter	True Differential I/O Standards - f_{HSDR} (data rate) (59)	SERDES factor J = 4 to 10 (60)(61)(62)	(62)	—	1434	(62)	—	1250	Mbps
		SERDES factor J = 3 (60)(61)(62)	(62)	—	1076	(62)	—	938	Mbps
		SERDES factor J = 2, uses DDR registers	(62)	—	275 (63)	(62)	—	250 (63)	Mbps
		SERDES factor J = 1, uses DDR registers	(62)	—	275 (63)	(62)	—	250 (63)	Mbps
	$t_{x\ Jitter}$ - True Differential I/O Standards	Total jitter for data rate, 600 Mbps – 1.6 Gbps	—	—	200	—	—	250	ps
		Total jitter for data rate, < 600 Mbps	—	—	0.12	—	—	0.15	UI
	t_{DUTY} (64)	TX output clock duty cycle for Differential I/O Standards	45	50	55	45	50	55	%
	$t_{RISE\ \&}$ & t_{FALL} (61) (65)	True Differential I/O Standards	—	—	180	—	—	200	ps

continued...

(59) Requires package skew compensation with PCB trace length.

(60) The F_{max} specification is based on the fast clock used for serial data. The interface F_{max} is also dependent on the parallel clock domain which is design dependent and requires timing analysis.

(61) The V_{CC} and V_{CCP} must be on a combined power layer and a maximum load of 5 pF for chip-to-chip interface.

(62) The minimum specification depends on the clock source (for example, the PLL and clock pin) and the clock routing resource (global, regional, or local) that you use. The I/O differential buffer and serializer do not have a minimum toggle rate.

(63) The maximum ideal data rate is the SERDES factor (J) x the PLL maximum output frequency (f_{OUT}) provided you can close the design timing and the signal integrity meets the interface requirements.

(64) Not applicable for DIVCLK = 1.

Memory Standard	Rate Support	Speed Grade	Ping Pong PHY Support	Maximum Frequency (MHz)	
				I/O Bank	3 V I/O Bank
			—	933	333
DDR3L SDRAM	Half rate	–5	Yes	533	225
			—	533	225
		–6	Yes	466	166
			—	466	166
	Quarter rate	–5	Yes	933	450
			—	933	450
		–6	Yes	933	333
			—	933	333
LPDDR3 SDRAM	Half rate	–5	—	400	225
		–6	—	333	166
	Quarter rate	–5	—	800	450
		–6	—	666	333

Related Information

External Memory Interface Spec Estimator
Provides the specific details of the memory standards supported.

DLL Range Specifications

Table 41. DLL Frequency Range Specifications for Intel Cyclone 10 GX Devices

Intel Cyclone 10 GX devices support memory interface frequencies lower than 600 MHz, although the reference clock that feeds the DLL must be at least 600 MHz. To support interfaces below 600 MHz, multiply the reference clock feeding the DLL to ensure the frequency is within the supported range.

Parameter	Performance (for All Speed Grades)	Unit
DLL operating frequency range	600 – 1333	MHz

JTAG Configuration Timing

Table 46. JTAG Timing Parameters and Values for Intel Cyclone 10 GX Devices

Symbol	Description	Min	Max	Unit
t_{JCP}	TCK clock period	30, 167 (69)	—	ns
t_{JCH}	TCK clock high time	14	—	ns
t_{JCL}	TCK clock low time	14	—	ns
$t_{JPSU\ (TDI)}$	TDI JTAG port setup time	2	—	ns
$t_{JPSU\ (TMS)}$	TMS JTAG port setup time	3	—	ns
t_{JPH}	JTAG port hold time	5	—	ns
t_{JPCO}	JTAG port clock to output	—	11	ns
t_{JPZX}	JTAG port high impedance to valid output	—	14	ns
t_{JPXZ}	JTAG port valid output to high impedance	—	14	ns

FPP Configuration Timing

DCLK-to-DATA[] Ratio (r) for FPP Configuration

Fast passive parallel (FPP) configuration requires a different DCLK-to-DATA[] ratio when you turn on encryption or the compression feature.

Depending on the DCLK-to-DATA[] ratio, the host must send a DCLK frequency that is *r* times the DATA[] rate in byte per second (Bps) or word per second (Wps). For example, in FPP ×16 where the *r* is 2, the DCLK frequency must be 2 times the DATA[] rate in Wps.

(69) The minimum TCK clock period is 167 ns if V_{CCBAT} is within the range 1.2 V – 1.5 V when you perform the volatile key programming.

Symbol	Parameter	Minimum	Maximum	Unit
t_{CF2CK} (72)	nCONFIG high to first rising edge on DCLK	3,010	—	µs
t_{ST2CK} (72)	nSTATUS high to first rising edge of DCLK	10	—	µs
t_{DSU}	DATA[] setup time before rising edge on DCLK	5.5	—	ns
t_{DH}	DATA[] hold time after rising edge on DCLK	0	—	ns
t_{CH}	DCLK high time	0.45 × 1/f_{MAX}	—	s
t_{CL}	DCLK low time	0.45 × 1/f_{MAX}	—	s
t_{CLK}	DCLK period	1/f_{MAX}	—	s
f_{MAX}	DCLK frequency (FPP ×8/×16/×32)	—	100	MHz
t_{CD2UM}	CONF_DONE high to user mode (73)	175	830	µs
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period	—	—
t_{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t_{CD2CU} + (600 × CLKUSR period)	—	—

Related Information

FPP Configuration Timing
Provides the FPP configuration timing waveforms.

(71) This value is applicable if you do not delay configuration by externally holding the nSTATUS low.

(72) If nSTATUS is monitored, follow the t_{ST2CK} specification. If nSTATUS is not monitored, follow the t_{CF2CK} specification.

(73) The minimum and maximum numbers apply only if you chose the internal oscillator as the clock source for initializing the device.

FPP Configuration Timing when DCLK-to-DATA[] >1

Table 49. FPP Timing Parameters When the DCLK-to-DATA[] Ratio is >1 for Intel Cyclone 10 GX Devices

Use these timing parameters when you use the decompression and design security features.

Symbol	Parameter	Minimum	Maximum	Unit
t_{CF2CD}	nCONFIG low to CONF_DONE low	480	1,440	ns
t_{CF2ST0}	nCONFIG low to nSTATUS low	320	960	ns
t_{CFG}	nCONFIG low pulse width	2	—	µs
t_{STATUS}	nSTATUS low pulse width	268	3,000 (74)	µs
t_{CF2ST1}	nCONFIG high to nSTATUS high	—	3,000 (74)	µs
t_{CF2CK} (75)	nCONFIG high to first rising edge on DCLK	3,010	—	µs
t_{ST2CK} (75)	nSTATUS high to first rising edge of DCLK	10	—	µs
t_{DSU}	DATA[] setup time before rising edge on DCLK	5.5	—	ns
t_{DH}	DATA[] hold time after rising edge on DCLK	$N–1/f_{DCLK}$ (76)	—	s
t_{CH}	DCLK high time	$0.45 \times 1/f_{MAX}$	—	s
t_{CL}	DCLK low time	$0.45 \times 1/f_{MAX}$	—	s
t_{CLK}	DCLK period	$1/f_{MAX}$	—	s
f_{MAX}	DCLK frequency (FPP ×8/×16/×32)	—	100	MHz
t_R	Input rise time	—	40	ns
t_F	Input fall time	—	40	ns

continued...

(74) You can obtain this value if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.

(75) If nSTATUS is monitored, follow the t_{ST2CK} specification. If nSTATUS is not monitored, follow the t_{CF2CK} specification.

(76) *N* is the DCLK-to-DATA ratio and f_{DCLK} is the DCLK frequency the system is operating.

Table 54. Configuration Bit Stream Sizes for Intel Cyclone 10 GX Devices

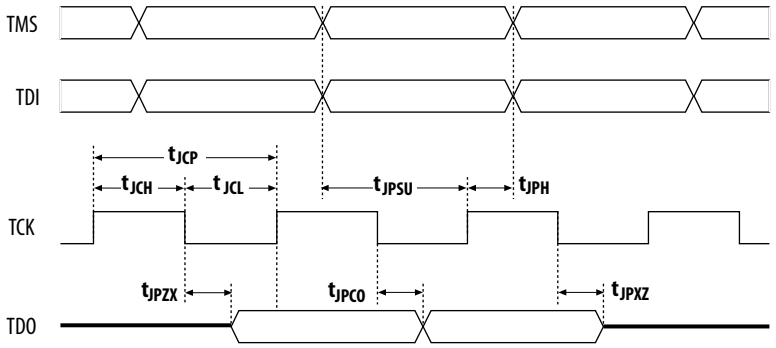
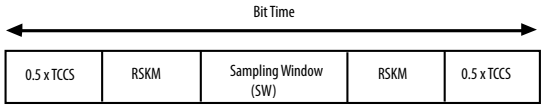
Use this table to estimate the file size before design compilation. Different configuration file formats, such as a hexadecimal file (`.hex`) or tabular text file (`.ttf`) format, have different file sizes.

For the different types of configuration file and file sizes, refer to the Intel Quartus Prime software. However, for a specific version of the Intel Quartus Prime software, any design targeted for the same device has the same uncompressed configuration file size.

I/O configuration shift register (IOCSR) is a long shift register that facilitates the device I/O peripheral settings. The IOCSR bit stream is part of the uncompressed configuration bit stream, and it is specifically for the Configuration via Protocol (CvP) feature.

Uncompressed configuration bit stream sizes are subject to change for improvements and optimizations in the configuration algorithm.

Variant	Product Line	Uncompressed Configuration Bit Stream Size (bits)	IOCSR Bit Stream Size (bits)	Recommended EPCQ-L Serial Configuration Device
Intel Cyclone 10 GX	GX 085	81,923,582	2,507,264	EPCQ-L256 or higher density
	GX 105	81,923,582	2,507,264	EPCQ-L256 or higher density
	GX 150	81,923,582	2,507,264	EPCQ-L256 or higher density
	GX 220	81,923,582	2,507,264	EPCQ-L256 or higher density

Term	Definition
	
R_L	Receiver differential input discrete resistor (external to the Intel Cyclone 10 GX device).
Sampling window (SW)	Timing Diagram—the period of time during which the data must be valid in order to capture it correctly. The setup and hold times determine the ideal strobe position in the sampling window, as shown: 
Single-ended voltage referenced I/O standard	The JEDEC standard for the SSTL and HSTL I/O defines both the AC and DC input signal values. The AC values indicate the voltage levels at which the receiver must meet its timing specifications. The DC values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. After the receiver input has crossed the AC value, the receiver changes to the new logic state. The new logic state is then maintained as long as the input stays beyond the DC threshold. This approach is intended to provide predictable receiver timing in the presence of input waveform ringing. Single-Ended Voltage Referenced I/O Standard

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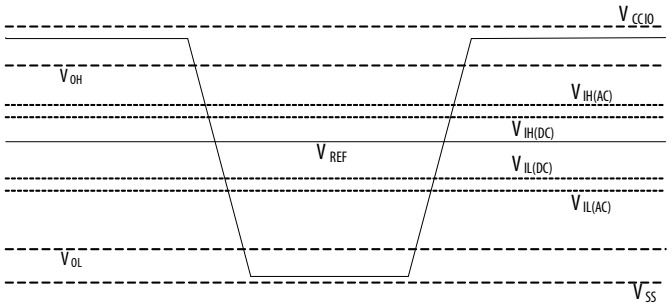
Term	Definition
	
t_C	High-speed receiver/transmitter input and output clock period.
TCCS (channel-to-channel-skew)	The timing difference between the fastest and slowest output edges, including the t_{CO} variation and clock skew, across channels driven by the same PLL. The clock is included in the TCCS measurement (refer to the Timing Diagram figure under SW in this table).
t_{DUTY}	High-speed I/O block—Duty cycle on high-speed transmitter output clock.
t_{FALL}	Signal high-to-low transition time (80–20%)
t_{INCCJ}	Cycle-to-cycle jitter tolerance on the PLL clock input
t_{OUTPJ_IO}	Period jitter on the GPIO driven by a PLL
t_{OUTPJ_DC}	Period jitter on the dedicated clock output driven by a PLL
t_{RISE}	Signal low-to-high transition time (20–80%)
Timing Unit Interval (TUI)	The timing budget allowed for skew, propagation delays, and the data sampling window. (TUI = 1/(Receiver Input Clock Frequency Multiplication Factor) = t_C/w).
$V_{CM(DC)}$	DC Common mode input voltage.
V_{ICM}	Input Common mode voltage—The common mode of the differential signal at the receiver.
V_{ID}	Input differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the receiver.
$V_{DIF(AC)}$	AC differential input voltage—Minimum AC input differential voltage required for switching.
$V_{DIF(DC)}$	DC differential input voltage— Minimum DC input differential voltage required for switching.
V_{IH}	Voltage input high—The minimum positive voltage applied to the input which is accepted by the device as a logic high.

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Term	Definition
$V_{IH(AC)}$	High-level AC input voltage
$V_{IH(DC)}$	High-level DC input voltage
V_{IL}	Voltage input low—The maximum positive voltage applied to the input which is accepted by the device as a logic low.
$V_{IL(AC)}$	Low-level AC input voltage
$V_{IL(DC)}$	Low-level DC input voltage
V_{OCM}	Output Common mode voltage—The common mode of the differential signal at the transmitter.
V_{OD}	Output differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission line at the transmitter.
V_{SWING}	Differential input voltage
V_{IX}	Input differential cross point voltage
V_{OX}	Output differential cross point voltage
W	High-speed I/O block—Clock Boost Factor

Document Revision History for the Intel Cyclone 10 GX Device Datasheet

Document Version	Changes
2018.06.15	• Added *Intel Cyclone 10 GX Devices Overshoot Duration* figure and description. • Added a link in the *OCT Calibration Accuracy Specifications* section. • Removed *Equation for OCT Variation Without Recalibration*. • Updated the note to CLKUSR in the *Initialization Clock Source Option and the Maximum Frequency for Intel Cyclone 10 GX Devices* table. • Updated the *I/O Timing* section on the I/O timing information generation guidelines. • Updated the description and maximum offset values in the *IOE Programmable Delay for Intel Cyclone 10 GX Devices* table.
2018.04.06	Added notes to I_{OUT} specification in the *Absolute Maximum Ratings for Intel Cyclone 10 GX Devices* table.