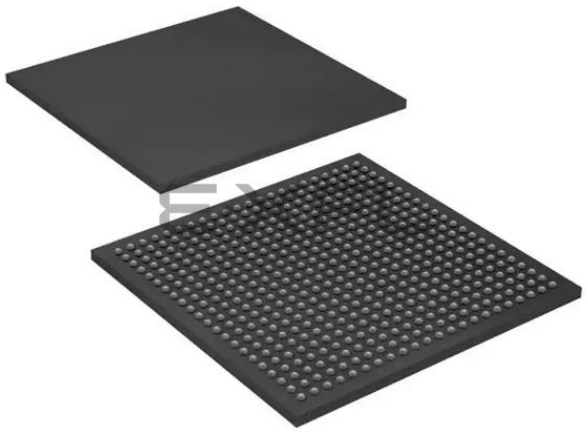

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

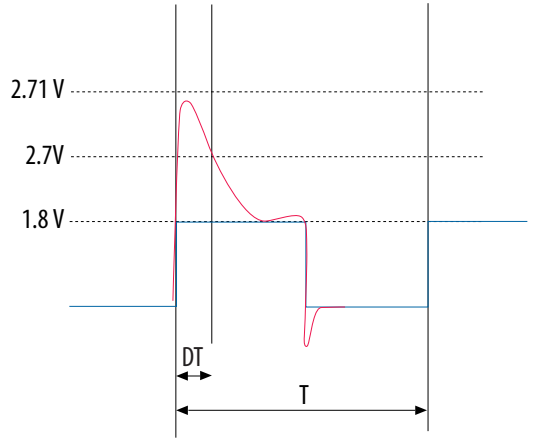
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | 54770 |
| Number of Logic Elements/Cells | 150000 |
| Total RAM Bits | 10907648 |
| Number of I/O | 188 |
| Number of Gates | - |
| Voltage - Supply | 0.9V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 484-BFBGA |
| Supplier Device Package | 484-UBGA (19x19) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/10cx150yu484i6g |

**Figure 1. Intel Cyclone 10 GX Devices Overshoot Duration**




## Recommended Operating Conditions

This section lists the functional operation limits for the AC and DC parameters for Intel Cyclone 10 GX devices.

### Recommended Operating Conditions

**Table 3. Recommended Operating Conditions for Intel Cyclone 10 GX Devices**

This table lists the steady-state voltage values expected from Intel Cyclone 10 GX devices. Power supply ramps must all be strictly monotonic, without plateaus.

| Symbol | Description | Condition | Minimum (8) | Typical | Maximum (8) | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Core voltage power supply | — | 0.87 | 0.9 | 0.93 | V |
| $V_{CCP}$ | Periphery circuitry and transceiver fabric interface power supply | — | 0.87 | 0.9 | 0.93 | V |
| $V_{CCPGM}$ | Configuration pins power supply | 1.8 V | 1.71 | 1.8 | 1.89 | V |
| | | 1.5 V | 1.425 | 1.5 | 1.575 | V |

*continued...*

(8) This value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

### Related Information

- Early Power Estimator User Guide
  Provides more information about power estimation tools.
- Power Analysis and Optimization User Guide: Intel Quartus Prime Pro Edition
  Provides more information about power estimation tools.

## I/O Pin Leakage Current

### Table 5. I/O Pin Leakage Current for Intel Cyclone 10 GX Devices

If $V_O = V_{CCIO}$ to $V_{CCIOMAX}$, 300 µA of leakage current per I/O is expected.

| Symbol | Description | Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| $I_I$ | Input pin | $V_I$ = 0 V to $V_{CCIOMAX}$ | –80 | 80 | µA |
| $I_{OZ}$ | Tri-stated I/O pin | $V_O$ = 0 V to $V_{CCIOMAX}$ | –80 | 80 | µA |

## Bus Hold Specifications

The bus-hold trip points are based on calculated input voltages from the JEDEC standard.

### Table 6. Bus Hold Parameters for Intel Cyclone 10 GX Devices

| Parameter | Symbol | Condition | $V_{CCIO}$ (V) | | | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 1.2 | | 1.5 | | 1.8 | | 2.5 | | 3.0 | | |
| | | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| Bus-hold, low, sustaining current | $I_{SUSL}$ | $V_{IN} > V_{IL}$ (max) | 8 (15), 26 (16) | — | 12 (15), 32 (16) | — | 30 (15), 55 (16) | — | 60 | — | 70 | — | µA |
| Bus-hold, high, sustaining current | $I_{SUSH}$ | $V_{IN} < V_{IH}$ (min) | –8 (15), –26 (16) | — | –12 (15), –32 (16) | — | –30 (15), –55 (16) | — | –60 | — | –70 | — | µA |

*continued...*

(15) This value is only applicable for LVDS I/O bank.

(16) This value is only applicable for 3 V I/O bank.

| Parameter | Symbol | Condition | $V_{CCIO}$ (V) | | | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 1.2 | | 1.5 | | 1.8 | | 2.5 | | 3.0 | | |
| | | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| Bus-hold, low, overdrive current | $I_{ODL}$ | 0 V < $V_{IN}$ < $V_{CCIO}$ | — | 125 | — | 175 | — | 200 | — | 300 | — | 500 | µA |
| Bus-hold, high, overdrive current | $I_{ODH}$ | 0 V < $V_{IN}$ < $V_{CCIO}$ | — | –125 | — | –175 | — | –200 | — | –300 | — | –500 | µA |
| Bus-hold trip point | $V_{TRIP}$ | — | 0.3 | 0.9 | 0.38 | 1.13 | 0.68 | 1.07 | 0.70 | 1.7 | 0.8 | 2 | V |

## OCT Calibration Accuracy Specifications

If you enable on-chip termination (OCT) calibration, calibration is automatically performed at power up for I/Os connected to the calibration block.

### Table 7. OCT Calibration Accuracy Specifications for Intel Cyclone 10 GX Devices

Calibration accuracy for the calibrated on-chip series termination ($R_S$ OCT) and on-chip parallel termination ($R_T$ OCT) are applicable at the moment of calibration. When process, voltage, and temperature (PVT) conditions change after calibration, the tolerance may change.

| Symbol | Description | Condition (V) | Resistance Tolerance | | Unit |
|---|---|---|---|---|---|
| | | | –E5, –I5 | –E6, –I6 | |
| 25-Ω and 50-Ω $R_S$ | Internal series termination with calibration (25-Ω and 50-Ω setting) | $V_{CCIO}$ = 1.8, 1.5, 1.2 | ± 15 | ± 15 | % |
| 34-Ω and 40-Ω $R_S$ | Internal series termination with calibration (34-Ω and 40-Ω setting) | $V_{CCIO}$ = 1.5, 1.25, 1.2 | ± 15 | ± 15 | % |
| | | $V_{CCIO}$ = 1.35 | ± 20 | ± 20 | % |
| 48-Ω, 60-Ω, 80-Ω, and 120-Ω $R_S$ | Internal series termination with calibration (48-Ω, 60-Ω, 80-Ω, and 120-Ω setting) | $V_{CCIO}$ = 1.2 | ± 15 | ± 15 | % |
| 240-Ω $R_S$ | Internal series termination with calibration (240-Ω setting) | $V_{CCIO}$ = 1.2 | ± 20 | ± 20 | % |
| 30-Ω $R_T$ | Internal parallel termination with calibration (30-Ω setting) | $V_{CCIO}$ = 1.5, 1.35, 1.25 | –10 to +40 | –10 to +40 | % |
| 34-Ω, 48-Ω, 80-Ω, and 240-Ω $R_T$ | Internal parallel termination with calibration (34-Ω, 48-Ω, 80-Ω, and 240-Ω setting) | $V_{CCIO}$ = 1.2 | ± 15 | ± 15 | % |

*continued...*

**Table 11. Internal Weak Pull-Down Resistor Values for Intel Cyclone 10 GX Devices**

| Pin Name | Description | Condition (V) | Value (19) | Unit |
|---|---|---|---|---|
| nIO_PULLUP | Dedicated input pin that determines the internal pull-ups on user I/O pins and dual-purpose I/O pins. | $V_{CC}$ = 0.9 ±3.33% | 25 | kΩ |
| TCK | Dedicated JTAG test clock input pin. | $V_{CCPGM}$ = 1.8 ±5 % | 25 | kΩ |
| | | $V_{CCPGM}$ = 1.5 ±5% | 25 | kΩ |
| | | $V_{CCPGM}$ = 1.2 ±5% | 25 | kΩ |
| MSEL[0:2] | Configuration input pins that set the configuration scheme for the FPGA device. | $V_{CCPGM}$ = 1.8 ±5% | 25 | kΩ |
| | | $V_{CCPGM}$ = 1.5 ±5% | 25 | kΩ |
| | | $V_{CCPGM}$ = 1.2 ±5% | 25 | kΩ |

### Related Information

Intel Cyclone 10 GX Device Family Pin Connection Guidelines
Provides more information about the pins that support internal weak pull-up and internal weak pull-down features.

## I/O Standard Specifications

Tables in this section list the input voltage ($V_{IH}$ and $V_{IL}$), output voltage ($V_{OH}$ and $V_{OL}$), and current drive characteristics ($I_{OH}$ and $I_{OL}$) for various I/O standards supported by Intel Cyclone 10 GX devices.

For minimum voltage values, use the minimum $V_{CCIO}$ values. For maximum voltage values, use the maximum $V_{CCIO}$ values.

You must perform timing closure analysis to determine the maximum achievable frequency for general purpose I/O standards.

### Related Information

Recommended Operating Conditions on page 7

| I/O Standard | $V_{IL(DC)}$ (V) | | $V_{IH(DC)}$ (V) | | $V_{IL(AC)}$ (V) | $V_{IH(AC)}$ (V) | $V_{OL}$ (V) | $V_{OH}$ (V) | $I_{OL}$ (21) (mA) | $I_{OH}$ (21) (mA) |
|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Max | Min | Max | Min | | |
| SSTL-12/ SSTL-12 Class I, II | — | $V_{REF}$ – 0.10 | $V_{REF}$ + 0.10 | — | $V_{REF}$ – 0.15 | $V_{REF}$ + 0.15 | 0.2 × $V_{CCIO}$ | 0.8 × $V_{CCIO}$ | — | — |
| HSTL-18 Class I | — | $V_{REF}$ –0.1 | $V_{REF}$ + 0.1 | — | $V_{REF}$ – 0.2 | $V_{REF}$ + 0.2 | 0.4 | $V_{CCIO}$ – 0.4 | 8 | –8 |
| HSTL-18 Class II | — | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | — | $V_{REF}$ – 0.2 | $V_{REF}$ + 0.2 | 0.4 | $V_{CCIO}$ – 0.4 | 16 | –16 |
| HSTL-15 Class I | — | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | — | $V_{REF}$ – 0.2 | $V_{REF}$ + 0.2 | 0.4 | $V_{CCIO}$ – 0.4 | 8 | –8 |
| HSTL-15 Class II | — | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | — | $V_{REF}$ – 0.2 | $V_{REF}$ + 0.2 | 0.4 | $V_{CCIO}$ –0.4 | 16 | –16 |
| HSTL-12 Class I | –0.15 | $V_{REF}$ – 0.08 | $V_{REF}$ + 0.08 | $V_{CCIO}$ + 0.15 | $V_{REF}$ – 0.15 | $V_{REF}$ + 0.15 | 0.25 × $V_{CCIO}$ | 0.75 × $V_{CCIO}$ | 8 | –8 |
| HSTL-12 Class II | –0.15 | $V_{REF}$ – 0.08 | $V_{REF}$ + 0.08 | $V_{CCIO}$ + 0.15 | $V_{REF}$ – 0.15 | $V_{REF}$ + 0.15 | 0.25 × $V_{CCIO}$ | 0.75 × $V_{CCIO}$ | 16 | –16 |
| HSUL-12 | — | $V_{REF}$ – 0.13 | $V_{REF}$ + 0.13 | — | $V_{REF}$ – 0.22 | $V_{REF}$ + 0.22 | 0.1 × $V_{CCIO}$ | 0.9 × $V_{CCIO}$ | — | — |
| POD12 | –0.15 | $V_{REF}$ – 0.08 | $V_{REF}$ + 0.08 | $V_{CCIO}$ + 0.15 | $V_{REF}$ – 0.15 | $V_{REF}$ + 0.15 | (0.7 – 0.15) × $V_{CCIO}$ | (0.7 + 0.15) × $V_{CCIO}$ | — | — |

## Differential SSTL I/O Standards Specifications

### Table 15. Differential SSTL I/O Standards Specifications for Intel Cyclone 10 GX Devices

| I/O Standard | $V_{CCIO}$ (V) | | | $V_{SWING(DC)}$ (V) | | $V_{SWING(AC)}$ (V) | | $V_{IX(AC)}$ (V) | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Max | Min | Max | Min | Typ | Max |
| SSTL-18 Class I, II | 1.71 | 1.8 | 1.89 | 0.25 | $V_{CCIO}$ + 0.6 | 0.5 | $V_{CCIO}$ + 0.6 | $V_{CCIO}/2$ – 0.175 | — | $V_{CCIO}/2$ + 0.175 |
| SSTL-15 Class I, II | 1.425 | 1.5 | 1.575 | 0.2 | (22) | $2(V_{IH(AC)} – V_{REF})$ | $2(V_{REF} – V_{IL(AC)})$ | $V_{CCIO}/2$ – 0.15 | — | $V_{CCIO}/2$ + 0.15 |

*continued...*

(21) To meet the $I_{OL}$ and $I_{OH}$ specifications, you must set the current strength settings accordingly. For example, to meet the SSTL15CI specification (8 mA), you should set the current strength settings to 8 mA. Setting at lower current strength may not meet the $I_{OL}$ and $I_{OH}$ specifications in the datasheet.

# Switching Characteristics

This section provides the performance characteristics of Intel Cyclone 10 GX core and periphery blocks for extended grade devices.

## Transceiver Performance Specifications

### Transceiver Performance for Intel Cyclone 10 GX Devices

#### Table 18. Transmitter and Receiver Data Rate Performance

| Symbol/Description | Condition | Datarate | Unit |
|---|---|---|---|
| Chip-to-Chip (29) | Maximum data rate<br>$V_{CCR\_GXB}$ = $V_{CCT\_GXB}$ = 1.03 V | 12.5 | Gbps |
| | Maximum data rate<br>$V_{CCR\_GXB}$ = $V_{CCT\_GXB}$ = 0.95 V | 11.3 | Gbps |
| | Minimum Data Rate | 1.0 (30) | Gbps |
| Backplane | Maximum data rate<br>$V_{CCR\_GXB}$ = $V_{CCT\_GXB}$ = 1.03 V | 6.6 | Gbps |
| | Minimum Data Rate | 1.0 (30) | Gbps |

#### Table 19. ATX PLL and Fractional PLL (fPLL) Performance

| Symbol/Description | Condition | Frequency | Unit |
|---|---|---|---|
| Supported Output Frequency | Maximum Frequency | 6.25 | GHz |
| | Minimum Frequency | 500 | MHz |

(29) Chip-to-chip links are applications with short reach channels.

(30) Intel Cyclone 10 GX transceivers can support data rates down to 125 Mbps with over sampling. You must create your own over sampling logic.

### Table 20. CMU PLL Performance

| Symbol/Description | Condition | Frequency | Unit |
|---|---|---|---|
| Supported Output Frequency | Maximum Frequency | 5.15625 | GHz |
| | Minimum Frequency | 2450 | MHz |

#### Related Information

Transceiver Power Supply Operating Conditions on page 9

## High-Speed Serial Transceiver-Fabric Interface Performance for Intel Cyclone 10 GX Devices

### Table 21. High-Speed Serial Transceiver-Fabric Interface Performance for Intel Cyclone 10 GX Devices

The frequencies listed are the maximum frequencies.

| Symbol/Description | Condition (V) | Core Speed Grade | | Unit |
|---|---|---|---|---|
| | | -5 | -6 | |
| 20-bit interface - FIFO | $V_{CC}$ = 0.9 | 400 | 400 | MHz |
| 20-bit interface - Registered | $V_{CC}$ = 0.9 | 400 | 400 | MHz |
| 32-bit interface - FIFO | $V_{CC}$ = 0.9 | 404 | 335 | MHz |
| 32-bit interface - Registered | $V_{CC}$ = 0.9 | 404 | 335 | MHz |
| 64-bit interface - FIFO | $V_{CC}$ = 0.9 | 234 | 222 | MHz |
| 64-bit interface - Registered | $V_{CC}$ = 0.9 | 234 | 222 | MHz |

## Transceiver Specifications for Intel Cyclone 10 GX Devices

### Table 22. Reference Clock Specifications

| Symbol/Description | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Supported I/O Standards | Dedicated reference clock pin | CML, Differential LVPECL, LVDS, and HCSL (31) | | | |
| | RX pin as a reference clock | CML, Differential LVPECL, and LVDS | | | |

continued...

(31) HCSL is only supported for PCIe.

| Symbol/Description | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| | 100-Ω setting | — | 100 ± 20% | — | Ω |
| $V_{OCM}$ (AC coupled) | $V_{CCT\_GXB}$ = 0.95 V | — | 450 | — | mV |
| | $V_{CCT\_GXB}$ = 1.03 V | — | 500 | — | mV |
| $V_{OCM}$ (DC coupled) | $V_{CCT\_GXB}$ = 0.95 V | — | 450 | — | mV |
| | $V_{CCT\_GXB}$ = 1.03 V | — | 500 | — | mV |
| Rise time (45) | 20% to 80% | 20 | — | 130 | ps |
| Fall time (45) | 80% to 20% | 20 | — | 130 | ps |
| Intra-differential pair skew | TX $V_{CM}$ = 0.5 V and slew rate setting of SLEW_R5 (46) | — | — | 15 | ps |

## Table 27. Typical Transmitter $V_{OD}$ Settings

| Symbol | $V_{OD}$ Setting | $V_{OD}$-to-$V_{CCT\_GXB}$ Ratio |
|---|---|---|
| $V_{OD}$ differential value = $V_{OD}$-to-$V_{CCT\_GXB}$ ratio x $V_{CCT\_GXB}$ | 31 | 1.00 |
| | 30 | 0.97 |
| | 29 | 0.93 |
| | 28 | 0.90 |
| | 27 | 0.87 |
| | 26 | 0.83 |
| | 25 | 0.80 |
| | 24 | 0.77 |
| | 23 | 0.73 |
| | 22 | 0.70 |

***continued...***

(45) The Intel Quartus Prime software automatically selects the appropriate slew rate depending on the design configurations.

(46) SLEW_R1 is the slowest and SLEW_R5 is the fastest. SLEW_R6 and SLEW_R7 are not used.

| Symbol | $V_{OD}$ Setting | $V_{OD}$-to-$V_{CCT\_GXB}$ Ratio |
|---|---|---|
| | 21 | 0.67 |
| | 20 | 0.63 |
| | 19 | 0.60 |
| | 18 | 0.57 |
| | 17 | 0.53 |
| | 16 | 0.50 |
| | 15 | 0.47 |
| | 14 | 0.43 |
| | 13 | 0.40 |
| | 12 | 0.37 |

**Table 28. Transmitter Channel-to-channel Skew Specifications**

| Mode | Channel Span | Maximum Skew | Unit |
|---|---|---|---|
| x6 Clock | Up to 6 channels in one bank | 61 | ps |
| xN Clock | Within 2 banks | 230 | ps |
| PLL Feedback Compensation (47), (48) | Side-wide | 1600 | ps |

**Related Information**

PLLs and Clock Networks

(47) `refclk` is set to 125 MHz during the test.

(48) You can reduce the lane-to-lane skew by increasing the reference clock frequency.

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{LOCK}$ | Time required to lock from end-of-device configuration or deassertion of `pll_powerdown` | — | — | — | 1 | ms |
| $t_{DLOCK}$ | Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays) | — | — | — | 1 | ms |
| $f_{CLBW}$ | PLL closed-loop bandwidth | — | 0.3 | — | 4 | MHz |
| $t_{PLL\_PSERR}$ | Accuracy of PLL phase shift | — | — | — | 50 | ps |
| $t_{ARESET}$ | Minimum pulse width on the `pll_powerdown` signal | — | 10 | — | — | ns |
| $t_{INCCJ}$ (50)(51) | Input clock cycle-to-cycle jitter | $F_{REF} \geq 100$ MHz | — | — | 0.13 | UI (p-p) |
| | | $F_{REF} < 100$ MHz | — | — | 650 | ps (p-p) |
| $t_{OUTPJ}$ (52) | Period jitter for clock output | $F_{OUT} \geq 100$ MHz | — | — | 600 | ps (p-p) |
| | | $F_{OUT} < 100$ MHz | — | — | 60 | mUI (p-p) |
| $t_{OUTCCJ}$ (52) | Cycle-to-cycle jitter for clock output | $F_{OUT} \geq 100$ MHz | — | — | 600 | ps (p-p) |
| | | $F_{OUT} < 100$ MHz | — | — | 60 | mUI (p-p) |
| $dK_{BIT}$ | Bit number of Delta Sigma Modulator (DSM) | — | — | 32 | — | bit |

## Related Information

Memory Output Clock Jitter Specifications on page 43
Provides more information about the external memory interface clock output jitter specifications.

(50) A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source with jitter < 120 ps.

(51) $F_{REF}$ is $f_{IN}/N$, specification applies when $N = 1$.

(52) External memory interface clock output jitter specifications use a different measurement method, which are available in Memory Output Clock Jitter Specification for Intel Cyclone 10 GX Devices table.

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{DLOCK}$ | Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays) | — | — | — | 1 | ms |
| $t_{PLL\_PSERR}$ | Accuracy of PLL phase shift | — | — | — | ±50 | ps |
| $t_{ARESET}$ | Minimum pulse width on the areset signal | — | 10 | — | — | ns |
| $t_{INCCJ}$ (54)(55) | Input clock cycle-to-cycle jitter | $F_{REF}$ ≥ 100 MHz | — | — | 0.15 | UI (p-p) |
| | | $F_{REF}$ < 100 MHz | — | — | 750 | ps (p-p) |
| $t_{OUTPJ\_DC}$ | Period jitter for dedicated clock output | $F_{OUT}$ ≥ 100 MHz | — | — | 175 | ps (p-p) |
| | | $F_{OUT}$ < 100 MHz | — | — | 17.5 | mUI (p-p) |
| $t_{OUTCCJ\_DC}$ | Cycle-to-cycle jitter for dedicated clock output | $F_{OUT}$ ≥ 100 MHz | — | — | 175 | ps (p-p) |
| | | $F_{OUT}$ < 100 MHz | — | — | 17.5 | mUI (p-p) |
| $t_{OUTPJ\_IO}$ (56) | Period jitter for clock output on the regular I/O | $F_{OUT}$ ≥ 100 MHz | — | — | 600 | ps (p-p) |
| | | $F_{OUT}$ < 100 MHz | — | — | 60 | mUI (p-p) |
| $t_{OUTCCJ\_IO}$ (56) | Cycle-to-cycle jitter for clock output on the regular I/O | $F_{OUT}$ ≥ 100 MHz | — | — | 600 | ps (p-p) |
| | | $F_{OUT}$ < 100 MHz | — | — | 60 | mUI (p-p) |
| $t_{CASC\_OUTPJ\_DC}$ | Period jitter for dedicated clock output in cascaded PLLs | $F_{OUT}$ ≥ 100 MHz | — | — | 175 | ps (p-p) |
| | | $F_{OUT}$ < 100 MHz | — | — | 17.5 | mUI (p-p) |

### Related Information

Memory Output Clock Jitter Specifications on page 43
Provides more information about the external memory interface clock output jitter specifications.

(54) A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source with jitter < 120 ps.

(55) $F_{REF}$ is $f_{IN}/N$, specification applies when $N = 1$.

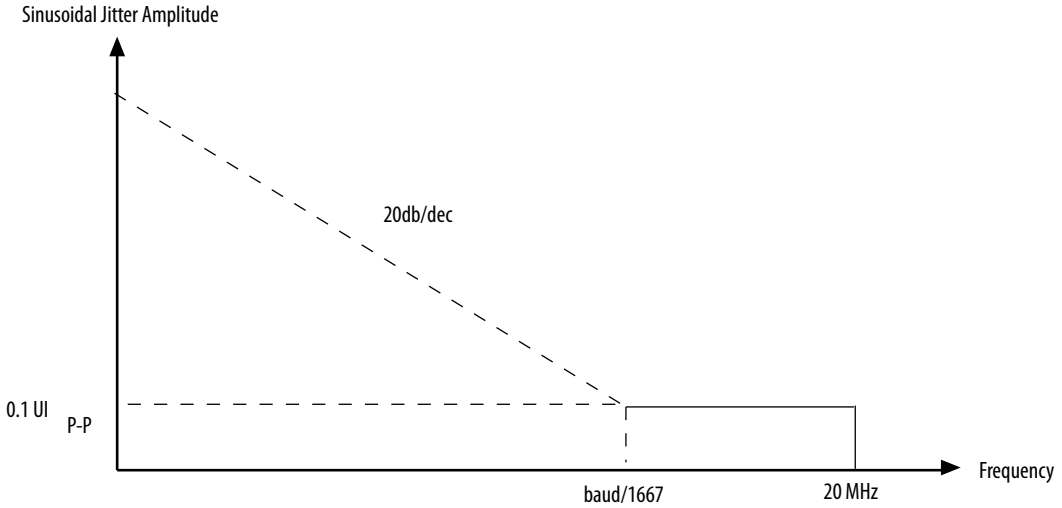
(56) External memory interface clock output jitter specifications use a different measurement method, which are available in Memory Output Clock Jitter Specification for Intel Cyclone 10 GX Devices table.

| Symbol | | Condition | –E5, –I5 | | | –E6, –I6 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | |
| | TCCS (64)(59) | True Differential I/O Standards | — | — | 150 | — | — | 150 | ps |
| Receiver | True Differential I/O Standards - $f_{HSDRDPA}$ (data rate) | SERDES factor J = 4 to 10 (60)(61)(62) | 150 | — | 1434 | 150 | — | 1250 | Mbps |
| | | SERDES factor J = 3 (60)(61)(62) | 150 | — | 1076 | 150 | — | 938 | Mbps |
| | $f_{HSDR}$ (data rate) (without DPA) (59) | SERDES factor J = 3 to 10 | (62) | — | (66) | (62) | — | (66) | Mbps |
| | | SERDES factor J = 2, uses DDR registers | (62) | — | (63) | (62) | — | (63) | Mbps |
| | | SERDES factor J = 1, uses DDR registers | (62) | — | (63) | (62) | — | (63) | Mbps |
| DPA (FIFO mode) | DPA run length | — | — | — | 10000 | — | — | 10000 | UI |
| DPA (soft CDR mode) | DPA run length | SGMII/GbE protocol | — | — | 5 | — | — | 5 | UI |
| | | All other protocols | — | — | 50 data transition per 208 UI | — | — | 50 data transition per 208 UI | — |
| Soft CDR mode | Soft-CDR ppm tolerance | — | — | — | 300 | — | — | 300 | ± ppm |
| Non DPA mode | Sampling Window | — | — | — | 300 | — | — | 300 | ps |

(65) This applies to default pre-emphasis and $V_{OD}$ settings only.

(66) You can estimate the achievable maximum data rate for non-DPA mode by performing link timing closure analysis. You must consider the board skew margin, transmitter delay margin, and receiver sampling margin to determine the maximum data rate supported.

**Figure 4. LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specifications for a Data Rate Less than 1.4 Gbps**




## Memory Standards Supported by the Hard Memory Controller

**Table 40. Memory Standards Supported by the Hard Memory Controller for Intel Cyclone 10 GX Devices**

This table lists the overall capability of the hard memory controller. For specific details, refer to the External Memory Interface Spec Estimator.

| Memory Standard | Rate Support | Speed Grade | Ping Pong PHY Support | Maximum Frequency (MHz) | |
|---|---|---|---|---|---|
| | | | | I/O Bank | 3 V I/O Bank |
| DDR3 SDRAM | Half rate | –5 | Yes | 533 | 225 |
| | | | — | 533 | 225 |
| | | –6 | Yes | 466 | 166 |
| | | | — | 466 | 166 |
| | Quarter rate | –5 | Yes | 933 | 450 |
| | | | — | 933 | 450 |
| | | –6 | Yes | 933 | 333 |

*continued...*

### Table 47. DCLK-to-DATA[] Ratio for Intel Cyclone 10 GX Devices

You cannot turn on encryption and compression at the same time for Intel Cyclone 10 GX devices.

| Configuration Scheme | Encryption | Compression | DCLK-to-DATA[] Ratio (r) |
|---|---|---|---|
| FPP (8-bit wide) | Off | Off | 1 |
| | On | Off | 1 |
| | Off | On | 2 |
| FPP (16-bit wide) | Off | Off | 1 |
| | On | Off | 2 |
| | Off | On | 4 |
| FPP (32-bit wide) | Off | Off | 1 |
| | On | Off | 4 |
| | Off | On | 8 |

## FPP Configuration Timing when DCLK-to-DATA[] = 1

*Note:* When you enable decompression or the design security feature, the DCLK-to-DATA[] ratio varies for FPP ×8, FPP ×16, and FPP ×32. For the respective DCLK-to-DATA[] ratio, refer to the DCLK-to-DATA[] Ratio for Intel Cyclone 10 GX Devices table.

### Table 48. FPP Timing Parameters When the DCLK-to-DATA[] Ratio is 1 for Intel Cyclone 10 GX Devices

Use these timing parameters when the decompression and design security features are disabled.

| Symbol | Parameter | Minimum | Maximum | Unit |
|---|---|---|---|---|
| $t_{CF2CD}$ | nCONFIG low to CONF_DONE low | 480 | 1,440 | ns |
| $t_{CF2ST0}$ | nCONFIG low to nSTATUS low | 320 | 960 | ns |
| $t_{CFG}$ | nCONFIG low pulse width | 2 | — | µs |
| $t_{STATUS}$ | nSTATUS low pulse width | 268 | 3,000 (70) | µs |
| $t_{CF2ST1}$ | nCONFIG high to nSTATUS high | — | 3,000 (71) | µs |

*continued...*

(70) This value is applicable if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.

## Initialization

### Table 53. Initialization Clock Source Option and the Maximum Frequency for Intel Cyclone 10 GX Devices

| Initialization Clock Source | Configuration Scheme | Maximum Frequency (MHz) | Minimum Number of Clock Cycles |
|---|---|---|---|
| Internal Oscillator | AS, PS, and FPP | 12.5 | 600 |
| CLKUSR (82)(83) | AS, PS, and FPP | 100 | |

## Configuration Files

There are two types of configuration bit stream formats for different configuration schemes:

- PS and FPP—Raw Binary File (`.rbf`)
- AS—Raw Programming Data File (`.rpd`)

The `.rpd` file size follows the Intel configuration devices capacity. However, the actual configuration bit stream size for `.rpd` file is the same as `.rbf` file.

(82) To enable CLKUSR as the initialization clock source, in the Intel Quartus Prime software, select **Device and Pin Options ➤ General ➤ Device initialization clock source ➤ CLKUSR pin**.

(83) If you use the CLKUSR pin for AS and transceiver calibration simultaneously, the only allowed frequency is 100 MHz.

## Table 54. Configuration Bit Stream Sizes for Intel Cyclone 10 GX Devices

Use this table to estimate the file size before design compilation. Different configuration file formats, such as a hexadecimal file (`.hex`) or tabular text file (`.ttf`) format, have different file sizes.

For the different types of configuration file and file sizes, refer to the Intel Quartus Prime software. However, for a specific version of the Intel Quartus Prime software, any design targeted for the same device has the same uncompressed configuration file size.

I/O configuration shift register (IOCSR) is a long shift register that facilitates the device I/O peripheral settings. The IOCSR bit stream is part of the uncompressed configuration bit stream, and it is specifically for the Configuration via Protocol (CvP) feature.

Uncompressed configuration bit stream sizes are subject to change for improvements and optimizations in the configuration algorithm.

| Variant | Product Line | Uncompressed Configuration Bit Stream Size (bits) | IOCSR Bit Stream Size (bits) | Recommended EPCQ-L Serial Configuration Device |
|---|---|---|---|---|
| Intel Cyclone 10 GX | GX 085 | 81,923,582 | 2,507,264 | EPCQ-L256 or higher density |
| | GX 105 | 81,923,582 | 2,507,264 | EPCQ-L256 or higher density |
| | GX 150 | 81,923,582 | 2,507,264 | EPCQ-L256 or higher density |
| | GX 220 | 81,923,582 | 2,507,264 | EPCQ-L256 or higher density |

## Remote System Upgrades

### Table 56. Remote System Upgrade Circuitry Timing Specifications for Intel Cyclone 10 GX Devices

| Parameter | Minimum | Maximum | Unit |
|---|---|---|---|
| $f_{MAX\_RU\_CLK}$ (86) | — | 40 | MHz |
| $t_{RU\_nCONFIG}$ (87) | 250 | — | ns |
| $t_{RU\_nRSTIMER}$ (88) | 250 | — | ns |

#### Related Information

- Remote System Upgrade State Machine
  Provides more information about configuration reset (RU_CONFIG) signal.
- User Watchdog Timer
  Provides more information about reset_timer (RU_nRSTIMER) signal.

## User Watchdog Internal Circuitry Timing Specifications

### Table 57. User Watchdog Internal Oscillator Frequency Specifications for Intel Cyclone 10 GX Devices

| Parameter | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|
| User watchdog internal oscillator frequency | 5.3 | 7.9 | 12.5 | MHz |

## I/O Timing

I/O timing data is typically used prior to designing the FPGA to get an estimate of the timing budget as part of the timing analysis. You may generate the I/O timing report manually using the Timing Analyzer or using the automated script.

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(86) This clock is user-supplied to the remote system upgrade circuitry. If you are using the Remote Update Intel FPGA IP core, the clock user-supplied to the Remote Update Intel FPGA IP core must meet this specification.

(87) This is equivalent to strobing the reconfiguration input of the Remote Update Intel FPGA IP core high for the minimum timing specification.

(88) This is equivalent to strobing the reset_timer input of the Remote Update Intel FPGA IP core high for the minimum timing specification.

The Intel Quartus Prime Timing Analyzer provides a more accurate and precise I/O timing data based on the specifics of the design after you complete place-and-route.

### Related Information

AN775: I/O Timing Information Generation Guidelines
Provides the techniques to generate I/O timing information using the Intel Quartus Prime software.

## Programmable IOE Delay

### Table 58. IOE Programmable Delay for Intel Cyclone 10 GX Devices

For the exact values for each setting, use the latest version of the Intel Quartus Prime software. The values in the table show the delay of programmable IOE delay chain with maximum offset settings after excluding the intrinsic delay (delay at minimum offset settings).

Programmable IOE delay settings are only applicable for I/O buffers and do not apply for any other delay elements in the PHYLite for Parallel Interfaces Intel Cyclone 10 FPGA IP core.

| Parameter [89] | Maximum Offset | Minimum Offset [90] | Fast Model | | Slow Model | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Extended | Industrial | –E5, –I5 | –E6, –I6 | |
| Input Delay Chain Setting (IO_IN_DLY_CHN) | 63 | 0 | 2.012 | 2.003 | 5.241 | 6.035 | ns |
| Output Delay Chain Setting (IO_OUT_DLY_CHN) | 15 | 0 | 0.478 | 0.475 | 1.263 | 1.462 | ns |

## Glossary

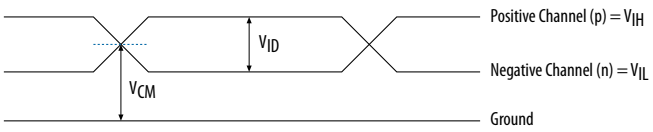
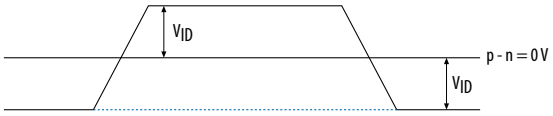
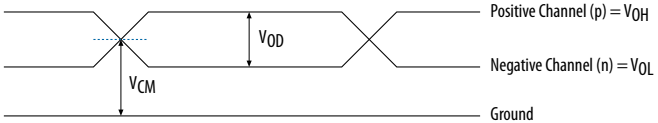
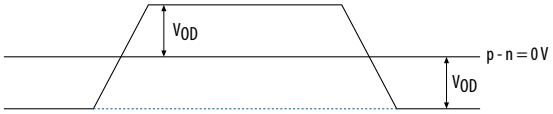
### Table 59. Glossary

| Term | Definition |
|---|---|
| Differential I/O Standards | Receiver Input Waveforms |

*continued...*

(89) You can set this value in the Intel Quartus Prime software by selecting **Input Delay Chain Setting** or **Output Delay Chain Setting** in the **Assignment Name** column.

(90) Minimum offset does not include the intrinsic delay.

| Term | Definition |
|---|---|
| | **Single-Ended Waveform**<br>  <br><br>**Differential Waveform**<br>  <br><br>Transmitter Output Waveforms<br>**Single-Ended Waveform**<br>  <br><br>**Differential Waveform**<br>  <br> |
| $f_{HSCLK}$ | I/O PLL input clock frequency. |
| $f_{HSDR}$ | High-speed I/O block—Maximum/minimum LVDS data transfer rate ($f_{HSDR}$ = 1/TUI), non-DPA. |
| $f_{HSDRDPA}$ | High-speed I/O block—Maximum/minimum LVDS data transfer rate ($f_{HSDRDPA}$ = 1/TUI), DPA. |
| J | High-speed I/O block—Deserialization factor (width of parallel data bus). |
| JTAG Timing Specifications | JTAG Timing Specifications: |

***continued...***

| Date | Version | Changes |
|---|---|---|
| November 2017 | 2017.11.10 | • Changed the full symbol names for $V_{CCR\_GXB}$ and $V_{CCT\_GXB}$, and changed the description for $V_{CCH\_GXB}$ in the *Transceiver Power Supply Operating Conditions for Intel Cyclone 10 GX Devices* table.<br>• Removed note from the *Transceiver Power Supply Operating Conditions* section.<br>• Added a footnote in the *Reference Clock Specifications* table.<br>• Removed the "Programmable AC Gain at High Gain mode and Data Rate ≤ 12.5 Gbps" parameter from the *Receiver Specifications* table.<br>• Changed the channel span descriptions for the x1 and x6 clock networks in the *Transceiver Clock Network Maximum Data Rate Specifications* table.<br>• Changed the description of the VOD ratio in the *Typical Transmitter $V_{OD}$ Settings* table.<br>• Changed the specifications for CDR PPM deviation limit in the *Receiver Specifications* table.<br>• Updated the description for $V_{CCT\_GXB}$, $V_{CCR\_GXB}$, and $V_{CCH\_GXB}$.<br>• Added note to $V_I$ in the *Recommended Operating Conditions for Intel Cyclone 10 GX Devices* table.<br>• Updated notes to RSDS and Mini-LVDS in the *Differential I/O Standards Specifications for Intel Cyclone 10 GX Devices* table.<br>• Updated $f_{VCO}$ specifications in the *Fractional PLL Specifications for Intel Cyclone 10 GX Devices* table.<br>• Updated temperature range from "–40 to 125°C" to "–40 to 100°C" in the *Internal Temperature Sensing Diode Specifications for Intel Cyclone 10 GX Devices* table.<br>• Updated the description for the *Memory Output Clock Jitter Specifications for Intel Cyclone 10 GX Devices* table.<br>• Updated the following IP cores name:<br>— Remote Update Intel FPGA<br>— PHYLite for Parallel Interfaces Intel Cyclone 10 FPGA<br>• Removed automotive-grade information.<br>• Removed Preliminary tags. |
| May 2017 | 2017.05.08 | Initial release. |