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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	80330
Number of Logic Elements/Cells	220000
Total RAM Bits	13752320
Number of I/O	236
Number of Gates	-
Voltage - Supply	0.9V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 100°C (TJ)
Package / Case	672-BBGA, FCBGA
Supplier Device Package	672-FBGA, FC (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/intel/10cx220yf672e5g

Table 1. Absolute Maximum Ratings for Intel Cyclone 10 GX Devices

Symbol	Description	Condition	Minimum	Maximum	Unit
V_{CC}	Core voltage power supply	—	–0.50	1.21	V
V_{CCP}	Periphery circuitry and transceiver fabric interface power supply	—	–0.50	1.21	V
V_{CCERAM}	Embedded memory power supply	—	–0.50	1.36	V
V_{CCPT}	Power supply for programmable power technology and I/O pre-driver	—	–0.50	2.46	V
V_{CCBAT}	Battery back-up power supply for design security volatile key register	—	–0.50	2.46	V
V_{CCPGM}	Configuration pins power supply	(1)	–0.50	2.46	V
V_{CCIO}	I/O buffers power supply	3 V I/O	–0.50	4.10	V
		LVDS I/O	–0.50	2.46	V
V_{CCA_PLL}	Phase-locked loop (PLL) analog power supply	—	–0.50	2.46	V
V_{CCT_GXB}	Transmitter power supply	—	–0.50	1.34	V
V_{CCR_GXB}	Receiver power supply	—	–0.50	1.34	V
V_{CCH_GXB}	Transceiver output buffer power supply	—	–0.50	2.46	V

continued...

(1) The LVDS I/O values are applicable to all dedicated and dual-function configuration I/Os.

Table 2. Maximum Allowed Overshoot During Transitions for Intel Cyclone 10 GX Devices

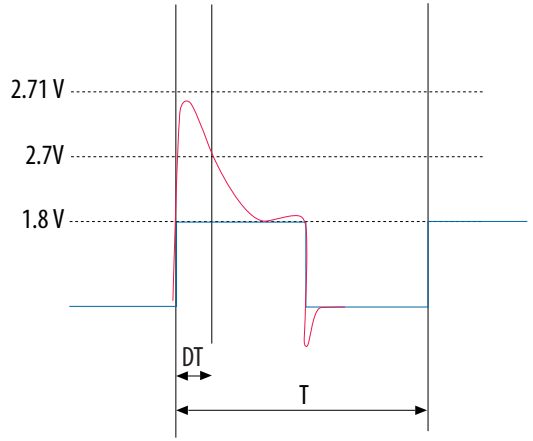
This table lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage of device lifetime. The LVDS I/O values are applicable to the VREFP_ADC and VREFN_ADC I/O pins.

Symbol	Description	Condition (V)		Overshoot Duration as % at T_J = 100°C	Unit
		LVDS I/O (7)	3 V I/O		
V_i (AC)	AC input voltage	2.50	3.80	100	%
		2.55	3.85	42	%
		2.60	3.90	18	%
		2.65	3.95	9	%
		2.70	4.00	4	%
		> 2.70	> 4.00	No overshoot allowed	%

For an overshoot of 2.5 V, the percentage of high time for the overshoot can be as high as 100% over a 10-year period. Percentage of high time is calculated as ([delta T]/T) × 100. This 10-year period assumes that the device is always turned on with 100% I/O toggle rate and 50% duty cycle signal.

(7) The LVDS I/O values are applicable to all dedicated and dual-function configuration I/Os.

Figure 1. Intel Cyclone 10 GX Devices Overshoot Duration



Recommended Operating Conditions

This section lists the functional operation limits for the AC and DC parameters for Intel Cyclone 10 GX devices.

Recommended Operating Conditions

Table 3. Recommended Operating Conditions for Intel Cyclone 10 GX Devices

This table lists the steady-state voltage values expected from Intel Cyclone 10 GX devices. Power supply ramps must all be strictly monotonic, without plateaus.

Symbol	Description	Condition	Minimum (8)	Typical	Maximum (8)	Unit
V_{CC}	Core voltage power supply	—	0.87	0.9	0.93	V
V_{CCP}	Periphery circuitry and transceiver fabric interface power supply	—	0.87	0.9	0.93	V
V_{CCPGM}	Configuration pins power supply	1.8 V	1.71	1.8	1.89	V
		1.5 V	1.425	1.5	1.575	V

continued...

(8) This value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

Symbol	Description	Condition	Minimum [8]	Typical	Maximum [8]	Unit
		1.2 V	1.14	1.2	1.26	V
V_{CCERAM}	Embedded memory power supply	0.9 V	0.87	0.9	0.93	V
V_{CCBAT} [9]	Battery back-up power supply (For design security volatile key register)	1.8 V	1.71	1.8	1.89	V
		1.2 V	1.14	1.2	1.26	V
V_{CCPT}	Power supply for programmable power technology and I/O pre-driver	1.8 V	1.71	1.8	1.89	V
V_{CCIO}	I/O buffers power supply	3.0 V (for 3 V I/O only)	2.85	3.0	3.15	V
		2.5 V (for 3 V I/O only)	2.375	2.5	2.625	V
		1.8 V	1.71	1.8	1.89	V
		1.5 V	1.425	1.5	1.575	V
		1.35 V	(10)	1.35	(10)	V
		1.25 V	1.19	1.25	1.31	V
		1.2 V	(10)	1.2	(10)	V
V_{CCA_PLL}	PLL analog voltage regulator power supply	—	1.71	1.8	1.89	V
V_{REFP_ADC}	Precision voltage reference for voltage sensor	—	1.2475	1.25	1.2525	V

continued...

(8) This value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

(9) If you do not use the design security feature in Intel Cyclone 10 GX devices, connect V_{CCBAT} to a 1.5-V to 1.8-V power supply. Intel Cyclone 10 GX power-on reset (POR) circuitry monitors V_{CCBAT}. Intel Cyclone 10 GX devices do not exit POR if V_{CCBAT} is not powered up.

(10) For minimum and maximum voltage values, refer to the I/O Standard Specifications section.

Symbol	Description	Condition	Minimum (8)	Typical	Maximum (8)	Unit
V_I (11)(12)	DC input voltage	3 V I/O	–0.3	—	3.3	V
		LVDS I/O	–0.3	—	2.19	V
V_O	Output voltage	—	0	—	V_{CCIO}	V
T_J	Operating junction temperature	Extended	0	—	100	°C
		Industrial	–40	—	100	°C
t_{RAMP} (13)	Power supply ramp time	Standard POR	200 µs	—	100 ms	—
		Fast POR	200 µs	—	4 ms	—

Related Information

I/O Standard Specifications on page 15

Transceiver Power Supply Operating Conditions

Table 4. Transceiver Power Supply Operating Conditions for Intel Cyclone 10 GX Devices

Symbol	Description	Condition	Minimum (14)	Typical	Maximum (14)	Unit
$V_{CCT\_GXB[L1][C,D]}$	Transmitter power supply	Chip-to-chip ≤ 12.5 Gbps Or	1.0	1.03	1.06	V

continued...

(8) This value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

(11) The LVDS I/O values are applicable to all dedicated and dual-function configuration I/Os.

(12) This value applies to both input and tri-stated output configuration. Pin voltage should not be externally pulled higher than the maximum value.

(13) t_{ramp} is the ramp time of each individual power supply, not the ramp time of all combined power supplies.

(14) This value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

Single-Ended I/O Standards Specifications

Table 12. Single-Ended I/O Standards Specifications for Intel Cyclone 10 GX Devices

I/O Standard	V_{CCIO} (V)			V_{IL} (V)		V_{IH} (V)		V_{OL} (V)	V_{OH} (V)	I_{OL} (20) (mA)	I_{OH} (20) (mA)
	Min	Typ	Max	Min	Max	Min	Max	Max	Min		
3.0-V LVTTL	2.85	3	3.15	–0.3	0.8	1.7	3.3	0.4	2.4	2	–2
3.0-V LVCMOS	2.85	3	3.15	–0.3	0.8	1.7	3.3	0.2	V_{CCIO} – 0.2	0.1	–0.1
2.5 V	2.375	2.5	2.625	–0.3	0.7	1.7	3.3	0.4	2	1	–1
1.8 V	1.71	1.8	1.89	–0.3	0.35 × V_{CCIO}	0.65 × V_{CCIO}	V_{CCIO} + 0.3	0.45	V_{CCIO} – 0.45	2	–2
1.5 V	1.425	1.5	1.575	–0.3	0.35 × V_{CCIO}	0.65 × V_{CCIO}	V_{CCIO} + 0.3	0.25 × V_{CCIO}	0.75 × V_{CCIO}	2	–2
1.2 V	1.14	1.2	1.26	–0.3	0.35 × V_{CCIO}	0.65 × V_{CCIO}	V_{CCIO} + 0.3	0.25 × V_{CCIO}	0.75 × V_{CCIO}	2	–2

Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications

Table 13. Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications for Intel Cyclone 10 GX Devices

I/O Standard	V_{CCIO} (V)			V_{REF} (V)			V_{TT} (V)		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
SSTL-18 Class I, II	1.71	1.8	1.89	0.833	0.9	0.969	V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04
SSTL-15 Class I, II	1.425	1.5	1.575	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}
SSTL-135/ SSTL-135 Class I, II	1.283	1.35	1.418	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}
SSTL-125/ SSTL-125 Class I, II	1.19	1.25	1.31	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}
SSTL-12/ SSTL-12 Class I, II	1.14	1.2	1.26	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}

continued...

(20) To meet the I_{OL} and I_{OH} specifications, you must set the current strength settings accordingly. For example, to meet the 3.0-V LVTTL specification (2 mA), you should set the current strength settings to 2 mA. Setting at lower current strength may not meet the I_{OL} and I_{OH} specifications in the datasheet.

I/O Standard	V_{CCIO} (V)			V_{REF} (V)			V_{TT} (V)		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
HSTL-18 Class I, II	1.71	1.8	1.89	0.85	0.9	0.95	—	$V_{CCIO}/2$	—
HSTL-15 Class I, II	1.425	1.5	1.575	0.68	0.75	0.9	—	$V_{CCIO}/2$	—
HSTL-12 Class I, II	1.14	1.2	1.26	0.47 × V_{CCIO}	0.5 × V_{CCIO}	0.53 × V_{CCIO}	—	$V_{CCIO}/2$	—
HSUL-12	1.14	1.2	1.3	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}	—	—	—
POD12	1.16	1.2	1.24	0.69 × V_{CCIO}	0.7 × V_{CCIO}	0.71 × V_{CCIO}	—	V_{CCIO}	—

Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications

Table 14. Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications for Intel Cyclone 10 GX Devices

I/O Standard	$V_{IL(DC)}$ (V)		$V_{IH(DC)}$ (V)		$V_{IL(AC)}$ (V)	$V_{IH(AC)}$ (V)	V_{OL} (V)	V_{OH} (V)	I_{OL} (21) (mA)	I_{OH} (21) (mA)
	Min	Max	Min	Max	Max	Min	Max	Min		
SSTL-18 Class I	–0.3	V_{REF} –0.125	V_{REF} + 0.125	V_{CCIO} + 0.3	V_{REF} – 0.25	V_{REF} + 0.25	V_{TT} – 0.603	V_{TT} + 0.603	6.7	–6.7
SSTL-18 Class II	–0.3	V_{REF} –0.125	V_{REF} + 0.125	V_{CCIO} + 0.3	V_{REF} – 0.25	V_{REF} + 0.25	0.28	V_{CCIO} –0.28	13.4	–13.4
SSTL-15 Class I	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.175	V_{REF} + 0.175	0.2 × V_{CCIO}	0.8 × V_{CCIO}	8	–8
SSTL-15 Class II	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.175	V_{REF} + 0.175	0.2 × V_{CCIO}	0.8 × V_{CCIO}	16	–16
SSTL-135/ SSTL-135 Class I, II	—	V_{REF} – 0.09	V_{REF} + 0.09	—	V_{REF} – 0.16	V_{REF} + 0.16	0.2 × V_{CCIO}	0.8 × V_{CCIO}	—	—
SSTL-125/ SSTL-125 Class I, II	—	V_{REF} – 0.09	V_{REF} + 0.09	—	V_{REF} – 0.15	V_{REF} + 0.15	0.2 × V_{CCIO}	0.8 × V_{CCIO}	—	—

continued...

(21) To meet the I_{OL} and I_{OH} specifications, you must set the current strength settings accordingly. For example, to meet the SSTL15CI specification (8 mA), you should set the current strength settings to 8 mA. Setting at lower current strength may not meet the I_{OL} and I_{OH} specifications in the datasheet.

Symbol/Description	Condition	Min	Typ	Max	Unit
t_{LTR} (40)	—	—	—	10	µs
t_{LTD} (41)	—	4	—	—	µs
t_{LTD_manual} (42)	—	4	—	—	µs
$t_{LTR\_LTD\_manual}$ (43)	—	15	—	—	µs
Run Length	—	—	—	200	UI
CDR PPM tolerance	PCIe-only	-300	—	300	PPM
	All other protocols	-1000	—	1000	PPM
Programmable DC Gain	Setting = 0-4	0	—	10	dB
Programmable AC Gain at High Gain mode and Data Rate ≤ 6 Gbps	Setting = 0-28 V_{CCR_GXB} = 0.95 V	0	—	19	dB
	Setting = 0-28 V_{CCR_GXB} = 1.03 V	0	—	21	dB

Table 26. Transmitter Specifications

Symbol/Description	Condition	Min	Typ	Max	Unit
Supported I/O Standards	—	High Speed Differential I/O (44)			—
Differential on-chip termination resistors	85-Ω setting	—	85 ± 20%	—	Ω

continued...

(40) t_{LTR} is the time required for the receive CDR to lock to the input reference clock frequency after coming out of reset.

(41) t_{LTD} is time required for the receiver CDR to start recovering valid data after the `rx_is_lockedtodata` signal goes high.

(42) t_{LTD_manual} is the time required for the receiver CDR to start recovering valid data after the `rx_is_lockedtodata` signal goes high when the CDR is functioning in the manual mode.

(43) $t_{LTR\_LTD\_manual}$ is the time the receiver CDR must be kept in lock to reference (LTR) mode after the `rx_is_lockedtoref` signal goes high when the CDR is functioning in the manual mode.

(44) High Speed Differential I/O is the dedicated I/O standard for the transmitter in Intel Cyclone 10 GX transceivers.

DSP Block Specifications

Table 32. DSP Block Performance Specifications for Intel Cyclone 10 GX Devices

Mode	Performance				Unit
	–E5	–I5	–E6	–I6	
Fixed-point 18 × 19 multiplication mode	456	438	364	346	MHz
Fixed-point 27 × 27 multiplication mode	450	434	358	344	MHz
Fixed-point 18 × 18 multiplier adder mode	459	440	370	351	MHz
Fixed-point 18 × 18 multiplier adder summed with 36-bit input mode	444	422	349	326	MHz
Fixed-point 18 × 19 systolic mode	459	440	370	351	MHz
Complex 18 × 19 multiplication mode	456	438	364	346	MHz
Floating point multiplication mode	447	427	347	326	MHz
Floating point adder or subtract mode	388	369	288	266	MHz
Floating point multiplier adder or subtract mode	386	368	290	270	MHz
Floating point multiplier accumulate mode	418	393	326	294	MHz
Floating point vector one mode	404	382	306	282	MHz
Floating point vector two mode	383	367	293	278	MHz

Memory Block Specifications

To achieve the maximum memory block performance, use a memory block clock that comes through global clock routing from an on-chip PLL and set to **50%** output duty cycle. Use the Intel Quartus Prime software to report timing for the memory block clocking schemes.

When you use the error detection cyclical redundancy check (CRC) feature, there is no degradation in f_{MAX}.

External Temperature Sensing Diode Specifications

Table 35. External Temperature Sensing Diode Specifications for Intel Cyclone 10 GX Devices

- The typical value is at 25°C.
- Diode accuracy improves with lower injection current.
- Absolute accuracy is dependent on third party external diode ADC and integration specifics.

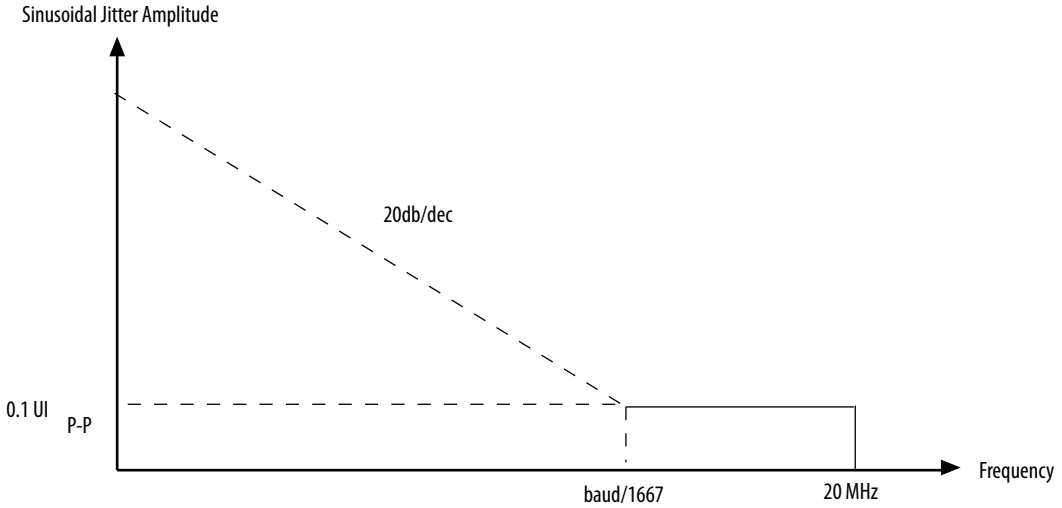
Description	Min	Typ	Max	Unit
I_{bias}, diode source current	10	—	100	µA
V_{bias}, voltage across diode	0.3	—	0.9	V
Series resistance	—	—	< 1	Ω
Diode ideality factor	—	1.03	—	—

Internal Voltage Sensor Specifications

Table 36. Internal Voltage Sensor Specifications for Intel Cyclone 10 GX Devices

Parameter		Minimum	Typical	Maximum	Unit
Resolution		—	—	6	Bit
Sampling rate		—	—	500	Ksps
Differential non-linearity (DNL)		—	—	±1	LSB
Integral non-linearity (INL)		—	—	±1	LSB
Gain error		—	—	±1	%
Offset error		—	—	±1	LSB
Input capacitance		—	20	—	pF
Clock frequency		0.1	—	11	MHz
Unipolar Input Mode	Input signal range for Vsigp	0	—	1.5	V
	Common mode voltage on Vsign	0	—	0.25	V
	Input signal range for Vsigp – Vsign	0	—	1.25	V

Figure 4. LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specifications for a Data Rate Less than 1.4 Gbps



Memory Standards Supported by the Hard Memory Controller

Table 40. Memory Standards Supported by the Hard Memory Controller for Intel Cyclone 10 GX Devices

This table lists the overall capability of the hard memory controller. For specific details, refer to the External Memory Interface Spec Estimator.

Memory Standard	Rate Support	Speed Grade	Ping Pong PHY Support	Maximum Frequency (MHz)	
				I/O Bank	3 V I/O Bank
DDR3 SDRAM	Half rate	–5	Yes	533	225
			—	533	225
		–6	Yes	466	166
			—	466	166
	Quarter rate	–5	Yes	933	450
			—	933	450
		–6	Yes	933	333

continued...

Memory Standard	Rate Support	Speed Grade	Ping Pong PHY Support	Maximum Frequency (MHz)	
				I/O Bank	3 V I/O Bank
			—	933	333
DDR3L SDRAM	Half rate	–5	Yes	533	225
			—	533	225
		–6	Yes	466	166
			—	466	166
	Quarter rate	–5	Yes	933	450
			—	933	450
		–6	Yes	933	333
			—	933	333
LPDDR3 SDRAM	Half rate	–5	—	400	225
		–6	—	333	166
	Quarter rate	–5	—	800	450
		–6	—	666	333

Related Information

External Memory Interface Spec Estimator
Provides the specific details of the memory standards supported.

DLL Range Specifications

Table 41. DLL Frequency Range Specifications for Intel Cyclone 10 GX Devices

Intel Cyclone 10 GX devices support memory interface frequencies lower than 600 MHz, although the reference clock that feeds the DLL must be at least 600 MHz. To support interfaces below 600 MHz, multiply the reference clock feeding the DLL to ensure the frequency is within the supported range.

Parameter	Performance (for All Speed Grades)	Unit
DLL operating frequency range	600 – 1333	MHz

JTAG Configuration Timing

Table 46. JTAG Timing Parameters and Values for Intel Cyclone 10 GX Devices

Symbol	Description	Min	Max	Unit
t_{JCP}	TCK clock period	30, 167 (69)	—	ns
t_{JCH}	TCK clock high time	14	—	ns
t_{JCL}	TCK clock low time	14	—	ns
$t_{JPSU\ (TDI)}$	TDI JTAG port setup time	2	—	ns
$t_{JPSU\ (TMS)}$	TMS JTAG port setup time	3	—	ns
t_{JPH}	JTAG port hold time	5	—	ns
t_{JPCO}	JTAG port clock to output	—	11	ns
t_{JPZX}	JTAG port high impedance to valid output	—	14	ns
t_{JPXZ}	JTAG port valid output to high impedance	—	14	ns

FPP Configuration Timing

DCLK-to-DATA[] Ratio (r) for FPP Configuration

Fast passive parallel (FPP) configuration requires a different DCLK-to-DATA[] ratio when you turn on encryption or the compression feature.

Depending on the DCLK-to-DATA[] ratio, the host must send a DCLK frequency that is *r* times the DATA[] rate in byte per second (Bps) or word per second (Wps). For example, in FPP ×16 where the *r* is 2, the DCLK frequency must be 2 times the DATA[] rate in Wps.

(69) The minimum TCK clock period is 167 ns if V_{CCBAT} is within the range 1.2 V – 1.5 V when you perform the volatile key programming.

FPP Configuration Timing when DCLK-to-DATA[] >1

Table 49. FPP Timing Parameters When the DCLK-to-DATA[] Ratio is >1 for Intel Cyclone 10 GX Devices

Use these timing parameters when you use the decompression and design security features.

Symbol	Parameter	Minimum	Maximum	Unit
t_{CF2CD}	nCONFIG low to CONF_DONE low	480	1,440	ns
t_{CF2ST0}	nCONFIG low to nSTATUS low	320	960	ns
t_{CFG}	nCONFIG low pulse width	2	—	µs
t_{STATUS}	nSTATUS low pulse width	268	3,000 (74)	µs
t_{CF2ST1}	nCONFIG high to nSTATUS high	—	3,000 (74)	µs
t_{CF2CK} (75)	nCONFIG high to first rising edge on DCLK	3,010	—	µs
t_{ST2CK} (75)	nSTATUS high to first rising edge of DCLK	10	—	µs
t_{DSU}	DATA[] setup time before rising edge on DCLK	5.5	—	ns
t_{DH}	DATA[] hold time after rising edge on DCLK	$N–1/f_{DCLK}$ (76)	—	s
t_{CH}	DCLK high time	$0.45 \times 1/f_{MAX}$	—	s
t_{CL}	DCLK low time	$0.45 \times 1/f_{MAX}$	—	s
t_{CLK}	DCLK period	$1/f_{MAX}$	—	s
f_{MAX}	DCLK frequency (FPP ×8/×16/×32)	—	100	MHz
t_R	Input rise time	—	40	ns
t_F	Input fall time	—	40	ns

continued...

(74) You can obtain this value if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.

(75) If nSTATUS is monitored, follow the t_{ST2CK} specification. If nSTATUS is not monitored, follow the t_{CF2CK} specification.

(76) *N* is the DCLK-to-DATA ratio and f_{DCLK} is the DCLK frequency the system is operating.

Symbol	Parameter	Minimum	Maximum	Unit
t_{CD2UM}	CONF_DONE high to user mode (77)	175	830	µs
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period	—	—
t_{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t_{CD2CU} + (600 × CLKUSR period)	—	—

Related Information

FPP Configuration Timing
Provides the FPP configuration timing waveforms.

AS Configuration Timing

Table 50. AS Timing Parameters for AS ×1 and AS ×4 Configurations in Intel Cyclone 10 GX Devices

The minimum and maximum numbers apply only if you choose the internal oscillator as the clock source for initializing the device.

The t_{CF2CD}, t_{CF2ST0}, t_{CFG}, t_{STATUS}, and t_{CF2ST1} timing parameters are identical to the timing parameters for passive serial (PS) mode listed in PS Timing Parameters for Intel Cyclone 10 GX Devices table.

Symbol	Parameter	Minimum	Maximum	Unit
t_{CO}	DCLK falling edge to AS_DATA0/ASDO output	—	2	ns
t_{SU}	Data setup time before falling edge on DCLK	1	—	ns
t_{DH}	Data hold time after falling edge on DCLK	1.5	—	ns
t_{CD2UM}	CONF_DONE high to user mode	175	830	µs
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period	—	—
t_{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t_{CD2CU} + (600 × CLKUSR period)	—	—

(77) The minimum and maximum numbers apply only if you use the internal oscillator as the clock source for initializing the device.

Symbol	Parameter	Minimum	Maximum	Unit
t_{CF2CK} (80)	nCONFIG high to first rising edge on DCLK	3,010	—	µs
t_{ST2CK} (80)	nSTATUS high to first rising edge of DCLK	10	—	µs
t_{DSU}	DATA[] setup time before rising edge on DCLK	5.5	—	ns
t_{DH}	DATA[] hold time after rising edge on DCLK	0	—	ns
t_{CH}	DCLK high time	0.45 × 1/f_{MAX}	—	s
t_{CL}	DCLK low time	0.45 × 1/f_{MAX}	—	s
t_{CLK}	DCLK period	1/f_{MAX}	—	s
f_{MAX}	DCLK frequency	—	125	MHz
t_{CD2UM}	CONF_DONE high to user mode (81)	175	830	µs
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period	—	—
t_{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t_{CD2CU} + (600 × CLKUSR period)	—	—

Related Information

PS Configuration Timing
Provides the PS configuration timing waveform.

(78) This value is applicable if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.

(79) This value is applicable if you do not delay configuration by externally holding the nSTATUS low.

(80) If nSTATUS is monitored, follow the t_{ST2CK} specification. If nSTATUS is not monitored, follow the t_{CF2CK} specification.

(81) The minimum and maximum numbers apply only if you choose the internal oscillator as the clock source for initializing the device.

Initialization

Table 53. Initialization Clock Source Option and the Maximum Frequency for Intel Cyclone 10 GX Devices

Initialization Clock Source	Configuration Scheme	Maximum Frequency (MHz)	Minimum Number of Clock Cycles
Internal Oscillator	AS, PS, and FPP	12.5	600
CLKUSR (82)(83)	AS, PS, and FPP	100	

Configuration Files

There are two types of configuration bit stream formats for different configuration schemes:

- PS and FPP—Raw Binary File (`.rbf`)
- AS—Raw Programming Data File (`.rpd`)

The `.rpd` file size follows the Intel configuration devices capacity. However, the actual configuration bit stream size for `.rpd` file is the same as `.rbf` file.

(82) To enable CLKUSR as the initialization clock source, in the Intel Quartus Prime software, select **Device and Pin Options ➤ General ➤ Device initialization clock source ➤ CLKUSR pin**.

(83) If you use the CLKUSR pin for AS and transceiver calibration simultaneously, the only allowed frequency is 100 MHz.

Remote System Upgrades

Table 56. Remote System Upgrade Circuitry Timing Specifications for Intel Cyclone 10 GX Devices

Parameter	Minimum	Maximum	Unit
$f_{MAX\_RU\_CLK}$ (86)	—	40	MHz
$t_{RU\_nCONFIG}$ (87)	250	—	ns
$t_{RU\_nRSTIMER}$ (88)	250	—	ns

Related Information

- Remote System Upgrade State Machine
  Provides more information about configuration reset (RU_CONFIG) signal.
- User Watchdog Timer
  Provides more information about reset_timer (RU_nRSTIMER) signal.

User Watchdog Internal Circuitry Timing Specifications

Table 57. User Watchdog Internal Oscillator Frequency Specifications for Intel Cyclone 10 GX Devices

Parameter	Minimum	Typical	Maximum	Unit
User watchdog internal oscillator frequency	5.3	7.9	12.5	MHz

I/O Timing

I/O timing data is typically used prior to designing the FPGA to get an estimate of the timing budget as part of the timing analysis. You may generate the I/O timing report manually using the Timing Analyzer or using the automated script.

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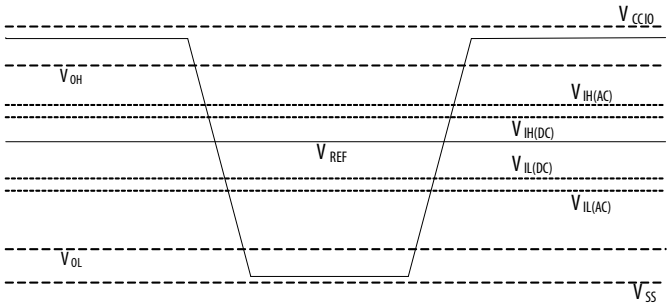
(86) This clock is user-supplied to the remote system upgrade circuitry. If you are using the Remote Update Intel FPGA IP core, the clock user-supplied to the Remote Update Intel FPGA IP core must meet this specification.

(87) This is equivalent to strobing the reconfiguration input of the Remote Update Intel FPGA IP core high for the minimum timing specification.

(88) This is equivalent to strobing the reset_timer input of the Remote Update Intel FPGA IP core high for the minimum timing specification.

Term	Definition
	
t_C	High-speed receiver/transmitter input and output clock period.
TCCS (channel-to-channel-skew)	The timing difference between the fastest and slowest output edges, including the t_{CO} variation and clock skew, across channels driven by the same PLL. The clock is included in the TCCS measurement (refer to the Timing Diagram figure under SW in this table).
t_{DUTY}	High-speed I/O block—Duty cycle on high-speed transmitter output clock.
t_{FALL}	Signal high-to-low transition time (80–20%)
t_{INCCJ}	Cycle-to-cycle jitter tolerance on the PLL clock input
t_{OUTPJ_IO}	Period jitter on the GPIO driven by a PLL
t_{OUTPJ_DC}	Period jitter on the dedicated clock output driven by a PLL
t_{RISE}	Signal low-to-high transition time (20–80%)
Timing Unit Interval (TUI)	The timing budget allowed for skew, propagation delays, and the data sampling window. (TUI = 1/(Receiver Input Clock Frequency Multiplication Factor) = t_C/w).
$V_{CM(DC)}$	DC Common mode input voltage.
V_{ICM}	Input Common mode voltage—The common mode of the differential signal at the receiver.
V_{ID}	Input differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the receiver.
$V_{DIF(AC)}$	AC differential input voltage—Minimum AC input differential voltage required for switching.
$V_{DIF(DC)}$	DC differential input voltage— Minimum DC input differential voltage required for switching.
V_{IH}	Voltage input high—The minimum positive voltage applied to the input which is accepted by the device as a logic high.

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Date	Version	Changes
November 2017	2017.11.10	• Changed the full symbol names for V_{CCR_GXB} and V_{CCT_GXB}, and changed the description for V_{CCH_GXB} in the *Transceiver Power Supply Operating Conditions for Intel Cyclone 10 GX Devices* table. • Removed note from the *Transceiver Power Supply Operating Conditions* section. • Added a footnote in the *Reference Clock Specifications* table. • Removed the "Programmable AC Gain at High Gain mode and Data Rate ≤ 12.5 Gbps" parameter from the *Receiver Specifications* table. • Changed the channel span descriptions for the x1 and x6 clock networks in the *Transceiver Clock Network Maximum Data Rate Specifications* table. • Changed the description of the VOD ratio in the *Typical Transmitter V_{OD} Settings* table. • Changed the specifications for CDR PPM deviation limit in the *Receiver Specifications* table. • Updated the description for V_{CCT_GXB}, V_{CCR_GXB}, and V_{CCH_GXB}. • Added note to V_I in the *Recommended Operating Conditions for Intel Cyclone 10 GX Devices* table. • Updated notes to RSDS and Mini-LVDS in the *Differential I/O Standards Specifications for Intel Cyclone 10 GX Devices* table. • Updated f_{VCO} specifications in the *Fractional PLL Specifications for Intel Cyclone 10 GX Devices* table. • Updated temperature range from "–40 to 125°C" to "–40 to 100°C" in the *Internal Temperature Sensing Diode Specifications for Intel Cyclone 10 GX Devices* table. • Updated the description for the *Memory Output Clock Jitter Specifications for Intel Cyclone 10 GX Devices* table. • Updated the following IP cores name: — Remote Update Intel FPGA — PHYLite for Parallel Interfaces Intel Cyclone 10 FPGA • Removed automotive-grade information. • Removed Preliminary tags.
May 2017	2017.05.08	Initial release.