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Details	
Product Status	Active
Number of LABs/CLBs	80330
Number of Logic Elements/Cells	220000
Total RAM Bits	13752320
Number of I/O	236
Number of Gates	-
Voltage - Supply	0.9V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	672-BBGA, FCBGA
Supplier Device Package	672-FBGA, FC (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/intel/10cx220yf672i5g

Intel® Cyclone® 10 GX Device Datasheet

This datasheet describes the electrical characteristics, switching characteristics, configuration specifications, and I/O timing for Intel® Cyclone® 10 GX devices.

Intel Cyclone 10 GX devices are offered in extended and industrial grades. Extended devices are offered in –E5 (fastest) and –E6 speed grades. Industrial grade devices are offered in the –I5 and –I6 speed grades.

Related Information

Intel Cyclone 10 GX Device Overview
Provides more information about the densities and packages in the Intel Cyclone 10 GX devices.

Electrical Characteristics

The following sections describe the operating conditions and power consumption of Intel Cyclone 10 GX devices.

Operating Conditions

Intel Cyclone 10 GX devices are rated according to a set of defined parameters. To maintain the highest possible performance and reliability of the Intel Cyclone 10 GX devices, you must consider the operating requirements described in this section.

Absolute Maximum Ratings

This section defines the maximum operating conditions for Intel Cyclone 10 GX devices. The values are based on experiments conducted with the devices and theoretical modeling of breakdown and damage mechanisms. The functional operation of the device is not implied for these conditions.

Caution: Conditions outside the range listed in the following table may cause permanent damage to the device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse effects on the device.

Table 1. Absolute Maximum Ratings for Intel Cyclone 10 GX Devices

Symbol	Description	Condition	Minimum	Maximum	Unit
V_{CC}	Core voltage power supply	—	–0.50	1.21	V
V_{CCP}	Periphery circuitry and transceiver fabric interface power supply	—	–0.50	1.21	V
V_{CCERAM}	Embedded memory power supply	—	–0.50	1.36	V
V_{CCPT}	Power supply for programmable power technology and I/O pre-driver	—	–0.50	2.46	V
V_{CCBAT}	Battery back-up power supply for design security volatile key register	—	–0.50	2.46	V
V_{CCPGM}	Configuration pins power supply	(1)	–0.50	2.46	V
V_{CCIO}	I/O buffers power supply	3 V I/O	–0.50	4.10	V
		LVDS I/O	–0.50	2.46	V
V_{CCA_PLL}	Phase-locked loop (PLL) analog power supply	—	–0.50	2.46	V
V_{CCT_GXB}	Transmitter power supply	—	–0.50	1.34	V
V_{CCR_GXB}	Receiver power supply	—	–0.50	1.34	V
V_{CCH_GXB}	Transceiver output buffer power supply	—	–0.50	2.46	V

continued...

(1) The LVDS I/O values are applicable to all dedicated and dual-function configuration I/Os.

Table 2. Maximum Allowed Overshoot During Transitions for Intel Cyclone 10 GX Devices

This table lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage of device lifetime. The LVDS I/O values are applicable to the VREFP_ADC and VREFN_ADC I/O pins.

Symbol	Description	Condition (V)		Overshoot Duration as % at T_J = 100°C	Unit
		LVDS I/O (7)	3 V I/O		
V_i (AC)	AC input voltage	2.50	3.80	100	%
		2.55	3.85	42	%
		2.60	3.90	18	%
		2.65	3.95	9	%
		2.70	4.00	4	%
		> 2.70	> 4.00	No overshoot allowed	%

For an overshoot of 2.5 V, the percentage of high time for the overshoot can be as high as 100% over a 10-year period. Percentage of high time is calculated as ([delta T]/T) × 100. This 10-year period assumes that the device is always turned on with 100% I/O toggle rate and 50% duty cycle signal.

(7) The LVDS I/O values are applicable to all dedicated and dual-function configuration I/Os.

Symbol	Description	Condition (V)	Resistance Tolerance		Unit
			–E5, –I5	–E6, –I6	
40-Ω, 60-Ω, and 120-Ω R_T	Internal parallel termination with calibration (40-Ω, 60-Ω, and 120-Ω setting)	V_{CCIO} = 1.5, 1.35, 1.25, 1.2	–10 to +40	–10 to +40	%
		V_{CCIO} = 1.2 (17)	± 15	± 15	%
80-Ω R_T	Internal parallel termination with calibration (80-Ω setting)	V_{CCIO} = 1.2	± 15	± 15	%

Related Information

I/O Standards Support in Intel Cyclone 10 GX Devices

OCT Without Calibration Resistance Tolerance Specifications

Table 8. OCT Without Calibration Resistance Tolerance Specifications for Intel Cyclone 10 GX Devices

This table lists the Intel Cyclone 10 GX OCT without calibration resistance tolerance to PVT changes.

Symbol	Description	Condition (V)	Resistance Tolerance		Unit
			–E5, –I5	–E6, –I6	
25-Ω and 50-Ω R_S	Internal series termination without calibration (25-Ω and 50-Ω setting)	V_{CCIO} = 3.0, 2.5	± 40	± 40	%
		V_{CCIO} = 1.8, 1.5, 1.2	± 50	± 50	%
34-Ω and 40-Ω R_S	Internal series termination without calibration (34-Ω and 40-Ω setting)	V_{CCIO} = 1.5, 1.35, 1.25, 1.2	± 50	± 50	%
48-Ω and 60-Ω R_S	Internal series termination without calibration (48-Ω and 60-Ω setting)	V_{CCIO} = 1.2	± 50	± 50	%
120-Ω R_s	Internal series termination without calibration (120-Ω setting)	V_{CCIO} = 1.2	± 50	± 50	%
100-Ω R_D	Internal differential termination (100-Ω setting)	V_{CCIO} = 1.8	± 35	± 40	%

(17) Only applicable to POD12 I/O standard.

Single-Ended I/O Standards Specifications

Table 12. Single-Ended I/O Standards Specifications for Intel Cyclone 10 GX Devices

I/O Standard	V_{CCIO} (V)			V_{IL} (V)		V_{IH} (V)		V_{OL} (V)	V_{OH} (V)	I_{OL} (20) (mA)	I_{OH} (20) (mA)
	Min	Typ	Max	Min	Max	Min	Max	Max	Min		
3.0-V LVTTL	2.85	3	3.15	–0.3	0.8	1.7	3.3	0.4	2.4	2	–2
3.0-V LVCMOS	2.85	3	3.15	–0.3	0.8	1.7	3.3	0.2	V_{CCIO} – 0.2	0.1	–0.1
2.5 V	2.375	2.5	2.625	–0.3	0.7	1.7	3.3	0.4	2	1	–1
1.8 V	1.71	1.8	1.89	–0.3	0.35 × V_{CCIO}	0.65 × V_{CCIO}	V_{CCIO} + 0.3	0.45	V_{CCIO} – 0.45	2	–2
1.5 V	1.425	1.5	1.575	–0.3	0.35 × V_{CCIO}	0.65 × V_{CCIO}	V_{CCIO} + 0.3	0.25 × V_{CCIO}	0.75 × V_{CCIO}	2	–2
1.2 V	1.14	1.2	1.26	–0.3	0.35 × V_{CCIO}	0.65 × V_{CCIO}	V_{CCIO} + 0.3	0.25 × V_{CCIO}	0.75 × V_{CCIO}	2	–2

Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications

Table 13. Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications for Intel Cyclone 10 GX Devices

I/O Standard	V_{CCIO} (V)			V_{REF} (V)			V_{TT} (V)		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
SSTL-18 Class I, II	1.71	1.8	1.89	0.833	0.9	0.969	V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04
SSTL-15 Class I, II	1.425	1.5	1.575	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}
SSTL-135/ SSTL-135 Class I, II	1.283	1.35	1.418	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}
SSTL-125/ SSTL-125 Class I, II	1.19	1.25	1.31	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}
SSTL-12/ SSTL-12 Class I, II	1.14	1.2	1.26	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}

continued...

(20) To meet the I_{OL} and I_{OH} specifications, you must set the current strength settings accordingly. For example, to meet the 3.0-V LVTTL specification (2 mA), you should set the current strength settings to 2 mA. Setting at lower current strength may not meet the I_{OL} and I_{OH} specifications in the datasheet.

I/O Standard	V_{CCIO} (V)			V_{REF} (V)			V_{TT} (V)		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
HSTL-18 Class I, II	1.71	1.8	1.89	0.85	0.9	0.95	—	$V_{CCIO}/2$	—
HSTL-15 Class I, II	1.425	1.5	1.575	0.68	0.75	0.9	—	$V_{CCIO}/2$	—
HSTL-12 Class I, II	1.14	1.2	1.26	0.47 × V_{CCIO}	0.5 × V_{CCIO}	0.53 × V_{CCIO}	—	$V_{CCIO}/2$	—
HSUL-12	1.14	1.2	1.3	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}	—	—	—
POD12	1.16	1.2	1.24	0.69 × V_{CCIO}	0.7 × V_{CCIO}	0.71 × V_{CCIO}	—	V_{CCIO}	—

Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications

Table 14. Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications for Intel Cyclone 10 GX Devices

I/O Standard	$V_{IL(DC)}$ (V)		$V_{IH(DC)}$ (V)		$V_{IL(AC)}$ (V)	$V_{IH(AC)}$ (V)	V_{OL} (V)	V_{OH} (V)	I_{OL} (21) (mA)	I_{OH} (21) (mA)
	Min	Max	Min	Max	Max	Min	Max	Min		
SSTL-18 Class I	–0.3	V_{REF} –0.125	V_{REF} + 0.125	V_{CCIO} + 0.3	V_{REF} – 0.25	V_{REF} + 0.25	V_{TT} – 0.603	V_{TT} + 0.603	6.7	–6.7
SSTL-18 Class II	–0.3	V_{REF} –0.125	V_{REF} + 0.125	V_{CCIO} + 0.3	V_{REF} – 0.25	V_{REF} + 0.25	0.28	V_{CCIO} –0.28	13.4	–13.4
SSTL-15 Class I	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.175	V_{REF} + 0.175	0.2 × V_{CCIO}	0.8 × V_{CCIO}	8	–8
SSTL-15 Class II	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.175	V_{REF} + 0.175	0.2 × V_{CCIO}	0.8 × V_{CCIO}	16	–16
SSTL-135/ SSTL-135 Class I, II	—	V_{REF} – 0.09	V_{REF} + 0.09	—	V_{REF} – 0.16	V_{REF} + 0.16	0.2 × V_{CCIO}	0.8 × V_{CCIO}	—	—
SSTL-125/ SSTL-125 Class I, II	—	V_{REF} – 0.09	V_{REF} + 0.09	—	V_{REF} – 0.15	V_{REF} + 0.15	0.2 × V_{CCIO}	0.8 × V_{CCIO}	—	—

continued...

(21) To meet the I_{OL} and I_{OH} specifications, you must set the current strength settings accordingly. For example, to meet the SSTL15CI specification (8 mA), you should set the current strength settings to 8 mA. Setting at lower current strength may not meet the I_{OL} and I_{OH} specifications in the datasheet.

I/O Standard	$V_{IL(DC)}$ (V)		$V_{IH(DC)}$ (V)		$V_{IL(AC)}$ (V)	$V_{IH(AC)}$ (V)	V_{OL} (V)	V_{OH} (V)	I_{OL} (21) (mA)	I_{OH} (21) (mA)
	Min	Max	Min	Max	Max	Min	Max	Min		
SSTL-12/ SSTL-12 Class I, II	—	V_{REF} – 0.10	V_{REF} + 0.10	—	V_{REF} – 0.15	V_{REF} + 0.15	0.2 × V_{CCIO}	0.8 × V_{CCIO}	—	—
HSTL-18 Class I	—	V_{REF} –0.1	V_{REF} + 0.1	—	V_{REF} – 0.2	V_{REF} + 0.2	0.4	V_{CCIO} – 0.4	8	–8
HSTL-18 Class II	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.2	V_{REF} + 0.2	0.4	V_{CCIO} – 0.4	16	–16
HSTL-15 Class I	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.2	V_{REF} + 0.2	0.4	V_{CCIO} – 0.4	8	–8
HSTL-15 Class II	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.2	V_{REF} + 0.2	0.4	V_{CCIO} –0.4	16	–16
HSTL-12 Class I	–0.15	V_{REF} – 0.08	V_{REF} + 0.08	V_{CCIO} + 0.15	V_{REF} – 0.15	V_{REF} + 0.15	0.25 × V_{CCIO}	0.75 × V_{CCIO}	8	–8
HSTL-12 Class II	–0.15	V_{REF} – 0.08	V_{REF} + 0.08	V_{CCIO} + 0.15	V_{REF} – 0.15	V_{REF} + 0.15	0.25 × V_{CCIO}	0.75 × V_{CCIO}	16	–16
HSUL-12	—	V_{REF} – 0.13	V_{REF} + 0.13	—	V_{REF} – 0.22	V_{REF} + 0.22	0.1 × V_{CCIO}	0.9 × V_{CCIO}	—	—
POD12	–0.15	V_{REF} – 0.08	V_{REF} + 0.08	V_{CCIO} + 0.15	V_{REF} – 0.15	V_{REF} + 0.15	(0.7 – 0.15) × V_{CCIO}	(0.7 + 0.15) × V_{CCIO}	—	—

Differential SSTL I/O Standards Specifications

Table 15. Differential SSTL I/O Standards Specifications for Intel Cyclone 10 GX Devices

I/O Standard	V_{CCIO} (V)			$V_{SWING(DC)}$ (V)		$V_{SWING(AC)}$ (V)		$V_{IX(AC)}$ (V)		
	Min	Typ	Max	Min	Max	Min	Max	Min	Typ	Max
SSTL-18 Class I, II	1.71	1.8	1.89	0.25	V_{CCIO} + 0.6	0.5	V_{CCIO} + 0.6	$V_{CCIO}/2$ – 0.175	—	$V_{CCIO}/2$ + 0.175
SSTL-15 Class I, II	1.425	1.5	1.575	0.2	(22)	$2(V_{IH(AC)} – V_{REF})$	$2(V_{REF} – V_{IL(AC)})$	$V_{CCIO}/2$ – 0.15	—	$V_{CCIO}/2$ + 0.15

continued...

(21) To meet the I_{OL} and I_{OH} specifications, you must set the current strength settings accordingly. For example, to meet the SSTL15CI specification (8 mA), you should set the current strength settings to 8 mA. Setting at lower current strength may not meet the I_{OL} and I_{OH} specifications in the datasheet.

I/O Standard	V_{CCIO} (V)			$V_{SWING(DC)}$ (V)		$V_{SWING(AC)}$ (V)		$V_{IX(AC)}$ (V)		
	Min	Typ	Max	Min	Max	Min	Max	Min	Typ	Max
SSTL-135/ SSTL-135 Class I, II	1.283	1.35	1.45	0.18	(22)	$2(V_{IH(AC)} - V_{REF})$	$2(V_{IL(AC)} - V_{REF})$	$V_{CCIO}/2 - 0.15$	$V_{CCIO}/2$	$V_{CCIO}/2 + 0.15$
SSTL-125/ SSTL-125 Class I, II	1.19	1.25	1.31	0.18	(22)	$2(V_{IH(AC)} - V_{REF})$	$2(V_{IL(AC)} - V_{REF})$	$V_{CCIO}/2 - 0.15$	$V_{CCIO}/2$	$V_{CCIO}/2 + 0.15$
SSTL-12/ SSTL-12 Class I, II	1.14	1.2	1.26	0.16	(22)	$2(V_{IH(AC)} - V_{REF})$	$2(V_{IL(AC)} - V_{REF})$	$V_{REF} - 0.15$	$V_{CCIO}/2$	$V_{REF} + 0.15$
POD12	1.16	1.2	1.24	0.16	—	0.3	—	$V_{REF} - 0.08$	—	$V_{REF} + 0.08$

Differential HSTL and HSUL I/O Standards Specifications

Table 16. Differential HSTL and HSUL I/O Standards Specifications for Intel Cyclone 10 GX Devices

I/O Standard	V_{CCIO} (V)			$V_{DIF(DC)}$ (V)		$V_{DIF(AC)}$ (V)		$V_{IX(AC)}$ (V)			$V_{CM(DC)}$ (V)		
	Min	Typ	Max	Min	Max	Min	Max	Min	Typ	Max	Min	Typ	Max
HSTL-18 Class I, II	1.71	1.8	1.89	0.2	—	0.4	—	0.78	—	1.12	0.78	—	1.12
HSTL-15 Class I, II	1.425	1.5	1.575	0.2	—	0.4	—	0.68	—	0.9	0.68	—	0.9
HSTL-12 Class I, II	1.14	1.2	1.26	0.16	$V_{CCIO} + 0.3$	0.3	$V_{CCIO} + 0.48$	—	$0.5 \times V_{CCIO}$	—	$0.4 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.6 \times V_{CCIO}$
HSUL-12	1.14	1.2	1.3	$2(V_{IH(DC)} - V_{REF})$	$2(V_{REF} - V_{IH(DC)})$	$2(V_{IH(AC)} - V_{REF})$	$2(V_{REF} - V_{IH(AC)})$	$0.5 \times V_{CCIO} - 0.12$	$0.5 \times V_{CCIO}$	$0.5 \times V_{CCIO} + 0.12$	$0.4 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.6 \times V_{CCIO}$

(22) The maximum value for $V_{SWING(DC)}$ is not defined. However, each single-ended signal needs to be within the respective single-ended limits ($V_{IH(DC)}$ and $V_{IL(DC)}$).

Switching Characteristics

This section provides the performance characteristics of Intel Cyclone 10 GX core and periphery blocks for extended grade devices.

Transceiver Performance Specifications

Transceiver Performance for Intel Cyclone 10 GX Devices

Table 18. Transmitter and Receiver Data Rate Performance

Symbol/Description	Condition	Datarate	Unit
Chip-to-Chip (29)	Maximum data rate V_{CCR_GXB} = V_{CCT_GXB} = 1.03 V	12.5	Gbps
	Maximum data rate V_{CCR_GXB} = V_{CCT_GXB} = 0.95 V	11.3	Gbps
	Minimum Data Rate	1.0 (30)	Gbps
Backplane	Maximum data rate V_{CCR_GXB} = V_{CCT_GXB} = 1.03 V	6.6	Gbps
	Minimum Data Rate	1.0 (30)	Gbps

Table 19. ATX PLL and Fractional PLL (fPLL) Performance

Symbol/Description	Condition	Frequency	Unit
Supported Output Frequency	Maximum Frequency	6.25	GHz
	Minimum Frequency	500	MHz

(29) Chip-to-chip links are applications with short reach channels.

(30) Intel Cyclone 10 GX transceivers can support data rates down to 125 Mbps with over sampling. You must create your own over sampling logic.

Symbol/Description	Condition	Min	Typ	Max	Unit
Input Reference Clock Frequency (CMU PLL)		61	—	800	MHz
Input Reference Clock Frequency (ATX PLL)		100	—	800	MHz
Input Reference Clock Frequency (fPLL PLL)		25 (32) / 50	—	800	MHz
Rise time	20% to 80%	—	—	400	ps
Fall time	80% to 20%	—	—	400	ps
Duty cycle	—	45	—	55	%
Spread-spectrum modulating clock frequency	PCIe	30	—	33	kHz
Spread-spectrum downspread	PCIe	—	0 to –0.5	—	%
On-chip termination resistors	—	—	100	—	Ω
Absolute V_{MAX}	Dedicated reference clock pin	—	—	1.6	V
	RX pin as a reference clock	—	—	1.2	V
Absolute V_{MIN}	—	–0.4	—	—	V
Peak-to-peak differential input voltage	—	200	—	1600	mV
V_{ICM} (AC coupled)	V_{CCR_GXB} = 0.95 V	—	0.95	—	V
	V_{CCR_GXB} = 1.03 V	—	1.03	—	V
V_{ICM} (DC coupled)	HCSL I/O standard for PCIe reference clock	250	—	550	mV
Transmitter REFCLK Phase Noise (622 MHz) (33)	100 Hz	—	—	–70	dBc/Hz
	1 kHz	—	—	–90	dBc/Hz

continued...

(32) 25 MHz is for HDMI applications only.

(33) To calculate the REFCLK phase noise requirement at frequencies other than 622 MHz, use the following formula: REFCLK phase noise at f (MHz) = REFCLK phase noise at 622 MHz + 20*log(f/622).

Symbol/Description	Condition	Min	Typ	Max	Unit
	100-Ω setting	—	100 ± 20%	—	Ω
V_{OCM} (AC coupled)	V_{CCT_GXB} = 0.95 V	—	450	—	mV
	V_{CCT_GXB} = 1.03 V	—	500	—	mV
V_{OCM} (DC coupled)	V_{CCT_GXB} = 0.95 V	—	450	—	mV
	V_{CCT_GXB} = 1.03 V	—	500	—	mV
Rise time (45)	20% to 80%	20	—	130	ps
Fall time (45)	80% to 20%	20	—	130	ps
Intra-differential pair skew	TX V_{CM} = 0.5 V and slew rate setting of SLEW_R5 (46)	—	—	15	ps

Table 27. Typical Transmitter V_{OD} Settings

Symbol	V_{OD} Setting	V_{OD}-to-V_{CCT_GXB} Ratio
V_{OD} differential value = V_{OD}-to-V_{CCT_GXB} ratio x V_{CCT_GXB}	31	1.00
	30	0.97
	29	0.93
	28	0.90
	27	0.87
	26	0.83
	25	0.80
	24	0.77
	23	0.73
	22	0.70

continued...

(45) The Intel Quartus Prime software automatically selects the appropriate slew rate depending on the design configurations.

(46) SLEW_R1 is the slowest and SLEW_R5 is the fastest. SLEW_R6 and SLEW_R7 are not used.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_{LOCK}	Time required to lock from end-of-device configuration or deassertion of `pll_powerdown`	—	—	—	1	ms
t_{DLOCK}	Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays)	—	—	—	1	ms
f_{CLBW}	PLL closed-loop bandwidth	—	0.3	—	4	MHz
t_{PLL_PSERR}	Accuracy of PLL phase shift	—	—	—	50	ps
t_{ARESET}	Minimum pulse width on the `pll_powerdown` signal	—	10	—	—	ns
t_{INCCJ} (50)(51)	Input clock cycle-to-cycle jitter	$F_{REF} \geq 100$ MHz	—	—	0.13	UI (p-p)
		$F_{REF} < 100$ MHz	—	—	650	ps (p-p)
t_{OUTPJ} (52)	Period jitter for clock output	$F_{OUT} \geq 100$ MHz	—	—	600	ps (p-p)
		$F_{OUT} < 100$ MHz	—	—	60	mUI (p-p)
t_{OUTCCJ} (52)	Cycle-to-cycle jitter for clock output	$F_{OUT} \geq 100$ MHz	—	—	600	ps (p-p)
		$F_{OUT} < 100$ MHz	—	—	60	mUI (p-p)
dK_{BIT}	Bit number of Delta Sigma Modulator (DSM)	—	—	32	—	bit

Related Information

Memory Output Clock Jitter Specifications on page 43
Provides more information about the external memory interface clock output jitter specifications.

(50) A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source with jitter < 120 ps.

(51) F_{REF} is f_{IN}/N, specification applies when $N = 1$.

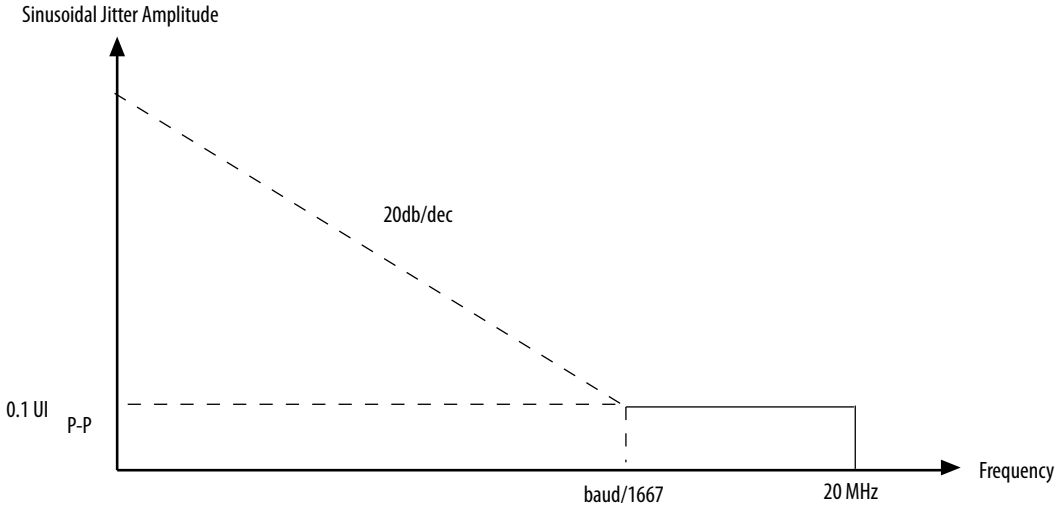
(52) External memory interface clock output jitter specifications use a different measurement method, which are available in Memory Output Clock Jitter Specification for Intel Cyclone 10 GX Devices table.

Symbol		Condition	–E5, –I5			–E6, –I6			Unit
			Min	Typ	Max	Min	Typ	Max	
	TCCS (64)(59)	True Differential I/O Standards	—	—	150	—	—	150	ps
Receiver	True Differential I/O Standards - $f_{HSDRDPA}$ (data rate)	SERDES factor J = 4 to 10 (60)(61)(62)	150	—	1434	150	—	1250	Mbps
		SERDES factor J = 3 (60)(61)(62)	150	—	1076	150	—	938	Mbps
	f_{HSDR} (data rate) (without DPA) (59)	SERDES factor J = 3 to 10	(62)	—	(66)	(62)	—	(66)	Mbps
		SERDES factor J = 2, uses DDR registers	(62)	—	(63)	(62)	—	(63)	Mbps
		SERDES factor J = 1, uses DDR registers	(62)	—	(63)	(62)	—	(63)	Mbps
DPA (FIFO mode)	DPA run length	—	—	—	10000	—	—	10000	UI
DPA (soft CDR mode)	DPA run length	SGMII/GbE protocol	—	—	5	—	—	5	UI
		All other protocols	—	—	50 data transition per 208 UI	—	—	50 data transition per 208 UI	—
Soft CDR mode	Soft-CDR ppm tolerance	—	—	—	300	—	—	300	± ppm
Non DPA mode	Sampling Window	—	—	—	300	—	—	300	ps

(65) This applies to default pre-emphasis and V_{OD} settings only.

(66) You can estimate the achievable maximum data rate for non-DPA mode by performing link timing closure analysis. You must consider the board skew margin, transmitter delay margin, and receiver sampling margin to determine the maximum data rate supported.

Figure 4. LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specifications for a Data Rate Less than 1.4 Gbps



Memory Standards Supported by the Hard Memory Controller

Table 40. Memory Standards Supported by the Hard Memory Controller for Intel Cyclone 10 GX Devices

This table lists the overall capability of the hard memory controller. For specific details, refer to the External Memory Interface Spec Estimator.

Memory Standard	Rate Support	Speed Grade	Ping Pong PHY Support	Maximum Frequency (MHz)	
				I/O Bank	3 V I/O Bank
DDR3 SDRAM	Half rate	–5	Yes	533	225
			—	533	225
		–6	Yes	466	166
			—	466	166
	Quarter rate	–5	Yes	933	450
			—	933	450
		–6	Yes	933	333

continued...

Memory Standard	Rate Support	Speed Grade	Ping Pong PHY Support	Maximum Frequency (MHz)	
				I/O Bank	3 V I/O Bank
			—	933	333
DDR3L SDRAM	Half rate	–5	Yes	533	225
			—	533	225
		–6	Yes	466	166
			—	466	166
	Quarter rate	–5	Yes	933	450
			—	933	450
		–6	Yes	933	333
			—	933	333
LPDDR3 SDRAM	Half rate	–5	—	400	225
		–6	—	333	166
	Quarter rate	–5	—	800	450
		–6	—	666	333

Related Information

External Memory Interface Spec Estimator
Provides the specific details of the memory standards supported.

DLL Range Specifications

Table 41. DLL Frequency Range Specifications for Intel Cyclone 10 GX Devices

Intel Cyclone 10 GX devices support memory interface frequencies lower than 600 MHz, although the reference clock that feeds the DLL must be at least 600 MHz. To support interfaces below 600 MHz, multiply the reference clock feeding the DLL to ensure the frequency is within the supported range.

Parameter	Performance (for All Speed Grades)	Unit
DLL operating frequency range	600 – 1333	MHz

DQS Logic Block Specifications

Table 42. DQS Phase Shift Error Specifications for DLL-Delayed Clock (t_{DQS_PSERR}) for Intel Cyclone 10 GX Devices

This error specification is the absolute maximum and minimum error.

Symbol	Performance (for All Speed Grades)	Unit
t_{DQS_PSERR}	5	ps

Memory Output Clock Jitter Specifications

Table 43. Memory Output Clock Jitter Specifications for Intel Cyclone 10 GX Devices

The clock jitter specification applies to the memory output clock pins clocked by an I/O PLL, or generated using differential signal-splitter and double data I/O circuits clocked by a PLL output routed on a PHY clock network as specified. Intel recommends using PHY clock networks for better jitter performance.

The memory output clock jitter is applicable when an input jitter of 10 ps peak-to-peak is applied with bit error rate (BER) 10^{-12}, equivalent to 14 sigma.

Protocol	Parameter	Symbol	Data Rate (Mbps)	Min	Max	Unit
DDR3	Clock period jitter	$t_{JIT(per)}$	1,866	–40	40	ps
	Cycle-to-cycle period jitter	$t_{JIT(cc)}$	1,866	–40	40	ps
	Duty cycle jitter	$t_{JIT(duty)}$	1,866	–40	40	ps

OCT Calibration Block Specifications

Table 44. OCT Calibration Block Specifications for Intel Cyclone 10 GX Devices

Symbol	Description	Min	Typ	Max	Unit
OCTUSRCLK	Clock required by OCT calibration blocks	—	—	20	MHz
T_{OCTCAL}	Number of OCTUSRCLK clock cycles required for R_S OCT /R_T OCT calibration	> 2000	—	—	Cycles
$T_{OCTSHIFT}$	Number of OCTUSRCLK clock cycles required for OCT code to shift out	—	32	—	Cycles
T_{RS_RT}	Time required between the `dyn_term_ctrl` and `oe` signal transitions in a bidirectional I/O buffer to dynamically switch between R_S OCT and R_T OCT	—	2.5	—	ns

Table 47. DCLK-to-DATA[] Ratio for Intel Cyclone 10 GX Devices

You cannot turn on encryption and compression at the same time for Intel Cyclone 10 GX devices.

Configuration Scheme	Encryption	Compression	DCLK-to-DATA[] Ratio (r)
FPP (8-bit wide)	Off	Off	1
	On	Off	1
	Off	On	2
FPP (16-bit wide)	Off	Off	1
	On	Off	2
	Off	On	4
FPP (32-bit wide)	Off	Off	1
	On	Off	4
	Off	On	8

FPP Configuration Timing when DCLK-to-DATA[] = 1

Note: When you enable decompression or the design security feature, the DCLK-to-DATA[] ratio varies for FPP ×8, FPP ×16, and FPP ×32. For the respective DCLK-to-DATA[] ratio, refer to the DCLK-to-DATA[] Ratio for Intel Cyclone 10 GX Devices table.

Table 48. FPP Timing Parameters When the DCLK-to-DATA[] Ratio is 1 for Intel Cyclone 10 GX Devices

Use these timing parameters when the decompression and design security features are disabled.

Symbol	Parameter	Minimum	Maximum	Unit
t_{CF2CD}	nCONFIG low to CONF_DONE low	480	1,440	ns
t_{CF2ST0}	nCONFIG low to nSTATUS low	320	960	ns
t_{CFG}	nCONFIG low pulse width	2	—	µs
t_{STATUS}	nSTATUS low pulse width	268	3,000 (70)	µs
t_{CF2ST1}	nCONFIG high to nSTATUS high	—	3,000 (71)	µs

continued...

(70) This value is applicable if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.

Symbol	Parameter	Minimum	Maximum	Unit
t_{CF2CK} (72)	nCONFIG high to first rising edge on DCLK	3,010	—	µs
t_{ST2CK} (72)	nSTATUS high to first rising edge of DCLK	10	—	µs
t_{DSU}	DATA[] setup time before rising edge on DCLK	5.5	—	ns
t_{DH}	DATA[] hold time after rising edge on DCLK	0	—	ns
t_{CH}	DCLK high time	0.45 × 1/f_{MAX}	—	s
t_{CL}	DCLK low time	0.45 × 1/f_{MAX}	—	s
t_{CLK}	DCLK period	1/f_{MAX}	—	s
f_{MAX}	DCLK frequency (FPP ×8/×16/×32)	—	100	MHz
t_{CD2UM}	CONF_DONE high to user mode (73)	175	830	µs
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period	—	—
t_{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t_{CD2CU} + (600 × CLKUSR period)	—	—

Related Information

FPP Configuration Timing
Provides the FPP configuration timing waveforms.

(71) This value is applicable if you do not delay configuration by externally holding the nSTATUS low.

(72) If nSTATUS is monitored, follow the t_{ST2CK} specification. If nSTATUS is not monitored, follow the t_{CF2CK} specification.

(73) The minimum and maximum numbers apply only if you chose the internal oscillator as the clock source for initializing the device.

FPP Configuration Timing when DCLK-to-DATA[] >1

Table 49. FPP Timing Parameters When the DCLK-to-DATA[] Ratio is >1 for Intel Cyclone 10 GX Devices

Use these timing parameters when you use the decompression and design security features.

Symbol	Parameter	Minimum	Maximum	Unit
t_{CF2CD}	nCONFIG low to CONF_DONE low	480	1,440	ns
t_{CF2ST0}	nCONFIG low to nSTATUS low	320	960	ns
t_{CFG}	nCONFIG low pulse width	2	—	µs
t_{STATUS}	nSTATUS low pulse width	268	3,000 (74)	µs
t_{CF2ST1}	nCONFIG high to nSTATUS high	—	3,000 (74)	µs
t_{CF2CK} (75)	nCONFIG high to first rising edge on DCLK	3,010	—	µs
t_{ST2CK} (75)	nSTATUS high to first rising edge of DCLK	10	—	µs
t_{DSU}	DATA[] setup time before rising edge on DCLK	5.5	—	ns
t_{DH}	DATA[] hold time after rising edge on DCLK	$N–1/f_{DCLK}$ (76)	—	s
t_{CH}	DCLK high time	$0.45 \times 1/f_{MAX}$	—	s
t_{CL}	DCLK low time	$0.45 \times 1/f_{MAX}$	—	s
t_{CLK}	DCLK period	$1/f_{MAX}$	—	s
f_{MAX}	DCLK frequency (FPP ×8/×16/×32)	—	100	MHz
t_R	Input rise time	—	40	ns
t_F	Input fall time	—	40	ns

continued...

(74) You can obtain this value if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.

(75) If nSTATUS is monitored, follow the t_{ST2CK} specification. If nSTATUS is not monitored, follow the t_{CF2CK} specification.

(76) *N* is the DCLK-to-DATA ratio and f_{DCLK} is the DCLK frequency the system is operating.

Term	Definition
$V_{IH(AC)}$	High-level AC input voltage
$V_{IH(DC)}$	High-level DC input voltage
V_{IL}	Voltage input low—The maximum positive voltage applied to the input which is accepted by the device as a logic low.
$V_{IL(AC)}$	Low-level AC input voltage
$V_{IL(DC)}$	Low-level DC input voltage
V_{OCM}	Output Common mode voltage—The common mode of the differential signal at the transmitter.
V_{OD}	Output differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission line at the transmitter.
V_{SWING}	Differential input voltage
V_{IX}	Input differential cross point voltage
V_{OX}	Output differential cross point voltage
W	High-speed I/O block—Clock Boost Factor

Document Revision History for the Intel Cyclone 10 GX Device Datasheet

Document Version	Changes
2018.06.15	• Added *Intel Cyclone 10 GX Devices Overshoot Duration* figure and description. • Added a link in the *OCT Calibration Accuracy Specifications* section. • Removed *Equation for OCT Variation Without Recalibration*. • Updated the note to CLKUSR in the *Initialization Clock Source Option and the Maximum Frequency for Intel Cyclone 10 GX Devices* table. • Updated the *I/O Timing* section on the I/O timing information generation guidelines. • Updated the description and maximum offset values in the *IOE Programmable Delay for Intel Cyclone 10 GX Devices* table.
2018.04.06	Added notes to I_{OUT} specification in the *Absolute Maximum Ratings for Intel Cyclone 10 GX Devices* table.