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Details	
Product Status	Active
Number of LABs/CLBs	80330
Number of Logic Elements/Cells	220000
Total RAM Bits	13752320
Number of I/O	236
Number of Gates	-
Voltage - Supply	0.9V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	672-BBGA, FCBGA
Supplier Device Package	672-FBGA, FC (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/intel/10cx220yf672i6g

Intel® Cyclone® 10 GX Device Datasheet

This datasheet describes the electrical characteristics, switching characteristics, configuration specifications, and I/O timing for Intel® Cyclone® 10 GX devices.

Intel Cyclone 10 GX devices are offered in extended and industrial grades. Extended devices are offered in –E5 (fastest) and –E6 speed grades. Industrial grade devices are offered in the –I5 and –I6 speed grades.

Related Information

Intel Cyclone 10 GX Device Overview
Provides more information about the densities and packages in the Intel Cyclone 10 GX devices.

Electrical Characteristics

The following sections describe the operating conditions and power consumption of Intel Cyclone 10 GX devices.

Operating Conditions

Intel Cyclone 10 GX devices are rated according to a set of defined parameters. To maintain the highest possible performance and reliability of the Intel Cyclone 10 GX devices, you must consider the operating requirements described in this section.

Absolute Maximum Ratings

This section defines the maximum operating conditions for Intel Cyclone 10 GX devices. The values are based on experiments conducted with the devices and theoretical modeling of breakdown and damage mechanisms. The functional operation of the device is not implied for these conditions.

Caution: Conditions outside the range listed in the following table may cause permanent damage to the device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse effects on the device.

Table 1. Absolute Maximum Ratings for Intel Cyclone 10 GX Devices

Symbol	Description	Condition	Minimum	Maximum	Unit
V_{CC}	Core voltage power supply	—	–0.50	1.21	V
V_{CCP}	Periphery circuitry and transceiver fabric interface power supply	—	–0.50	1.21	V
V_{CCERAM}	Embedded memory power supply	—	–0.50	1.36	V
V_{CCPT}	Power supply for programmable power technology and I/O pre-driver	—	–0.50	2.46	V
V_{CCBAT}	Battery back-up power supply for design security volatile key register	—	–0.50	2.46	V
V_{CCPGM}	Configuration pins power supply	(1)	–0.50	2.46	V
V_{CCIO}	I/O buffers power supply	3 V I/O	–0.50	4.10	V
		LVDS I/O	–0.50	2.46	V
V_{CCA_PLL}	Phase-locked loop (PLL) analog power supply	—	–0.50	2.46	V
V_{CCT_GXB}	Transmitter power supply	—	–0.50	1.34	V
V_{CCR_GXB}	Receiver power supply	—	–0.50	1.34	V
V_{CCH_GXB}	Transceiver output buffer power supply	—	–0.50	2.46	V

continued...

(1) The LVDS I/O values are applicable to all dedicated and dual-function configuration I/Os.

Symbol	Description	Condition	Minimum	Maximum	Unit
I_{OUT}	DC output current per pin	—	−25 (2)(3)(4)(5)(6)	25	mA
T_J	Operating junction temperature	—	−55	125	°C
T_{STG}	Storage temperature (no bias)	—	−65	150	°C

Related Information

- AN 692: Power Sequencing Considerations for Intel Cyclone 10 GX, Intel Arria 10, and Intel Stratix 10 Devices
  Provides the power sequencing requirements for Intel Cyclone 10 GX devices.
- Power-Up and Power-Down Sequences, Power Management in Intel Cyclone 10 GX Devices chapter
  Provides the power sequencing requirements for Intel Cyclone 10 GX devices.

Maximum Allowed Overshoot and Undershoot Voltage

During transitions, input signals may overshoot to the voltage listed in the following table and undershoot to −2.0 V for input currents less than 100 mA and periods shorter than 20 ns.

The maximum allowed overshoot duration is specified as a percentage of high time over the lifetime of the device. A DC signal is equivalent to 100% duty cycle.

For example, a signal that overshoots to 2.70 V for LVDS I/O can only be at 2.70 V for ~4% over the lifetime of the device.

---

(2) The maximum current allowed through any LVDS I/O bank pin when the device is not turned on or during power-up/power-down conditions is 10 mA.

(3) Total current per LVDS I/O bank must not exceed 100 mA.

(4) Voltage level must not exceed 1.89 V.

(5) Applies to all I/O standards and settings supported by LVDS I/O banks, including single-ended and differential I/Os.

(6) Applies only to LVDS I/O banks. 3 V I/O banks are not covered under this specification and must be implemented as per the power sequencing requirement. For more details, refer to *AN 692: Power Sequencing Considerations for Intel Cyclone 10 GX, Intel Arria® 10, and Intel Stratix® 10 Devices* and *Power Management in Intel Cyclone 10 GX Devices chapter*.

Table 2. Maximum Allowed Overshoot During Transitions for Intel Cyclone 10 GX Devices

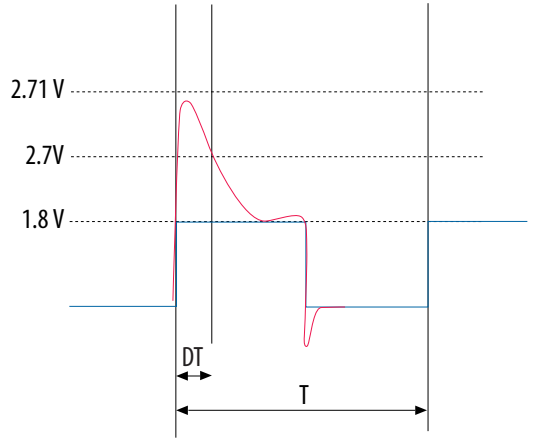
This table lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage of device lifetime. The LVDS I/O values are applicable to the VREFP_ADC and VREFN_ADC I/O pins.

Symbol	Description	Condition (V)		Overshoot Duration as % at T_J = 100°C	Unit
		LVDS I/O (7)	3 V I/O		
V_i (AC)	AC input voltage	2.50	3.80	100	%
		2.55	3.85	42	%
		2.60	3.90	18	%
		2.65	3.95	9	%
		2.70	4.00	4	%
		> 2.70	> 4.00	No overshoot allowed	%

For an overshoot of 2.5 V, the percentage of high time for the overshoot can be as high as 100% over a 10-year period. Percentage of high time is calculated as ([delta T]/T) × 100. This 10-year period assumes that the device is always turned on with 100% I/O toggle rate and 50% duty cycle signal.

(7) The LVDS I/O values are applicable to all dedicated and dual-function configuration I/Os.

Figure 1. Intel Cyclone 10 GX Devices Overshoot Duration



Recommended Operating Conditions

This section lists the functional operation limits for the AC and DC parameters for Intel Cyclone 10 GX devices.

Recommended Operating Conditions

Table 3. Recommended Operating Conditions for Intel Cyclone 10 GX Devices

This table lists the steady-state voltage values expected from Intel Cyclone 10 GX devices. Power supply ramps must all be strictly monotonic, without plateaus.

Symbol	Description	Condition	Minimum (8)	Typical	Maximum (8)	Unit
V_{CC}	Core voltage power supply	—	0.87	0.9	0.93	V
V_{CCP}	Periphery circuitry and transceiver fabric interface power supply	—	0.87	0.9	0.93	V
V_{CCPGM}	Configuration pins power supply	1.8 V	1.71	1.8	1.89	V
		1.5 V	1.425	1.5	1.575	V

continued...

(8) This value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

Symbol	Description	Condition	Minimum (8)	Typical	Maximum (8)	Unit
V_I (11)(12)	DC input voltage	3 V I/O	–0.3	—	3.3	V
		LVDS I/O	–0.3	—	2.19	V
V_O	Output voltage	—	0	—	V_{CCIO}	V
T_J	Operating junction temperature	Extended	0	—	100	°C
		Industrial	–40	—	100	°C
t_{RAMP} (13)	Power supply ramp time	Standard POR	200 µs	—	100 ms	—
		Fast POR	200 µs	—	4 ms	—

Related Information

I/O Standard Specifications on page 15

Transceiver Power Supply Operating Conditions

Table 4. Transceiver Power Supply Operating Conditions for Intel Cyclone 10 GX Devices

Symbol	Description	Condition	Minimum (14)	Typical	Maximum (14)	Unit
$V_{CCT\_GXB[L1][C,D]}$	Transmitter power supply	Chip-to-chip ≤ 12.5 Gbps Or	1.0	1.03	1.06	V

continued...

(8) This value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

(11) The LVDS I/O values are applicable to all dedicated and dual-function configuration I/Os.

(12) This value applies to both input and tri-stated output configuration. Pin voltage should not be externally pulled higher than the maximum value.

(13) t_{ramp} is the ramp time of each individual power supply, not the ramp time of all combined power supplies.

(14) This value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

Related Information

- Early Power Estimator User Guide
  Provides more information about power estimation tools.
- Power Analysis and Optimization User Guide: Intel Quartus Prime Pro Edition
  Provides more information about power estimation tools.

I/O Pin Leakage Current

Table 5. I/O Pin Leakage Current for Intel Cyclone 10 GX Devices

If $V_O = V_{CCIO}$ to $V_{CCIOMAX}$, 300 µA of leakage current per I/O is expected.

Symbol	Description	Condition	Min	Max	Unit
I_I	Input pin	V_I = 0 V to $V_{CCIOMAX}$	–80	80	µA
I_{OZ}	Tri-stated I/O pin	V_O = 0 V to $V_{CCIOMAX}$	–80	80	µA

Bus Hold Specifications

The bus-hold trip points are based on calculated input voltages from the JEDEC standard.

Table 6. Bus Hold Parameters for Intel Cyclone 10 GX Devices

Parameter	Symbol	Condition	V_{CCIO} (V)										Unit
			1.2		1.5		1.8		2.5		3.0		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Bus-hold, low, sustaining current	I_{SUSL}	$V_{IN} > V_{IL}$ (max)	8 (15), 26 (16)	—	12 (15), 32 (16)	—	30 (15), 55 (16)	—	60	—	70	—	µA
Bus-hold, high, sustaining current	I_{SUSH}	$V_{IN} < V_{IH}$ (min)	–8 (15), –26 (16)	—	–12 (15), –32 (16)	—	–30 (15), –55 (16)	—	–60	—	–70	—	µA

continued...

(15) This value is only applicable for LVDS I/O bank.

(16) This value is only applicable for 3 V I/O bank.

Parameter	Symbol	Condition	V_{CCIO} (V)										Unit
			1.2		1.5		1.8		2.5		3.0		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Bus-hold, low, overdrive current	I_{ODL}	0 V < V_{IN} < V_{CCIO}	—	125	—	175	—	200	—	300	—	500	µA
Bus-hold, high, overdrive current	I_{ODH}	0 V < V_{IN} < V_{CCIO}	—	–125	—	–175	—	–200	—	–300	—	–500	µA
Bus-hold trip point	V_{TRIP}	—	0.3	0.9	0.38	1.13	0.68	1.07	0.70	1.7	0.8	2	V

OCT Calibration Accuracy Specifications

If you enable on-chip termination (OCT) calibration, calibration is automatically performed at power up for I/Os connected to the calibration block.

Table 7. OCT Calibration Accuracy Specifications for Intel Cyclone 10 GX Devices

Calibration accuracy for the calibrated on-chip series termination (R_S OCT) and on-chip parallel termination (R_T OCT) are applicable at the moment of calibration. When process, voltage, and temperature (PVT) conditions change after calibration, the tolerance may change.

Symbol	Description	Condition (V)	Resistance Tolerance		Unit
			–E5, –I5	–E6, –I6	
25-Ω and 50-Ω R_S	Internal series termination with calibration (25-Ω and 50-Ω setting)	V_{CCIO} = 1.8, 1.5, 1.2	± 15	± 15	%
34-Ω and 40-Ω R_S	Internal series termination with calibration (34-Ω and 40-Ω setting)	V_{CCIO} = 1.5, 1.25, 1.2	± 15	± 15	%
		V_{CCIO} = 1.35	± 20	± 20	%
48-Ω, 60-Ω, 80-Ω, and 120-Ω R_S	Internal series termination with calibration (48-Ω, 60-Ω, 80-Ω, and 120-Ω setting)	V_{CCIO} = 1.2	± 15	± 15	%
240-Ω R_S	Internal series termination with calibration (240-Ω setting)	V_{CCIO} = 1.2	± 20	± 20	%
30-Ω R_T	Internal parallel termination with calibration (30-Ω setting)	V_{CCIO} = 1.5, 1.35, 1.25	–10 to +40	–10 to +40	%
34-Ω, 48-Ω, 80-Ω, and 240-Ω R_T	Internal parallel termination with calibration (34-Ω, 48-Ω, 80-Ω, and 240-Ω setting)	V_{CCIO} = 1.2	± 15	± 15	%

continued...

I/O Standard	V_{CCIO} (V)			$V_{SWING(DC)}$ (V)		$V_{SWING(AC)}$ (V)		$V_{IX(AC)}$ (V)		
	Min	Typ	Max	Min	Max	Min	Max	Min	Typ	Max
SSTL-135/ SSTL-135 Class I, II	1.283	1.35	1.45	0.18	(22)	$2(V_{IH(AC)} - V_{REF})$	$2(V_{IL(AC)} - V_{REF})$	$V_{CCIO}/2 - 0.15$	$V_{CCIO}/2$	$V_{CCIO}/2 + 0.15$
SSTL-125/ SSTL-125 Class I, II	1.19	1.25	1.31	0.18	(22)	$2(V_{IH(AC)} - V_{REF})$	$2(V_{IL(AC)} - V_{REF})$	$V_{CCIO}/2 - 0.15$	$V_{CCIO}/2$	$V_{CCIO}/2 + 0.15$
SSTL-12/ SSTL-12 Class I, II	1.14	1.2	1.26	0.16	(22)	$2(V_{IH(AC)} - V_{REF})$	$2(V_{IL(AC)} - V_{REF})$	$V_{REF} - 0.15$	$V_{CCIO}/2$	$V_{REF} + 0.15$
POD12	1.16	1.2	1.24	0.16	—	0.3	—	$V_{REF} - 0.08$	—	$V_{REF} + 0.08$

Differential HSTL and HSUL I/O Standards Specifications

Table 16. Differential HSTL and HSUL I/O Standards Specifications for Intel Cyclone 10 GX Devices

I/O Standard	V_{CCIO} (V)			$V_{DIF(DC)}$ (V)		$V_{DIF(AC)}$ (V)		$V_{IX(AC)}$ (V)			$V_{CM(DC)}$ (V)		
	Min	Typ	Max	Min	Max	Min	Max	Min	Typ	Max	Min	Typ	Max
HSTL-18 Class I, II	1.71	1.8	1.89	0.2	—	0.4	—	0.78	—	1.12	0.78	—	1.12
HSTL-15 Class I, II	1.425	1.5	1.575	0.2	—	0.4	—	0.68	—	0.9	0.68	—	0.9
HSTL-12 Class I, II	1.14	1.2	1.26	0.16	$V_{CCIO} + 0.3$	0.3	$V_{CCIO} + 0.48$	—	$0.5 \times V_{CCIO}$	—	$0.4 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.6 \times V_{CCIO}$
HSUL-12	1.14	1.2	1.3	$2(V_{IH(DC)} - V_{REF})$	$2(V_{REF} - V_{IH(DC)})$	$2(V_{IH(AC)} - V_{REF})$	$2(V_{REF} - V_{IH(AC)})$	$0.5 \times V_{CCIO} - 0.12$	$0.5 \times V_{CCIO}$	$0.5 \times V_{CCIO} + 0.12$	$0.4 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.6 \times V_{CCIO}$

(22) The maximum value for $V_{SWING(DC)}$ is not defined. However, each single-ended signal needs to be within the respective single-ended limits ($V_{IH(DC)}$ and $V_{IL(DC)}$).

Table 25. Receiver Specifications

Symbol/Description	Condition	Min	Typ	Max	Unit
Supported I/O Standards	—	High Speed Differential I/O, CML , Differential LVPECL , and LVDS(35)			
Absolute V_{MAX} for a receiver pin (36)	—	—	—	1.2	V
Absolute V_{MIN} for a receiver pin (37)	—	-0.4	—	—	V
Maximum peak-to-peak differential input voltage V_{ID} (diff p-p) before device configuration	—	—	—	1.6	V
Maximum peak-to-peak differential input voltage V_{ID} (diff p-p) after device configuration	V_{CCR_GXB} = 0.95 V	—	—	2.4	V
	V_{CCR_GXB} = 1.03 V	—	—	2.0	V
Minimum differential eye opening at receiver serial input pins (38)	—	50	—	—	mV
Differential on-chip termination resistors	85-Ω setting	—	85 ± 30%	—	Ω
	100-Ω setting	—	100 ± 30%	—	Ω
V_{ICM} (AC and DC coupled) (39)	V_{CCR_GXB} = 0.95 V	—	600	—	mV
	V_{CCR_GXB} = 1.03 V	—	700	—	mV

continued...

(35) CML, Differential LVPECL, and LVDS are only used on AC coupled links.

(36) The device cannot tolerate prolonged operation at this absolute maximum.

(37) The device cannot tolerate prolonged operation at this absolute minimum.

(38) The differential eye opening specification at the receiver input pins assumes that Receiver Equalization is disabled. If you enable Receiver Equalization, the receiver circuitry can tolerate a lower minimum eye opening, depending on the equalization level.

(39) Intel Cyclone 10 GX devices support DC coupling to other Intel Cyclone 10 GX devices and other devices with a transmitter that has matching common mode voltage.

Symbol/Description	Condition	Min	Typ	Max	Unit
	100-Ω setting	—	100 ± 20%	—	Ω
V_{OCM} (AC coupled)	V_{CCT_GXB} = 0.95 V	—	450	—	mV
	V_{CCT_GXB} = 1.03 V	—	500	—	mV
V_{OCM} (DC coupled)	V_{CCT_GXB} = 0.95 V	—	450	—	mV
	V_{CCT_GXB} = 1.03 V	—	500	—	mV
Rise time (45)	20% to 80%	20	—	130	ps
Fall time (45)	80% to 20%	20	—	130	ps
Intra-differential pair skew	TX V_{CM} = 0.5 V and slew rate setting of SLEW_R5 (46)	—	—	15	ps

Table 27. Typical Transmitter V_{OD} Settings

Symbol	V_{OD} Setting	V_{OD}-to-V_{CCT_GXB} Ratio
V_{OD} differential value = V_{OD}-to-V_{CCT_GXB} ratio x V_{CCT_GXB}	31	1.00
	30	0.97
	29	0.93
	28	0.90
	27	0.87
	26	0.83
	25	0.80
	24	0.77
	23	0.73
	22	0.70

continued...

(45) The Intel Quartus Prime software automatically selects the appropriate slew rate depending on the design configurations.

(46) SLEW_R1 is the slowest and SLEW_R5 is the fastest. SLEW_R6 and SLEW_R7 are not used.

Core Performance Specifications

Clock Tree Specifications

Table 29. Clock Tree Performance for Intel Cyclone 10 GX Devices

Parameter	Performance (All Speed Grades)	Unit
Global clock, regional clock, and small periphery clock	644	MHz
Large periphery clock	525	MHz

PLL Specifications

Fractional PLL Specifications

Table 30. Fractional PLL Specifications for Intel Cyclone 10 GX Devices

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{IN}	Input clock frequency	—	30	—	800 (49)	MHz
f_{INPFD}	Input clock frequency to the phase frequency detector (PFD)	—	30	—	700	MHz
f_{CASC_INPFD}	Input clock frequency to the PFD of destination cascade PLL	—	30	—	60	MHz
f_{VCO}	PLL voltage-controlled oscillator (VCO) operating range	—	6	—	12.5	GHz
$t_{EINDUTY}$	Input clock duty cycle	—	45	—	55	%
f_{OUT}	Output frequency for internal global or regional clock	—	—	—	644	MHz
$f_{DYCONFIGCLK}$	Dynamic configuration clock for `reconfig_clk`	—	—	—	100	MHz

continued...

(49) This specification is limited by the I/O maximum frequency. The maximum achievable I/O frequency is different for each I/O standard and is depends on design and system specific factors. Ensure proper timing closure in your design and perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_{LOCK}	Time required to lock from end-of-device configuration or deassertion of `pll_powerdown`	—	—	—	1	ms
t_{DLOCK}	Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays)	—	—	—	1	ms
f_{CLBW}	PLL closed-loop bandwidth	—	0.3	—	4	MHz
t_{PLL_PSERR}	Accuracy of PLL phase shift	—	—	—	50	ps
t_{ARESET}	Minimum pulse width on the `pll_powerdown` signal	—	10	—	—	ns
t_{INCCJ} (50)(51)	Input clock cycle-to-cycle jitter	$F_{REF} \geq 100$ MHz	—	—	0.13	UI (p-p)
		$F_{REF} < 100$ MHz	—	—	650	ps (p-p)
t_{OUTPJ} (52)	Period jitter for clock output	$F_{OUT} \geq 100$ MHz	—	—	600	ps (p-p)
		$F_{OUT} < 100$ MHz	—	—	60	mUI (p-p)
t_{OUTCCJ} (52)	Cycle-to-cycle jitter for clock output	$F_{OUT} \geq 100$ MHz	—	—	600	ps (p-p)
		$F_{OUT} < 100$ MHz	—	—	60	mUI (p-p)
dK_{BIT}	Bit number of Delta Sigma Modulator (DSM)	—	—	32	—	bit

Related Information

Memory Output Clock Jitter Specifications on page 43
Provides more information about the external memory interface clock output jitter specifications.

(50) A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source with jitter < 120 ps.

(51) F_{REF} is f_{IN}/N, specification applies when $N = 1$.

(52) External memory interface clock output jitter specifications use a different measurement method, which are available in Memory Output Clock Jitter Specification for Intel Cyclone 10 GX Devices table.

I/O PLL Specifications

Table 31. I/O PLL Specifications for Intel Cyclone 10 GX Devices

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{IN}	Input clock frequency	–5 speed grade	10	—	700 (53)	MHz
		–6 speed grade	10	—	650 (53)	MHz
f_{INPFD}	Input clock frequency to the PFD	—	10	—	325	MHz
f_{CASC_INPFD}	Input clock frequency to the PFD of destination cascade PLL	—	10	—	60	MHz
f_{VCO}	PLL VCO operating range	–5 speed grade	600	—	1434	MHz
		–6 speed grade	600	—	1250	MHz
f_{CLBW}	PLL closed-loop bandwidth	—	0.1	—	8	MHz
$t_{EINDUTY}$	Input clock or external feedback clock input duty cycle	—	40	—	60	%
f_{OUT}	Output frequency for internal global or regional clock (C counter)	–5, –6 speed grade	—	—	644	MHz
f_{OUT_EXT}	Output frequency for external clock output	–5 speed grade	—	—	720	MHz
		–6 speed grade	—	—	650	MHz
$t_{OUTDUTY}$	Duty cycle for dedicated external clock output (when set to 50%)	—	45	50	55	%
t_{FCOMP}	External feedback clock compensation time	—	—	—	10	ns
$f_{DYCONFIGCLK}$	Dynamic configuration clock for `mgmt_clk` and `scanclk`	—	—	—	100	MHz
t_{LOCK}	Time required to lock from end-of-device configuration or deassertion of `areset`	—	—	—	1	ms

continued...

(53) This specification is limited by the I/O maximum frequency. The maximum achievable I/O frequency is different for each I/O standard and is depends on design and system specific factors. Ensure proper timing closure in your design and perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

DPA Lock Time Specifications

Figure 2. DPA Lock Time Specifications with DPA PLL Calibration Enabled

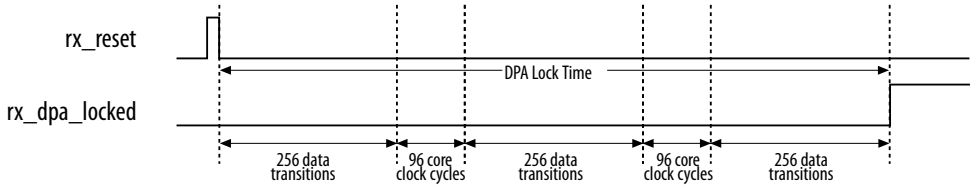


Table 38. DPA Lock Time Specifications for Intel Cyclone 10 GX Devices

The specifications are applicable to both extended and industrial grades. The DPA lock time is for one channel. One data transition is defined as a 0-to-1 or 1-to-0 transition.

Standard	Training Pattern	Number of Data Transitions in One Repetition of the Training Pattern	Number of Repetitions per 256 Data Transitions (67)	Maximum Data Transition
SPI-4	00000000001111111111	2	128	640
Parallel Rapid I/O	00001111	2	128	640
	10010000	4	64	640
Miscellaneous	10101010	8	32	640
	01010101	8	32	640

(67) This is the number of repetitions for the stated training pattern to achieve the 256 data transitions.

LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specifications

Figure 3. LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specifications for a Data Rate Equal to 1.4 Gbps

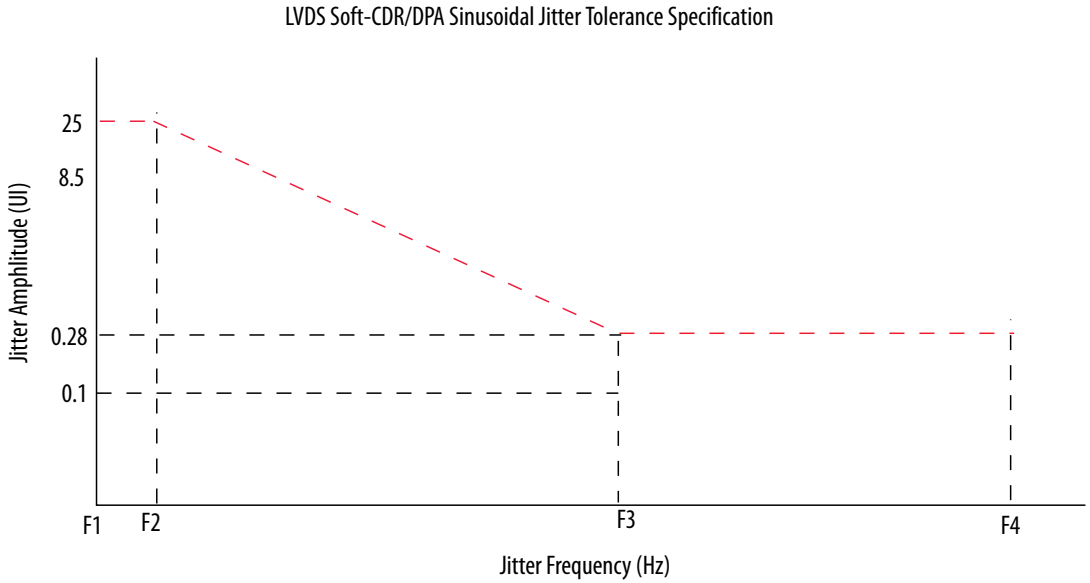


Table 39. LVDS Soft-CDR/DPA Sinusoidal Jitter Mask Values for a Data Rate Equal to 1.4 Gbps

Jitter Frequency (Hz)		Sinusoidal Jitter (UI)
F1	10,000	25.00
F2	17,565	25.00
F3	1,493,000	0.28
F4	50,000,000	0.28

DQS Logic Block Specifications

Table 42. DQS Phase Shift Error Specifications for DLL-Delayed Clock (t_{DQS_PSERR}) for Intel Cyclone 10 GX Devices

This error specification is the absolute maximum and minimum error.

Symbol	Performance (for All Speed Grades)	Unit
t_{DQS_PSERR}	5	ps

Memory Output Clock Jitter Specifications

Table 43. Memory Output Clock Jitter Specifications for Intel Cyclone 10 GX Devices

The clock jitter specification applies to the memory output clock pins clocked by an I/O PLL, or generated using differential signal-splitter and double data I/O circuits clocked by a PLL output routed on a PHY clock network as specified. Intel recommends using PHY clock networks for better jitter performance.

The memory output clock jitter is applicable when an input jitter of 10 ps peak-to-peak is applied with bit error rate (BER) 10^{-12}, equivalent to 14 sigma.

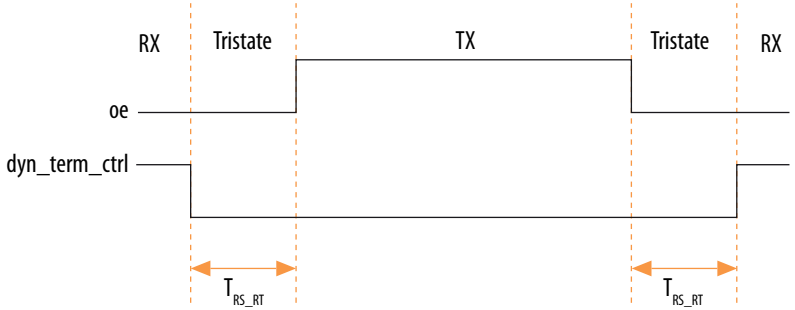
Protocol	Parameter	Symbol	Data Rate (Mbps)	Min	Max	Unit
DDR3	Clock period jitter	$t_{JIT(per)}$	1,866	–40	40	ps
	Cycle-to-cycle period jitter	$t_{JIT(cc)}$	1,866	–40	40	ps
	Duty cycle jitter	$t_{JIT(duty)}$	1,866	–40	40	ps

OCT Calibration Block Specifications

Table 44. OCT Calibration Block Specifications for Intel Cyclone 10 GX Devices

Symbol	Description	Min	Typ	Max	Unit
OCTUSRCLK	Clock required by OCT calibration blocks	—	—	20	MHz
T_{OCTCAL}	Number of OCTUSRCLK clock cycles required for R_S OCT /R_T OCT calibration	> 2000	—	—	Cycles
$T_{OCTSHIFT}$	Number of OCTUSRCLK clock cycles required for OCT code to shift out	—	32	—	Cycles
T_{RS_RT}	Time required between the `dyn_term_ctrl` and `oe` signal transitions in a bidirectional I/O buffer to dynamically switch between R_S OCT and R_T OCT	—	2.5	—	ns

Figure 5. Timing Diagram for on oe and dyn_term_ctrl Signals



Configuration Specifications

This section provides configuration specifications and timing for Intel Cyclone 10 GX devices.

POR Specifications

Power-on reset (POR) delay is defined as the delay between the time when all the power supplies monitored by the POR circuitry reach the minimum recommended operating voltage to the time when the nSTATUS is released high and your device is ready to begin configuration.

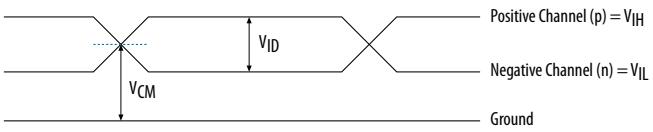
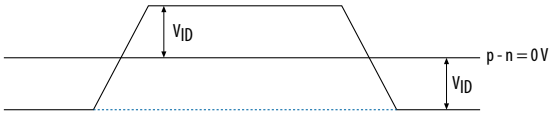
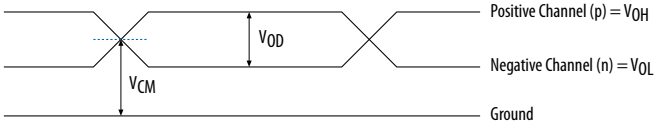
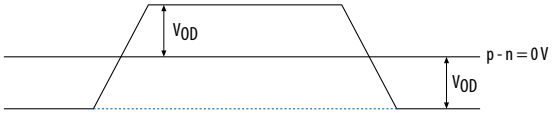
Table 45. Fast and Standard POR Delay Specification for Intel Cyclone 10 GX Devices

POR Delay	Minimum	Maximum	Unit
Fast	4	12 (68)	ms
Standard	100	300	ms

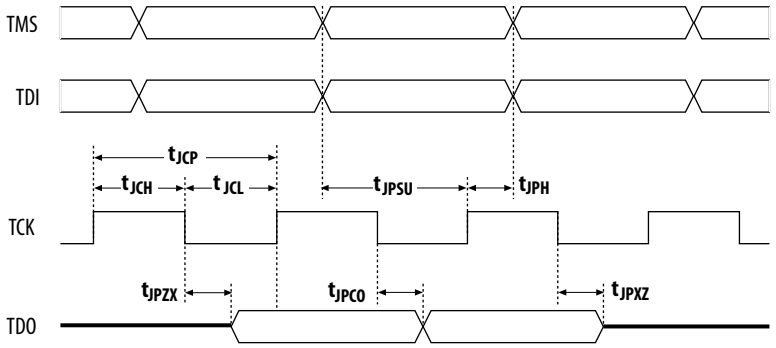
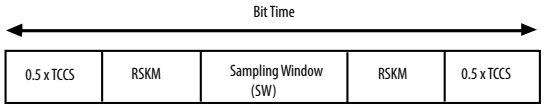
Related Information

MSEL Pin Settings
Provides more information about POR delay based on MSEL pin settings for each configuration scheme.

(68) The maximum pulse width of the fast POR delay is 12 ms, providing enough time for the PCIe hard IP to initialize after the POR trip.

Term	Definition
	Single-Ended Waveform  **Differential Waveform**  Transmitter Output Waveforms **Single-Ended Waveform**  **Differential Waveform** 
f_{HSCLK}	I/O PLL input clock frequency.
f_{HSDR}	High-speed I/O block—Maximum/minimum LVDS data transfer rate (f_{HSDR} = 1/TUI), non-DPA.
$f_{HSDRDPA}$	High-speed I/O block—Maximum/minimum LVDS data transfer rate ($f_{HSDRDPA}$ = 1/TUI), DPA.
J	High-speed I/O block—Deserialization factor (width of parallel data bus).
JTAG Timing Specifications	JTAG Timing Specifications:

continued...

Term	Definition
	
R_L	Receiver differential input discrete resistor (external to the Intel Cyclone 10 GX device).
Sampling window (SW)	Timing Diagram—the period of time during which the data must be valid in order to capture it correctly. The setup and hold times determine the ideal strobe position in the sampling window, as shown: 
Single-ended voltage referenced I/O standard	The JEDEC standard for the SSTL and HSTL I/O defines both the AC and DC input signal values. The AC values indicate the voltage levels at which the receiver must meet its timing specifications. The DC values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. After the receiver input has crossed the AC value, the receiver changes to the new logic state. The new logic state is then maintained as long as the input stays beyond the DC threshold. This approach is intended to provide predictable receiver timing in the presence of input waveform ringing. Single-Ended Voltage Referenced I/O Standard

continued...