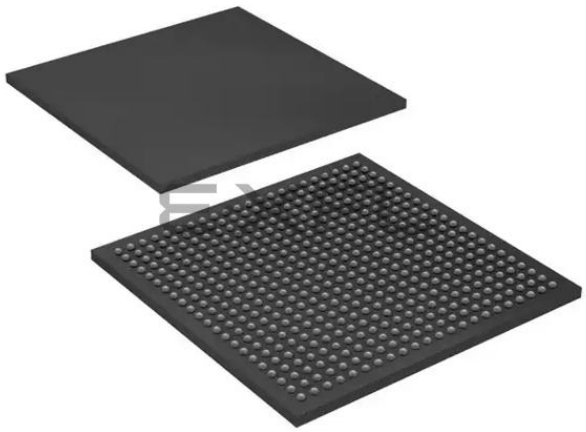

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	80330
Number of Logic Elements/Cells	220000
Total RAM Bits	13752320
Number of I/O	188
Number of Gates	-
Voltage - Supply	0.9V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	484-BFBGA
Supplier Device Package	484-UBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/intel/10cx220yu484i6g

Symbol	Description	Condition	Minimum	Maximum	Unit
I_{OUT}	DC output current per pin	—	−25 (2)(3)(4)(5)(6)	25	mA
T_J	Operating junction temperature	—	−55	125	°C
T_{STG}	Storage temperature (no bias)	—	−65	150	°C

Related Information

- AN 692: Power Sequencing Considerations for Intel Cyclone 10 GX, Intel Arria 10, and Intel Stratix 10 Devices
  Provides the power sequencing requirements for Intel Cyclone 10 GX devices.
- Power-Up and Power-Down Sequences, Power Management in Intel Cyclone 10 GX Devices chapter
  Provides the power sequencing requirements for Intel Cyclone 10 GX devices.

Maximum Allowed Overshoot and Undershoot Voltage

During transitions, input signals may overshoot to the voltage listed in the following table and undershoot to −2.0 V for input currents less than 100 mA and periods shorter than 20 ns.

The maximum allowed overshoot duration is specified as a percentage of high time over the lifetime of the device. A DC signal is equivalent to 100% duty cycle.

For example, a signal that overshoots to 2.70 V for LVDS I/O can only be at 2.70 V for ~4% over the lifetime of the device.

---

(2) The maximum current allowed through any LVDS I/O bank pin when the device is not turned on or during power-up/power-down conditions is 10 mA.

(3) Total current per LVDS I/O bank must not exceed 100 mA.

(4) Voltage level must not exceed 1.89 V.

(5) Applies to all I/O standards and settings supported by LVDS I/O banks, including single-ended and differential I/Os.

(6) Applies only to LVDS I/O banks. 3 V I/O banks are not covered under this specification and must be implemented as per the power sequencing requirement. For more details, refer to *AN 692: Power Sequencing Considerations for Intel Cyclone 10 GX, Intel Arria® 10, and Intel Stratix® 10 Devices* and *Power Management in Intel Cyclone 10 GX Devices chapter*.

Table 2. Maximum Allowed Overshoot During Transitions for Intel Cyclone 10 GX Devices

This table lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage of device lifetime. The LVDS I/O values are applicable to the VREFP_ADC and VREFN_ADC I/O pins.

Symbol	Description	Condition (V)		Overshoot Duration as % at T_J = 100°C	Unit
		LVDS I/O (7)	3 V I/O		
V_i (AC)	AC input voltage	2.50	3.80	100	%
		2.55	3.85	42	%
		2.60	3.90	18	%
		2.65	3.95	9	%
		2.70	4.00	4	%
		> 2.70	> 4.00	No overshoot allowed	%

For an overshoot of 2.5 V, the percentage of high time for the overshoot can be as high as 100% over a 10-year period. Percentage of high time is calculated as ([delta T]/T) × 100. This 10-year period assumes that the device is always turned on with 100% I/O toggle rate and 50% duty cycle signal.

(7) The LVDS I/O values are applicable to all dedicated and dual-function configuration I/Os.

Parameter	Symbol	Condition	V_{CCIO} (V)										Unit
			1.2		1.5		1.8		2.5		3.0		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Bus-hold, low, overdrive current	I_{ODL}	0 V < V_{IN} < V_{CCIO}	—	125	—	175	—	200	—	300	—	500	µA
Bus-hold, high, overdrive current	I_{ODH}	0 V < V_{IN} < V_{CCIO}	—	–125	—	–175	—	–200	—	–300	—	–500	µA
Bus-hold trip point	V_{TRIP}	—	0.3	0.9	0.38	1.13	0.68	1.07	0.70	1.7	0.8	2	V

OCT Calibration Accuracy Specifications

If you enable on-chip termination (OCT) calibration, calibration is automatically performed at power up for I/Os connected to the calibration block.

Table 7. OCT Calibration Accuracy Specifications for Intel Cyclone 10 GX Devices

Calibration accuracy for the calibrated on-chip series termination (R_S OCT) and on-chip parallel termination (R_T OCT) are applicable at the moment of calibration. When process, voltage, and temperature (PVT) conditions change after calibration, the tolerance may change.

Symbol	Description	Condition (V)	Resistance Tolerance		Unit
			–E5, –I5	–E6, –I6	
25-Ω and 50-Ω R_S	Internal series termination with calibration (25-Ω and 50-Ω setting)	V_{CCIO} = 1.8, 1.5, 1.2	± 15	± 15	%
34-Ω and 40-Ω R_S	Internal series termination with calibration (34-Ω and 40-Ω setting)	V_{CCIO} = 1.5, 1.25, 1.2	± 15	± 15	%
		V_{CCIO} = 1.35	± 20	± 20	%
48-Ω, 60-Ω, 80-Ω, and 120-Ω R_S	Internal series termination with calibration (48-Ω, 60-Ω, 80-Ω, and 120-Ω setting)	V_{CCIO} = 1.2	± 15	± 15	%
240-Ω R_S	Internal series termination with calibration (240-Ω setting)	V_{CCIO} = 1.2	± 20	± 20	%
30-Ω R_T	Internal parallel termination with calibration (30-Ω setting)	V_{CCIO} = 1.5, 1.35, 1.25	–10 to +40	–10 to +40	%
34-Ω, 48-Ω, 80-Ω, and 240-Ω R_T	Internal parallel termination with calibration (34-Ω, 48-Ω, 80-Ω, and 240-Ω setting)	V_{CCIO} = 1.2	± 15	± 15	%

continued...

Symbol	Description	Condition (V)	Resistance Tolerance		Unit
			–E5, –I5	–E6, –I6	
40-Ω, 60-Ω, and 120-Ω R_T	Internal parallel termination with calibration (40-Ω, 60-Ω, and 120-Ω setting)	V_{CCIO} = 1.5, 1.35, 1.25, 1.2	–10 to +40	–10 to +40	%
		V_{CCIO} = 1.2 (17)	± 15	± 15	%
80-Ω R_T	Internal parallel termination with calibration (80-Ω setting)	V_{CCIO} = 1.2	± 15	± 15	%

Related Information

I/O Standards Support in Intel Cyclone 10 GX Devices

OCT Without Calibration Resistance Tolerance Specifications

Table 8. OCT Without Calibration Resistance Tolerance Specifications for Intel Cyclone 10 GX Devices

This table lists the Intel Cyclone 10 GX OCT without calibration resistance tolerance to PVT changes.

Symbol	Description	Condition (V)	Resistance Tolerance		Unit
			–E5, –I5	–E6, –I6	
25-Ω and 50-Ω R_S	Internal series termination without calibration (25-Ω and 50-Ω setting)	V_{CCIO} = 3.0, 2.5	± 40	± 40	%
		V_{CCIO} = 1.8, 1.5, 1.2	± 50	± 50	%
34-Ω and 40-Ω R_S	Internal series termination without calibration (34-Ω and 40-Ω setting)	V_{CCIO} = 1.5, 1.35, 1.25, 1.2	± 50	± 50	%
48-Ω and 60-Ω R_S	Internal series termination without calibration (48-Ω and 60-Ω setting)	V_{CCIO} = 1.2	± 50	± 50	%
120-Ω R_s	Internal series termination without calibration (120-Ω setting)	V_{CCIO} = 1.2	± 50	± 50	%
100-Ω R_D	Internal differential termination (100-Ω setting)	V_{CCIO} = 1.8	± 35	± 40	%

(17) Only applicable to POD12 I/O standard.

I/O Standard	V_{CCIO} (V)			$V_{SWING(DC)}$ (V)		$V_{SWING(AC)}$ (V)		$V_{IX(AC)}$ (V)		
	Min	Typ	Max	Min	Max	Min	Max	Min	Typ	Max
SSTL-135/ SSTL-135 Class I, II	1.283	1.35	1.45	0.18	(22)	$2(V_{IH(AC)} - V_{REF})$	$2(V_{IL(AC)} - V_{REF})$	$V_{CCIO}/2 - 0.15$	$V_{CCIO}/2$	$V_{CCIO}/2 + 0.15$
SSTL-125/ SSTL-125 Class I, II	1.19	1.25	1.31	0.18	(22)	$2(V_{IH(AC)} - V_{REF})$	$2(V_{IL(AC)} - V_{REF})$	$V_{CCIO}/2 - 0.15$	$V_{CCIO}/2$	$V_{CCIO}/2 + 0.15$
SSTL-12/ SSTL-12 Class I, II	1.14	1.2	1.26	0.16	(22)	$2(V_{IH(AC)} - V_{REF})$	$2(V_{IL(AC)} - V_{REF})$	$V_{REF} - 0.15$	$V_{CCIO}/2$	$V_{REF} + 0.15$
POD12	1.16	1.2	1.24	0.16	—	0.3	—	$V_{REF} - 0.08$	—	$V_{REF} + 0.08$

Differential HSTL and HSUL I/O Standards Specifications

Table 16. Differential HSTL and HSUL I/O Standards Specifications for Intel Cyclone 10 GX Devices

I/O Standard	V_{CCIO} (V)			$V_{DIF(DC)}$ (V)		$V_{DIF(AC)}$ (V)		$V_{IX(AC)}$ (V)			$V_{CM(DC)}$ (V)		
	Min	Typ	Max	Min	Max	Min	Max	Min	Typ	Max	Min	Typ	Max
HSTL-18 Class I, II	1.71	1.8	1.89	0.2	—	0.4	—	0.78	—	1.12	0.78	—	1.12
HSTL-15 Class I, II	1.425	1.5	1.575	0.2	—	0.4	—	0.68	—	0.9	0.68	—	0.9
HSTL-12 Class I, II	1.14	1.2	1.26	0.16	$V_{CCIO} + 0.3$	0.3	$V_{CCIO} + 0.48$	—	$0.5 \times V_{CCIO}$	—	$0.4 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.6 \times V_{CCIO}$
HSUL-12	1.14	1.2	1.3	$2(V_{IH(DC)} - V_{REF})$	$2(V_{REF} - V_{IH(DC)})$	$2(V_{IH(AC)} - V_{REF})$	$2(V_{REF} - V_{IH(AC)})$	$0.5 \times V_{CCIO} - 0.12$	$0.5 \times V_{CCIO}$	$0.5 \times V_{CCIO} + 0.12$	$0.4 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.6 \times V_{CCIO}$

(22) The maximum value for $V_{SWING(DC)}$ is not defined. However, each single-ended signal needs to be within the respective single-ended limits ($V_{IH(DC)}$ and $V_{IL(DC)}$).

Table 25. Receiver Specifications

Symbol/Description	Condition	Min	Typ	Max	Unit
Supported I/O Standards	—	High Speed Differential I/O, CML , Differential LVPECL , and LVDS(35)			
Absolute V_{MAX} for a receiver pin (36)	—	—	—	1.2	V
Absolute V_{MIN} for a receiver pin (37)	—	-0.4	—	—	V
Maximum peak-to-peak differential input voltage V_{ID} (diff p-p) before device configuration	—	—	—	1.6	V
Maximum peak-to-peak differential input voltage V_{ID} (diff p-p) after device configuration	V_{CCR_GXB} = 0.95 V	—	—	2.4	V
	V_{CCR_GXB} = 1.03 V	—	—	2.0	V
Minimum differential eye opening at receiver serial input pins (38)	—	50	—	—	mV
Differential on-chip termination resistors	85-Ω setting	—	85 ± 30%	—	Ω
	100-Ω setting	—	100 ± 30%	—	Ω
V_{ICM} (AC and DC coupled) (39)	V_{CCR_GXB} = 0.95 V	—	600	—	mV
	V_{CCR_GXB} = 1.03 V	—	700	—	mV

continued...

(35) CML, Differential LVPECL, and LVDS are only used on AC coupled links.

(36) The device cannot tolerate prolonged operation at this absolute maximum.

(37) The device cannot tolerate prolonged operation at this absolute minimum.

(38) The differential eye opening specification at the receiver input pins assumes that Receiver Equalization is disabled. If you enable Receiver Equalization, the receiver circuitry can tolerate a lower minimum eye opening, depending on the equalization level.

(39) Intel Cyclone 10 GX devices support DC coupling to other Intel Cyclone 10 GX devices and other devices with a transmitter that has matching common mode voltage.

Symbol/Description	Condition	Min	Typ	Max	Unit
t_{LTR} (40)	—	—	—	10	µs
t_{LTD} (41)	—	4	—	—	µs
t_{LTD_manual} (42)	—	4	—	—	µs
$t_{LTR\_LTD\_manual}$ (43)	—	15	—	—	µs
Run Length	—	—	—	200	UI
CDR PPM tolerance	PCIe-only	-300	—	300	PPM
	All other protocols	-1000	—	1000	PPM
Programmable DC Gain	Setting = 0-4	0	—	10	dB
Programmable AC Gain at High Gain mode and Data Rate ≤ 6 Gbps	Setting = 0-28 V_{CCR_GXB} = 0.95 V	0	—	19	dB
	Setting = 0-28 V_{CCR_GXB} = 1.03 V	0	—	21	dB

Table 26. Transmitter Specifications

Symbol/Description	Condition	Min	Typ	Max	Unit
Supported I/O Standards	—	High Speed Differential I/O (44)			—
Differential on-chip termination resistors	85-Ω setting	—	85 ± 20%	—	Ω

continued...

(40) t_{LTR} is the time required for the receive CDR to lock to the input reference clock frequency after coming out of reset.

(41) t_{LTD} is time required for the receiver CDR to start recovering valid data after the `rx_is_lockedtodata` signal goes high.

(42) t_{LTD_manual} is the time required for the receiver CDR to start recovering valid data after the `rx_is_lockedtodata` signal goes high when the CDR is functioning in the manual mode.

(43) $t_{LTR\_LTD\_manual}$ is the time the receiver CDR must be kept in lock to reference (LTR) mode after the `rx_is_lockedtoref` signal goes high when the CDR is functioning in the manual mode.

(44) High Speed Differential I/O is the dedicated I/O standard for the transmitter in Intel Cyclone 10 GX transceivers.

Symbol/Description	Condition	Min	Typ	Max	Unit
	100-Ω setting	—	100 ± 20%	—	Ω
V_{OCM} (AC coupled)	V_{CCT_GXB} = 0.95 V	—	450	—	mV
	V_{CCT_GXB} = 1.03 V	—	500	—	mV
V_{OCM} (DC coupled)	V_{CCT_GXB} = 0.95 V	—	450	—	mV
	V_{CCT_GXB} = 1.03 V	—	500	—	mV
Rise time (45)	20% to 80%	20	—	130	ps
Fall time (45)	80% to 20%	20	—	130	ps
Intra-differential pair skew	TX V_{CM} = 0.5 V and slew rate setting of SLEW_R5 (46)	—	—	15	ps

Table 27. Typical Transmitter V_{OD} Settings

Symbol	V_{OD} Setting	V_{OD}-to-V_{CCT_GXB} Ratio
V_{OD} differential value = V_{OD}-to-V_{CCT_GXB} ratio x V_{CCT_GXB}	31	1.00
	30	0.97
	29	0.93
	28	0.90
	27	0.87
	26	0.83
	25	0.80
	24	0.77
	23	0.73
	22	0.70

continued...

(45) The Intel Quartus Prime software automatically selects the appropriate slew rate depending on the design configurations.

(46) SLEW_R1 is the slowest and SLEW_R5 is the fastest. SLEW_R6 and SLEW_R7 are not used.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_{LOCK}	Time required to lock from end-of-device configuration or deassertion of `pll_powerdown`	—	—	—	1	ms
t_{DLOCK}	Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays)	—	—	—	1	ms
f_{CLBW}	PLL closed-loop bandwidth	—	0.3	—	4	MHz
t_{PLL_PSERR}	Accuracy of PLL phase shift	—	—	—	50	ps
t_{ARESET}	Minimum pulse width on the `pll_powerdown` signal	—	10	—	—	ns
t_{INCCJ} (50)(51)	Input clock cycle-to-cycle jitter	$F_{REF} \geq 100$ MHz	—	—	0.13	UI (p-p)
		$F_{REF} < 100$ MHz	—	—	650	ps (p-p)
t_{OUTPJ} (52)	Period jitter for clock output	$F_{OUT} \geq 100$ MHz	—	—	600	ps (p-p)
		$F_{OUT} < 100$ MHz	—	—	60	mUI (p-p)
t_{OUTCCJ} (52)	Cycle-to-cycle jitter for clock output	$F_{OUT} \geq 100$ MHz	—	—	600	ps (p-p)
		$F_{OUT} < 100$ MHz	—	—	60	mUI (p-p)
dK_{BIT}	Bit number of Delta Sigma Modulator (DSM)	—	—	32	—	bit

Related Information

Memory Output Clock Jitter Specifications on page 43
Provides more information about the external memory interface clock output jitter specifications.

(50) A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source with jitter < 120 ps.

(51) F_{REF} is f_{IN}/N, specification applies when $N = 1$.

(52) External memory interface clock output jitter specifications use a different measurement method, which are available in Memory Output Clock Jitter Specification for Intel Cyclone 10 GX Devices table.

I/O PLL Specifications

Table 31. I/O PLL Specifications for Intel Cyclone 10 GX Devices

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{IN}	Input clock frequency	–5 speed grade	10	—	700 (53)	MHz
		–6 speed grade	10	—	650 (53)	MHz
f_{INPFD}	Input clock frequency to the PFD	—	10	—	325	MHz
f_{CASC_INPFD}	Input clock frequency to the PFD of destination cascade PLL	—	10	—	60	MHz
f_{VCO}	PLL VCO operating range	–5 speed grade	600	—	1434	MHz
		–6 speed grade	600	—	1250	MHz
f_{CLBW}	PLL closed-loop bandwidth	—	0.1	—	8	MHz
$t_{EINDUTY}$	Input clock or external feedback clock input duty cycle	—	40	—	60	%
f_{OUT}	Output frequency for internal global or regional clock (C counter)	–5, –6 speed grade	—	—	644	MHz
f_{OUT_EXT}	Output frequency for external clock output	–5 speed grade	—	—	720	MHz
		–6 speed grade	—	—	650	MHz
$t_{OUTDUTY}$	Duty cycle for dedicated external clock output (when set to 50%)	—	45	50	55	%
t_{FCOMP}	External feedback clock compensation time	—	—	—	10	ns
$f_{DYCONFIGCLK}$	Dynamic configuration clock for `mgmt_clk` and `scanclk`	—	—	—	100	MHz
t_{LOCK}	Time required to lock from end-of-device configuration or deassertion of `areset`	—	—	—	1	ms

continued...

(53) This specification is limited by the I/O maximum frequency. The maximum achievable I/O frequency is different for each I/O standard and is depends on design and system specific factors. Ensure proper timing closure in your design and perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

DSP Block Specifications

Table 32. DSP Block Performance Specifications for Intel Cyclone 10 GX Devices

Mode	Performance				Unit
	–E5	–I5	–E6	–I6	
Fixed-point 18 × 19 multiplication mode	456	438	364	346	MHz
Fixed-point 27 × 27 multiplication mode	450	434	358	344	MHz
Fixed-point 18 × 18 multiplier adder mode	459	440	370	351	MHz
Fixed-point 18 × 18 multiplier adder summed with 36-bit input mode	444	422	349	326	MHz
Fixed-point 18 × 19 systolic mode	459	440	370	351	MHz
Complex 18 × 19 multiplication mode	456	438	364	346	MHz
Floating point multiplication mode	447	427	347	326	MHz
Floating point adder or subtract mode	388	369	288	266	MHz
Floating point multiplier adder or subtract mode	386	368	290	270	MHz
Floating point multiplier accumulate mode	418	393	326	294	MHz
Floating point vector one mode	404	382	306	282	MHz
Floating point vector two mode	383	367	293	278	MHz

Memory Block Specifications

To achieve the maximum memory block performance, use a memory block clock that comes through global clock routing from an on-chip PLL and set to **50%** output duty cycle. Use the Intel Quartus Prime software to report timing for the memory block clocking schemes.

When you use the error detection cyclical redundancy check (CRC) feature, there is no degradation in f_{MAX}.

External Temperature Sensing Diode Specifications

Table 35. External Temperature Sensing Diode Specifications for Intel Cyclone 10 GX Devices

- The typical value is at 25°C.
- Diode accuracy improves with lower injection current.
- Absolute accuracy is dependent on third party external diode ADC and integration specifics.

Description	Min	Typ	Max	Unit
I_{bias}, diode source current	10	—	100	µA
V_{bias}, voltage across diode	0.3	—	0.9	V
Series resistance	—	—	< 1	Ω
Diode ideality factor	—	1.03	—	—

Internal Voltage Sensor Specifications

Table 36. Internal Voltage Sensor Specifications for Intel Cyclone 10 GX Devices

Parameter		Minimum	Typical	Maximum	Unit
Resolution		—	—	6	Bit
Sampling rate		—	—	500	Ksps
Differential non-linearity (DNL)		—	—	±1	LSB
Integral non-linearity (INL)		—	—	±1	LSB
Gain error		—	—	±1	%
Offset error		—	—	±1	LSB
Input capacitance		—	20	—	pF
Clock frequency		0.1	—	11	MHz
Unipolar Input Mode	Input signal range for Vsigp	0	—	1.5	V
	Common mode voltage on Vsign	0	—	0.25	V
	Input signal range for Vsigp – Vsign	0	—	1.25	V

Symbol		Condition	–E5, –I5			–E6, –I6			Unit
			Min	Typ	Max	Min	Typ	Max	
	TCCS (64)(59)	True Differential I/O Standards	—	—	150	—	—	150	ps
Receiver	True Differential I/O Standards - $f_{HSDRDPA}$ (data rate)	SERDES factor J = 4 to 10 (60)(61)(62)	150	—	1434	150	—	1250	Mbps
		SERDES factor J = 3 (60)(61)(62)	150	—	1076	150	—	938	Mbps
	f_{HSDR} (data rate) (without DPA) (59)	SERDES factor J = 3 to 10	(62)	—	(66)	(62)	—	(66)	Mbps
		SERDES factor J = 2, uses DDR registers	(62)	—	(63)	(62)	—	(63)	Mbps
		SERDES factor J = 1, uses DDR registers	(62)	—	(63)	(62)	—	(63)	Mbps
DPA (FIFO mode)	DPA run length	—	—	—	10000	—	—	10000	UI
DPA (soft CDR mode)	DPA run length	SGMII/GbE protocol	—	—	5	—	—	5	UI
		All other protocols	—	—	50 data transition per 208 UI	—	—	50 data transition per 208 UI	—
Soft CDR mode	Soft-CDR ppm tolerance	—	—	—	300	—	—	300	± ppm
Non DPA mode	Sampling Window	—	—	—	300	—	—	300	ps

(65) This applies to default pre-emphasis and V_{OD} settings only.

(66) You can estimate the achievable maximum data rate for non-DPA mode by performing link timing closure analysis. You must consider the board skew margin, transmitter delay margin, and receiver sampling margin to determine the maximum data rate supported.

LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specifications

Figure 3. LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specifications for a Data Rate Equal to 1.4 Gbps

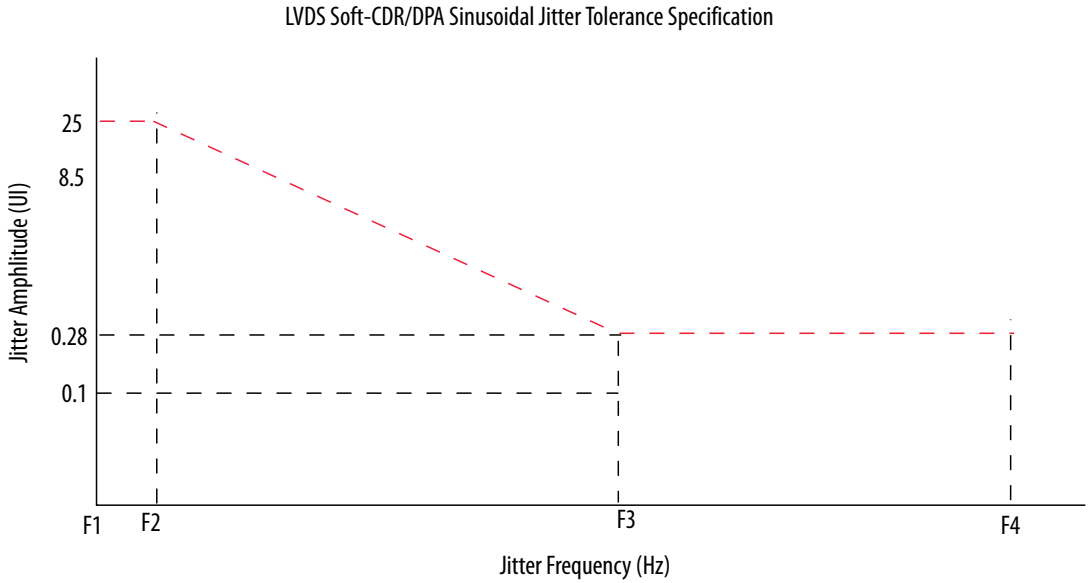
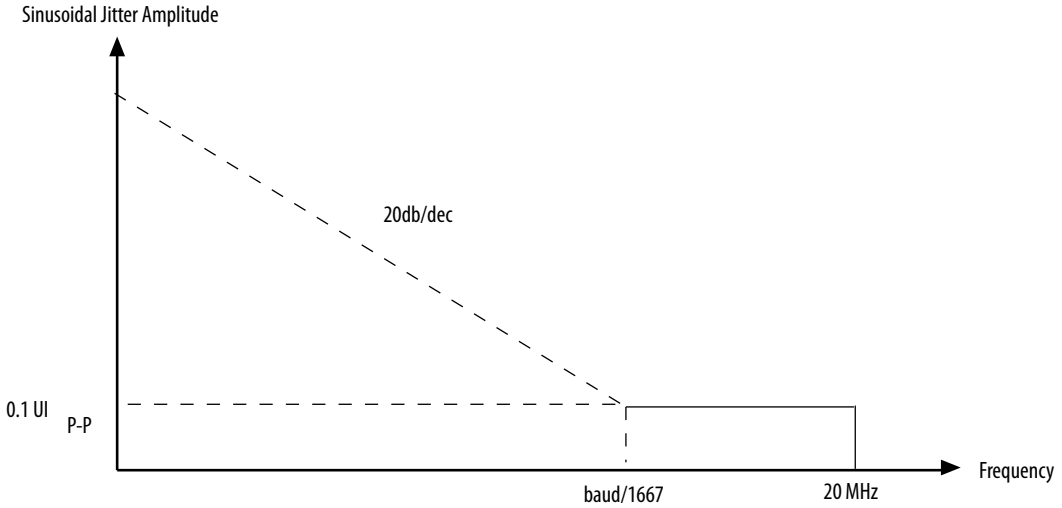


Table 39. LVDS Soft-CDR/DPA Sinusoidal Jitter Mask Values for a Data Rate Equal to 1.4 Gbps

Jitter Frequency (Hz)		Sinusoidal Jitter (UI)
F1	10,000	25.00
F2	17,565	25.00
F3	1,493,000	0.28
F4	50,000,000	0.28

Figure 4. LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specifications for a Data Rate Less than 1.4 Gbps



Memory Standards Supported by the Hard Memory Controller

Table 40. Memory Standards Supported by the Hard Memory Controller for Intel Cyclone 10 GX Devices

This table lists the overall capability of the hard memory controller. For specific details, refer to the External Memory Interface Spec Estimator.

Memory Standard	Rate Support	Speed Grade	Ping Pong PHY Support	Maximum Frequency (MHz)	
				I/O Bank	3 V I/O Bank
DDR3 SDRAM	Half rate	–5	Yes	533	225
			—	533	225
		–6	Yes	466	166
			—	466	166
	Quarter rate	–5	Yes	933	450
			—	933	450
		–6	Yes	933	333

continued...

Memory Standard	Rate Support	Speed Grade	Ping Pong PHY Support	Maximum Frequency (MHz)	
				I/O Bank	3 V I/O Bank
			—	933	333
DDR3L SDRAM	Half rate	–5	Yes	533	225
			—	533	225
		–6	Yes	466	166
			—	466	166
	Quarter rate	–5	Yes	933	450
			—	933	450
		–6	Yes	933	333
			—	933	333
LPDDR3 SDRAM	Half rate	–5	—	400	225
		–6	—	333	166
	Quarter rate	–5	—	800	450
		–6	—	666	333

Related Information

External Memory Interface Spec Estimator
Provides the specific details of the memory standards supported.

DLL Range Specifications

Table 41. DLL Frequency Range Specifications for Intel Cyclone 10 GX Devices

Intel Cyclone 10 GX devices support memory interface frequencies lower than 600 MHz, although the reference clock that feeds the DLL must be at least 600 MHz. To support interfaces below 600 MHz, multiply the reference clock feeding the DLL to ensure the frequency is within the supported range.

Parameter	Performance (for All Speed Grades)	Unit
DLL operating frequency range	600 – 1333	MHz

Symbol	Parameter	Minimum	Maximum	Unit
t_{CF2CK} (72)	nCONFIG high to first rising edge on DCLK	3,010	—	µs
t_{ST2CK} (72)	nSTATUS high to first rising edge of DCLK	10	—	µs
t_{DSU}	DATA[] setup time before rising edge on DCLK	5.5	—	ns
t_{DH}	DATA[] hold time after rising edge on DCLK	0	—	ns
t_{CH}	DCLK high time	0.45 × 1/f_{MAX}	—	s
t_{CL}	DCLK low time	0.45 × 1/f_{MAX}	—	s
t_{CLK}	DCLK period	1/f_{MAX}	—	s
f_{MAX}	DCLK frequency (FPP ×8/×16/×32)	—	100	MHz
t_{CD2UM}	CONF_DONE high to user mode (73)	175	830	µs
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period	—	—
t_{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t_{CD2CU} + (600 × CLKUSR period)	—	—

Related Information

FPP Configuration Timing
Provides the FPP configuration timing waveforms.

(71) This value is applicable if you do not delay configuration by externally holding the nSTATUS low.

(72) If nSTATUS is monitored, follow the t_{ST2CK} specification. If nSTATUS is not monitored, follow the t_{CF2CK} specification.

(73) The minimum and maximum numbers apply only if you chose the internal oscillator as the clock source for initializing the device.

Symbol	Parameter	Minimum	Maximum	Unit
t_{CF2CK} (80)	nCONFIG high to first rising edge on DCLK	3,010	—	µs
t_{ST2CK} (80)	nSTATUS high to first rising edge of DCLK	10	—	µs
t_{DSU}	DATA[] setup time before rising edge on DCLK	5.5	—	ns
t_{DH}	DATA[] hold time after rising edge on DCLK	0	—	ns
t_{CH}	DCLK high time	0.45 × 1/f_{MAX}	—	s
t_{CL}	DCLK low time	0.45 × 1/f_{MAX}	—	s
t_{CLK}	DCLK period	1/f_{MAX}	—	s
f_{MAX}	DCLK frequency	—	125	MHz
t_{CD2UM}	CONF_DONE high to user mode (81)	175	830	µs
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period	—	—
t_{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t_{CD2CU} + (600 × CLKUSR period)	—	—

Related Information

PS Configuration Timing
Provides the PS configuration timing waveform.

(78) This value is applicable if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.

(79) This value is applicable if you do not delay configuration by externally holding the nSTATUS low.

(80) If nSTATUS is monitored, follow the t_{ST2CK} specification. If nSTATUS is not monitored, follow the t_{CF2CK} specification.

(81) The minimum and maximum numbers apply only if you choose the internal oscillator as the clock source for initializing the device.

Minimum Configuration Time Estimation

Table 55. Minimum Configuration Time Estimation for Intel Cyclone 10 GX Devices

The estimated values are based on the uncompressed configuration bit stream sizes in the Configuration Bit Stream Sizes for Intel Cyclone 10 GX Devices table.

Variant	Product Line	Active Serial (84)			Fast Passive Parallel (85)		
		Width	DCLK (MHz)	Minimum Configuration Time (ms)	Width	DCLK (MHz)	Minimum Configuration Time (ms)
Intel Cyclone 10 GX	GX 085	4	100	204.81	32	100	25.60
	GX 105	4	100	204.81	32	100	25.60
	GX 150	4	100	204.81	32	100	25.60
	GX 220	4	100	204.81	32	100	25.60

Related Information

- Configuration Files on page 52
- DCLK Frequency Specification in the AS Configuration Scheme on page 50
  Provides the DCLK frequency using internal oscillator.

(84) The minimum configuration time is calculated based on DCLK frequency of 100 MHz. Only external CLKUSR may guarantee the frequency accuracy of 100 MHz. If you use internal oscillator of 100 MHz, you may not get the actual frequency of 100 MHz. For the DCLK frequency using internal oscillator, refer to the DCLK Frequency Specification in the AS Configuration Scheme table.

(85) Maximum FPGA FPP bandwidth may exceed bandwidth available from some external storage or control logic.

Date	Version	Changes
November 2017	2017.11.10	• Changed the full symbol names for V_{CCR_GXB} and V_{CCT_GXB}, and changed the description for V_{CCH_GXB} in the *Transceiver Power Supply Operating Conditions for Intel Cyclone 10 GX Devices* table. • Removed note from the *Transceiver Power Supply Operating Conditions* section. • Added a footnote in the *Reference Clock Specifications* table. • Removed the "Programmable AC Gain at High Gain mode and Data Rate ≤ 12.5 Gbps" parameter from the *Receiver Specifications* table. • Changed the channel span descriptions for the x1 and x6 clock networks in the *Transceiver Clock Network Maximum Data Rate Specifications* table. • Changed the description of the VOD ratio in the *Typical Transmitter V_{OD} Settings* table. • Changed the specifications for CDR PPM deviation limit in the *Receiver Specifications* table. • Updated the description for V_{CCT_GXB}, V_{CCR_GXB}, and V_{CCH_GXB}. • Added note to V_I in the *Recommended Operating Conditions for Intel Cyclone 10 GX Devices* table. • Updated notes to RSDS and Mini-LVDS in the *Differential I/O Standards Specifications for Intel Cyclone 10 GX Devices* table. • Updated f_{VCO} specifications in the *Fractional PLL Specifications for Intel Cyclone 10 GX Devices* table. • Updated temperature range from "–40 to 125°C" to "–40 to 100°C" in the *Internal Temperature Sensing Diode Specifications for Intel Cyclone 10 GX Devices* table. • Updated the description for the *Memory Output Clock Jitter Specifications for Intel Cyclone 10 GX Devices* table. • Updated the following IP cores name: — Remote Update Intel FPGA — PHYLite for Parallel Interfaces Intel Cyclone 10 FPGA • Removed automotive-grade information. • Removed Preliminary tags.
May 2017	2017.05.08	Initial release.