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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	12V1
Core Size	16-Bit
Speed	25MHz
Connectivity	CANbus, IrDA, LINbus, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	54
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3.13V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s9s12g128f0clh

Table 1-12. 32-Pin LQFP Pinout for S12GN48

	Function <----lowest-----PRIORITY-----highest---->					Power Supply	Internal Pull Resistor	
Package Pin	Pin	2nd Func.	3rd Func.	4th Func	5th Func		CTRL	Reset State
5	VSS	—	—	—	—	—	—	—
6	PE1[1]	XTAL	—	—	—	—	PUCR/PDPEE	Down
7	TEST	—	—	—	—	N.A.	$\overline{\text{RESET}}$ pin	Down
8	BKGD	MODC	—	—	—	V_{DDX}	PUCR/BKPUE	Up
9	PP0	KWP0	ETRIG0	API_EXTCLK	PWM0	V_{DDX}	PERP/PPSP	Disabled
10	PP1	KWP1	ETRIG1	ECLKX2	PWM1	V_{DDX}	PERP/PPSP	Disabled
11	PP2	KWP2	ETRIG2	PWM2	—	V_{DDX}	PERP/PPSP	Disabled
12	PP3	KWP3	ETRIG3	PWM3	—	V_{DDX}	PERP/PPSP	Disabled
13	PT3	IOC3	—	—	—	V_{DDX}	PERT/PPST	Disabled
14	PT2	IOC2	—	—	—	V_{DDX}	PERT/PPST	Disabled
15	PT1	IOC1	$\overline{\text{IRQ}}$	—	—	V_{DDX}	PERT/PPST	Disabled
16	PT0	IOC0	$\overline{\text{XIRQ}}$	—	—	V_{DDX}	PERT/PPST	Disabled
17	PAD0	KWAD0	AN0	—	—	V_{DDA}	PER1AD/PPS1AD	Disabled
18	PAD1	KWAD1	AN1	—	—	V_{DDA}	PER1AD/PPS1AD	Disabled
19	PAD2	KWAD2	AN2	—	—	V_{DDA}	PER1AD/PPS1AD	Disabled
20	PAD3	KWAD3	AN3	—	—	V_{DDA}	PER1AD/PPS1AD	Disabled
21	PAD4	KWAD4	AN4	—	—	V_{DDA}	PER1AD/PPS1AD	Disabled
22	PAD5	KWAD5	AN5	ACMPO	—	V_{DDA}	PER1AD/PPS1AD	Disabled
23	PAD6	KWAD6	AN6	ACMPP	—	V_{DDA}	PER1AD/PPS1AD	Disabled
24	PAD7	KWAD7	AN7	ACMPM	—	V_{DDA}	PER1AD/PPS1AD	Disabled
25	PS0	RXD0	—	—	—	V_{DDX}	PERS/PPSS	Up
26	PS1	TXD0	—	—	—	V_{DDX}	PERS/PPSS	Up
27	PS4	PWM4	MISO0	—	—	V_{DDX}	PERS/PPSS	Up
28	PS5	IOC4	MOSI0	—	—	V_{DDX}	PERS/PPSS	Up
29	PS6	IOC5	SCK0	—	—	V_{DDX}	PERS/PPSS	Up
30	PS7	API_EXTCLK	ECLK	PWM5	$\overline{\text{SS0}}$	V_{DDX}	PERS/PPSS	Up
31	PM0	RXD1	—	—	—	V_{DDX}	PERM/PPSM	Disabled
32	PM1	TXD1	—	—	—	V_{DDX}	PERM/PPSM	Disabled

1.8.9.2 Pinout 64-Pin LQFP

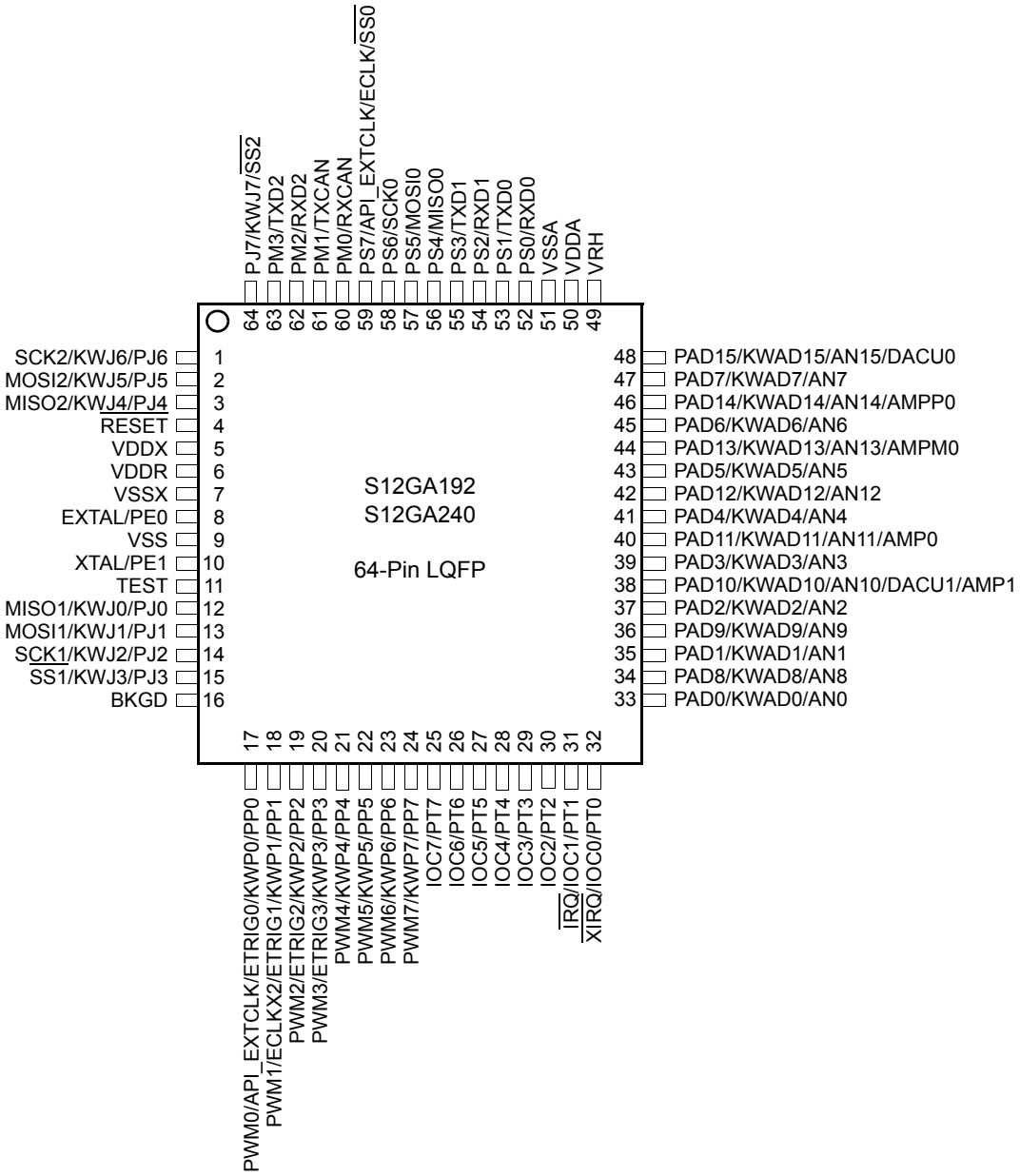

Figure 1-25. 64-Pin LQFP Pinout for S12GA192 and S12GA240

1.12.3 Effects of Reset

When a reset occurs, MCU registers and control bits are initialized. Refer to the respective block sections for register reset states.

On each reset, the Flash module executes a reset sequence to load Flash configuration registers.

1.12.3.1 Flash Configuration Reset Sequence Phase

On each reset, the Flash module holds CPU activity while loading Flash module registers from the Flash memory. If double faults are detected in the reset phase, Flash module protection and security may be active on leaving reset. This is explained in more detail in the Flash module Section 29.1, “Introduction”.

1.12.3.2 Reset While Flash Command Active

If a reset occurs while any Flash command is in progress, that command will be immediately aborted. The state of the word being programmed or the sector/block being erased is not guaranteed.

1.12.3.3 I/O Pins

Refer to the PIM section for reset configurations of all peripheral module ports.

1.12.3.4 RAM

The RAM arrays are not initialized out of reset.

1.13 COP Configuration

The COP time-out rate bits CR[2:0] and the WCOP bit in the CPMUCOP register at address 0x003C are loaded from the Flash register FOPT. See Table 1-36 and Table 1-37 for coding. The FOPT register is loaded from the Flash configuration field byte at global address 0x3_FF0E during the reset sequence.

Table 1-36. Initial COP Rate Configuration

NV[2:0] in FOPT Register	CR[2:0] in CPMUCOP Register
000	111
001	110
010	101
011	100
100	011
101	010
110	001
111	000

Table 2-14. Port P Pins PP7-0 (continued)

PP3-PP2	• Except 20 TSSOP: The PWM channels 3 and 2 signal are mapped to these pins when used with the PWM function. The enabled PWM channel forces the I/O state to be an output. • Except 20 TSSOP: The ADC ETRIG 3 and 2 signal are mapped to these pins when used with the ADC function. The enabled external trigger function has no effect on the I/O state. Refer to Section 2.6.4, “ADC External Triggers ETRIG3-0”. • Except 20 TSSOP: Pin interrupts can be generated if enabled in input or output mode. • Signal priority: Except 20 TSSOP: PWM > GPO
PP1	• Except 20 TSSOP: The PWM channel 1 signal is mapped to this pin when used with the PWM function. The enabled PWM channel forces the I/O state to be an output. • Except 100 LQFP and 20 TSSOP: The ECLKX2 signal is mapped to this pin when used with the external clock function. The enabled ECLKX2 forces the I/O state to an output. • Except 20 TSSOP: The ADC ETRIG1 signal is mapped to this pin when used with the ADC function. The enabled external trigger function has no effect on the I/O state. Refer to Section 2.6.4, “ADC External Triggers ETRIG3-0”. • Except 20 TSSOP: Pin interrupts can be generated if enabled in input or output mode. • Signal priority: Except 100 LQFP and 20 TSSOP: PWM1 > ECLKX2 > GPO 100 LQFP: PWM1 > GPO
PP0	• Except 20 TSSOP: The PWM channel 0 signal is mapped to this pin when used with the PWM function. The enabled PWM channel forces the I/O state to be an output. • Except 100 LQFP and 20 TSSOP: The API_EXTCLK signal is mapped to this pin when used with the external clock function. If the Autonomous Periodic Interrupt clock is enabled and routed here the I/O state is forced to output. • Except 20 TSSOP: The ADC ETRIG0 signal is mapped to this pin when used with the ADC function. The enabled external trigger function has no effect on the I/O state. Refer to Section 2.6.4, “ADC External Triggers ETRIG3-0”. • Except 20 TSSOP: Pin interrupts can be generated if enabled in input or output mode. • Signal priority: Except 100 LQFP and 20 TSSOP: PWM0 > API_EXTCLK > GPO 100 LQFP: PWM0 > GPO

2.4.3.1 Port A Data Register (PORTA)

Address 0x0000 (G1) Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
W								
Reset	0	0	0	0	0	0	0	0

Address 0x0000 (G2, G3) Access: User read only

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

Figure 2-2. Port A Data Register (PORTA)

[1] Read: Anytime. The data source is depending on the data direction value.
Write: Anytime

Table 2-22. PORTA Register Field Descriptions

Field	Description
7-0 PA	**Port A general-purpose input/output data**—Data Register The associated pin can be used as general-purpose I/O. In general-purpose output mode the port data register bit value is driven to the pin. If the associated data direction bit is set to 1, a read returns the value of the port data register bit, otherwise the buffered pin input state is read.

2.4.3.2 Port B Data Register (PORTB)

Address 0x0001 (G1) Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
W								
Reset	0	0	0	0	0	0	0	0

Address 0x0001 (G2, G3) Access: User read only

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

Figure 2-3. Port B Data Register (PORTB)

Chapter 5
S12G Memory Map Controller (S12GMMCV1)

Table 5-1. Revision History Table

Rev. No. (Item No.)	Date (Submitted By)	Sections Affected	Substantial Change(s)
01.02	20-May 2010		Updates for S12VR48 and S12VR64

5.1 Introduction

The S12GMMC module controls the access to all internal memories and peripherals for the CPU12 and S12SBDM module. It regulates access priorities and determines the address mapping of the on-chip resources. Figure 5-1 shows a block diagram of the S12GMMC module.

5.1.1 Glossary

Table 5-2. Glossary Of Terms

Term	Definition
Local Addresses	Address within the CPU12's Local Address Map (Figure 5-11)
Global Address	Address within the Global Address Map (Figure 5-11)
Aligned Bus Access	Bus access to an even address.
Misaligned Bus Access	Bus access to an odd address.
NS	Normal Single-Chip Mode
SS	Special Single-Chip Mode
Unimplemented Address Ranges	Address ranges which are not mapped to any on-chip resource.
NVM	Non-volatile Memory; Flash or EEPROM
IFR	NVM Information Row. Refer to FTMRG Block Guide

5.1.2 Overview

The S12GMMC connects the CPU12's and the S12SBDM's bus interfaces to the MCU's on-chip resources (memories and peripherals). It arbitrates the bus accesses and determines all of the MCU's memory maps. Furthermore, the S12GMMC is responsible for constraining memory accesses on secured devices and for selecting the MCU's functional mode.

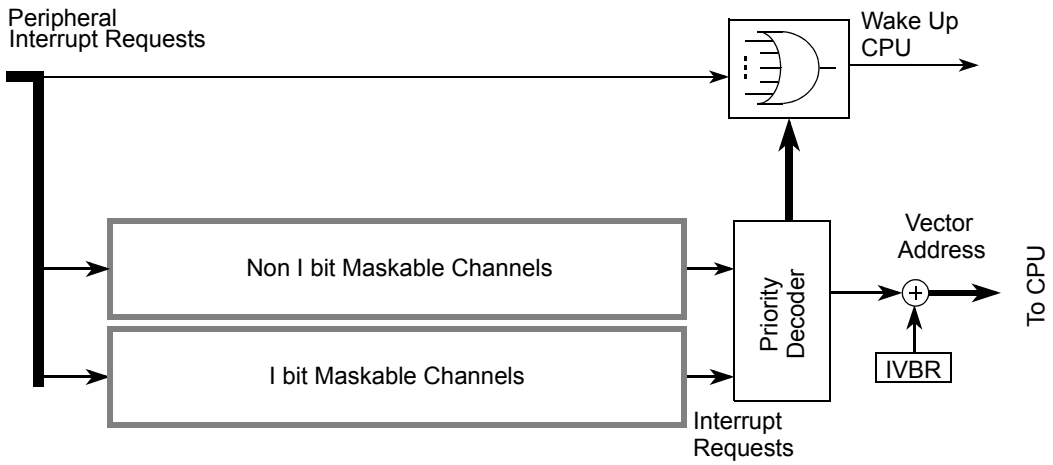

Figure 6-1. INT Block Diagram

6.2 External Signal Description

The INT module has no external signals.

6.3 Memory Map and Register Definition

This section provides a detailed description of all registers accessible in the INT module.

6.3.1 Register Descriptions

This section describes in address order all the INT registers and their individual bits.

6.3.1.1 Interrupt Vector Base Register (IVBR)

Address: 0x0120

	7	6	5	4	3	2	1	0
R W	IVB_ADDR[7:0]							
Reset	1	1	1	1	1	1	1	1

Figure 6-2. Interrupt Vector Base Register (IVBR)

Read: Anytime

Write: Anytime

— The Bus Clock is based on the Oscillator Clock (OSCCLK).
— The PLLCLK is always on to qualify the external oscillator clock. Therefore it is necessary to make sure a valid PLL configuration is used for the selected oscillator frequency.
— This mode can be entered from default mode PEI by performing the following steps:
  – Make sure the PLL configuration is valid for the selected oscillator frequency.
  – Enable the external oscillator (OSCE bit)
  – Wait for oscillator to start up (UPOSC=1)
  – Select the Oscillator Clock (OSCCLK) as Bus Clock (PLLSEL=0).
— The PLLCLK is on and used to qualify the external oscillator clock.

10.1.2.2 Wait Mode

For S12CPMU Wait Mode is the same as Run Mode.

10.1.2.3 Stop Mode

This mode is entered by executing the CPU STOP instruction.

The voltage regulator is in Reduced Power Mode (RPM).

The API is available.

The Phase Locked Loop (PLL) is off.

The Internal Reference Clock (IRC1M) is off.

Core Clock, Bus Clock and BDM Clock are stopped.

Depending on the setting of the PSTP and the OSCE bit, Stop Mode can be differentiated between Full Stop Mode (PSTP = 0 or OSCE=0) and Pseudo Stop Mode (PSTP = 1 and OSCE=1). In addition, the behavior of the COP in each mode will change based on the clocking method selected by COPOSCSEL[1:0].

- **Full Stop Mode (PSTP = 0 or OSCE=0)**
  External oscillator (XOSCLCP) is disabled.
  — If COPOSCSEL1=0:
    The COP and RTI counters halt during Full Stop Mode.
    After wake-up from Full Stop Mode the Core Clock and Bus Clock are running on PLLCLK (PLLSEL=1). COP and RTI are running on IRCCLK (COPOSCSEL0=0, RTIOSCSEL=0).
  — If COPOSCSEL1=1:
    During Full Stop Mode the COP is running on ACLK (trimmable internal RC-Oscillator clock) and the RTI counter halts.
    After wake-up from Full Stop Mode the Core Clock and Bus Clock are running on PLLCLK (PLLSEL=1). The COP runs on ACLK and RTI is running on IRCCLK (COPOSCSEL0=0, RTIOSCSEL=0).

13.1 Introduction

The ADC10B12C is a 12-channel, 10-bit, multiplexed input successive approximation analog-to-digital converter. Refer to device electrical specifications for ATD accuracy.

13.1.1 Features

- 8-, 10-bit resolution.
- Automatic return to low power after conversion sequence
- Automatic compare with interrupt for higher than or less/equal than programmable value
- Programmable sample time.
- Left/right justified result data.
- External trigger control.
- Sequence complete interrupt.
- Analog input multiplexer for 8 analog input channels.
- Special conversions for VRH, VRL, (VRL+VRH)/2.
- 1-to-12 conversion sequence lengths.
- Continuous conversion mode.
- Multiple channel scans.
- Configurable external trigger functionality on any AD channel or any of four additional trigger inputs. The four additional trigger inputs can be chip external or internal. Refer to device specification for availability and connectivity.
- Configurable location for channel wrap around (when converting multiple channels in a sequence).

13.3.2.12.2 Right Justified Result Data (DJM=1)

Module Base +
0x0010 = ATDDR0, 0x0012 = ATDDR1, 0x0014 = ATDDR2, 0x0016 = ATDDR3
0x0018 = ATDDR4, 0x001A = ATDDR5, 0x001C = ATDDR6, 0x001E = ATDDR7
0x0020 = ATDDR8, 0x0022 = ATDDR9, 0x0024 = ATDDR10, 0x0026 = ATDDR11

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0	0	0	0	Result-Bit[11:0]											
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 13-15. Right justified ATD conversion result register (ATDDR*n*)

Table 13-22 shows how depending on the A/D resolution the conversion result is transferred to the ATD result registers for right justified data. Compare is always done using all 12 bits of both the conversion result and the compare value in ATDDRn.

Table 13-22. Conversion result mapping to ATDDRn

A/D resolution	DJM	conversion result mapping to ATDDR*n*
8-bit data	1	Result-Bit[11:8]=0000, Result-Bit[7:0] = conversion result
10-bit data	1	Result-Bit[11:10]=00, Result-Bit[9:0] = conversion result

Chapter 14
Analog-to-Digital Converter (ADC12B12CV2)

Revision History

Version Number	Revision Date	Effective Date	Author	Description of Changes
V02.00	13 May 2009	13 May 2009		Initial version copied from V01.06, changed unused Bits in ATDDIEN to read logic 1
V02.01	30.Nov 2009	30.Nov 2009		Updated Table 14-15 Analog Input Channel Select Coding - description of internal channels. Updated register ATDDR (left/right justified result) description in section 14.3.2.12.1/14-502 and 14.3.2.12.2/14-503 and added table Table 14-21 to improve feature description.
V02.02	09 Feb 2010	09 Feb 2010		Fixed typo in Table 14-9- conversion result for 3mV and 10bit resolution
V02.03	26 Feb 2010	26 Feb 2010		Corrected Table 14-15 Analog Input Channel Select Coding - description of internal channels.
V02.04	14 Apr 2010	14 Apr 2010		Corrected typos to be in-line with SoC level pin naming conventions for VDDA, VSSA, VRL and VRH.
V02.05	25 Aug 2010	25 Aug 2010		Removed feature of conversion during STOP and general wording clean up done in Section 14.4, “Functional Description
V02.06	09 Sep 2010	09 Sep 2010		Update of internal only information.
V02.07	11 Feb 2011	11 Feb 2011		Connectivity Information regarding internal channel_6 added to Table 14-15.
V02.08	29 Mar 2011	29 Mar 2011		Fixed typo in bit description field Table 14-14 for bits CD, CC, CB, CA. Last sentence contained a wrong highest channel number (it is not AN7 to AN0 instead it is AN11 to AN0).
V02.09	22. Jun 2012	22. Jun 2012		Update of register write access information in section 14.3.2.9/14-500.
V02.10	29 Jun 2012	29. Jun 2012		Removed IP name in block diagram Figure 14-1
V02.11	02 Oct 2012	02 Oct 2012		Added user information to avoid maybe false external trigger events when enabling the external trigger mode (Section 14.4.2.1, “External Trigger Input).

Table 16-11. ATD Behavior in Freeze Mode (Breakpoint)

FRZ1	FRZ0	Behavior in Freeze Mode
0	0	Continue conversion
0	1	Reserved
1	0	Finish current conversion, then freeze
1	1	Freeze Immediately

16.3.2.5 ATD Control Register 4 (ATDCTL4)

Writes to this register will abort current conversion sequence.

Module Base + 0x0004

Figure 16-7. ATD Control Register 4 (ATDCTL4)

Read: Anytime

Write: Anytime

Table 16-12. ATDCTL4 Field Descriptions

Field	Description
7–5 SMP[2:0]	**Sample Time Select** — These three bits select the length of the sample time in units of ATD conversion clock cycles. Note that the ATD conversion clock period is itself a function of the prescaler value (bits PRS4-0). Table 16-13 lists the available sample time lengths.
4–0 PRS[4:0]	**ATD Clock Prescaler** — These 5 bits are the binary prescaler value PRS. The ATD conversion clock frequency is calculated as follows: $f_{ATDCLK} = \frac{f_{BUS}}{2 \times (PRS + 1)}$ Refer to Device Specification for allowed frequency range of f_{ATDCLK}.

Table 16-13. Sample Time Select

SMP2	SMP1	SMP0	Sample Time in Number of ATD Clock Cycles
0	0	0	4
0	0	1	6
0	1	0	8
0	1	1	10
1	0	0	12
1	0	1	16
1	1	0	20

[3] SPIDRH can be written repeatedly without any effect on SPTEF. SPTEF Flag is cleared only by writing to SPIDRL after reading SPISR with SPTEF == 1.

21.3.2.5 SPI Data Register (SPIDR = SPIDRH:SPIDRL)

Module Base +0x0004

	7	6	5	4	3	2	1	0
R	R15	R14	R13	R12	R11	R10	R9	R8
W	T15	T14	T13	T12	T11	T10	T9	T8
Reset	0	0	0	0	0	0	0	0

Figure 21-7. SPI Data Register High (SPIDRH)

Module Base +0x0005

	7	6	5	4	3	2	1	0
R	R7	R6	R5	R4	R3	R2	R1	R0
W	T7	T6	T5	T4	T3	T2	T1	T0
Reset	0	0	0	0	0	0	0	0

Figure 21-8. SPI Data Register Low (SPIDRL)

Read: Anytime; read data only valid when SPIF is set

Write: Anytime

The SPI data register is both the input and output register for SPI data. A write to this register allows data to be queued and transmitted. For an SPI configured as a master, queued data is transmitted immediately after the previous transmission has completed. The SPI transmitter empty flag SPTEF in the SPISR register indicates when the SPI data register is ready to accept new data.

Received data in the SPIDR is valid when SPIF is set.

If SPIF is cleared and data has been received, the received data is transferred from the receive shift register to the SPIDR and SPIF is set.

If SPIF is set and not serviced, and a second data value has been received, the second received data is kept as valid data in the receive shift register until the start of another transmission. The data in the SPIDR does not change.

If SPIF is set and valid data is in the receive shift register, and SPIF is serviced before the start of a third transmission, the data in the receive shift register is transferred into the SPIDR and SPIF remains set (see Figure 21-9).

If SPIF is set and valid data is in the receive shift register, and SPIF is serviced after the start of a third transmission, the data in the receive shift register has become invalid and is not transferred into the SPIDR (see Figure 21-10).

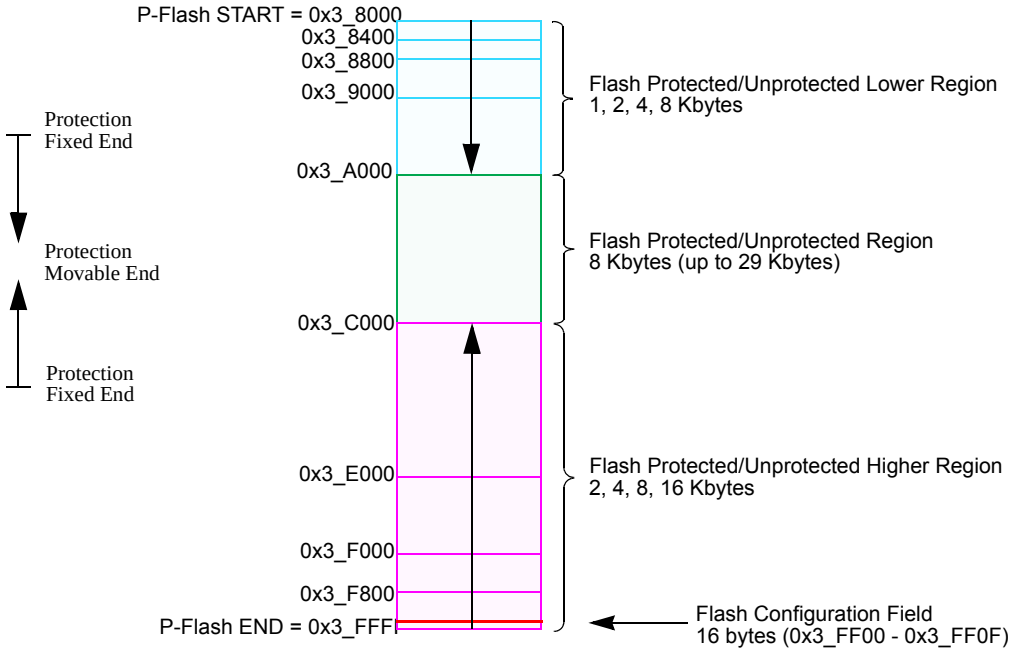

Figure 25-2. P-Flash Memory Map

Table 25-5. Program IFR Fields

Global Address	Size (Bytes)	Field Description
0x0_4000 – 0x0_4007	8	Reserved
0x0_4008 – 0x0_40B5	174	Reserved
0x0_40B6 – 0x0_40B7	2	Version ID[1]
0x0_40B8 – 0x0_40BF	8	Reserved
0x0_40C0 – 0x0_40FF	64	Program Once Field Refer to Section 25.4.6.6, “Program Once Command”

[1] Used to track firmware patch versions, see Section 25.4.2

Table 26-6. Memory Controller Resource Fields (NVMRES[1]=1)

Global Address	Size (Bytes)	Description
0x0_4000 – 0x040FF	256	P-Flash IFR (see Table 26-5)
0x0_4100 – 0x0_41FF	256	Reserved.
0x0_4200 – 0x0_57FF		Reserved
0x0_5800 – 0x0_59FF	512	Reserved
0x0_5A00 – 0x0_5FFF	1,536	Reserved
0x0_6000 – 0x0_6BFF	3,072	Reserved
0x0_6C00 – 0x0_7FFF	5,120	Reserved

1 NVMRES - See Section 26.4.3 for NVMRES (NVM Resource) detail.

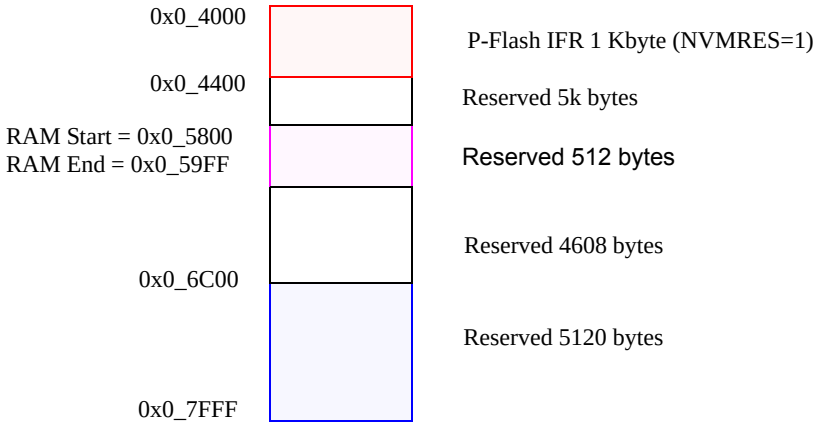

Figure 26-3. Memory Controller Resource Memory Map (NVMRES=1)

26.3.2 Register Descriptions

The Flash module contains a set of 20 control and status registers located between Flash module base + 0x0000 and 0x0013.

In the case of the writable registers, the write accesses are forbidden during Fash command execution (for more detail, see Caution note in Section 26.3).

26.4.7 Interrupts

The Flash module can generate an interrupt when a Flash command operation has completed or when a Flash command operation has detected an ECC fault.

Table 26-66. Flash Interrupt Sources

Interrupt Source	Interrupt Flag	Local Enable	Global (CCR) Mask
Flash Command Complete	CCIF (FSTAT register)	CCIE (FCNFG register)	I Bit
ECC Double Bit Fault on Flash Read	DFDIF (FERSTAT register)	DFDIE (FERCNFG register)	I Bit
ECC Single Bit Fault on Flash Read	SFDIF (FERSTAT register)	SFDIE (FERCNFG register)	I Bit

NOTE

Vector addresses and their relative interrupt priority are determined at the MCU level.

26.4.7.1 Description of Flash Interrupt Operation

The Flash module uses the CCIF flag in combination with the CCIE interrupt enable bit to generate the Flash command interrupt request. The Flash module uses the DFDIF and SFDIF flags in combination with the DFDIE and SFDIE interrupt enable bits to generate the Flash error interrupt request. For a detailed description of the register bits involved, refer to Section 26.3.2.5, “Flash Configuration Register (FCNFG)”, Section 26.3.2.6, “Flash Error Configuration Register (FERCNFG)”, Section 26.3.2.7, “Flash Status Register (FSTAT)”, and Section 26.3.2.8, “Flash Error Status Register (FERSTAT)”.

The logic used for generating the Flash module interrupts is shown in Figure 26-27.

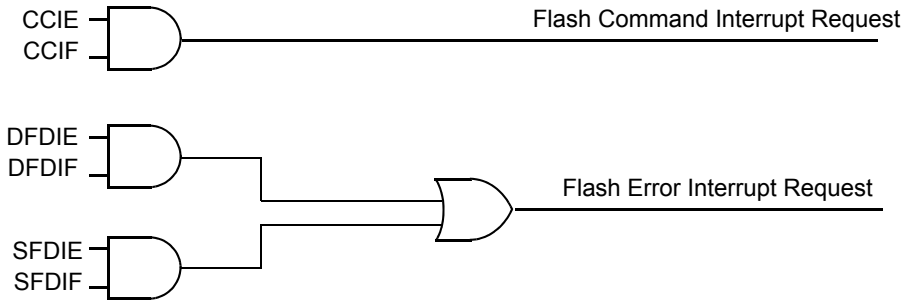

Figure 26-27. Flash Module Interrupts Implementation

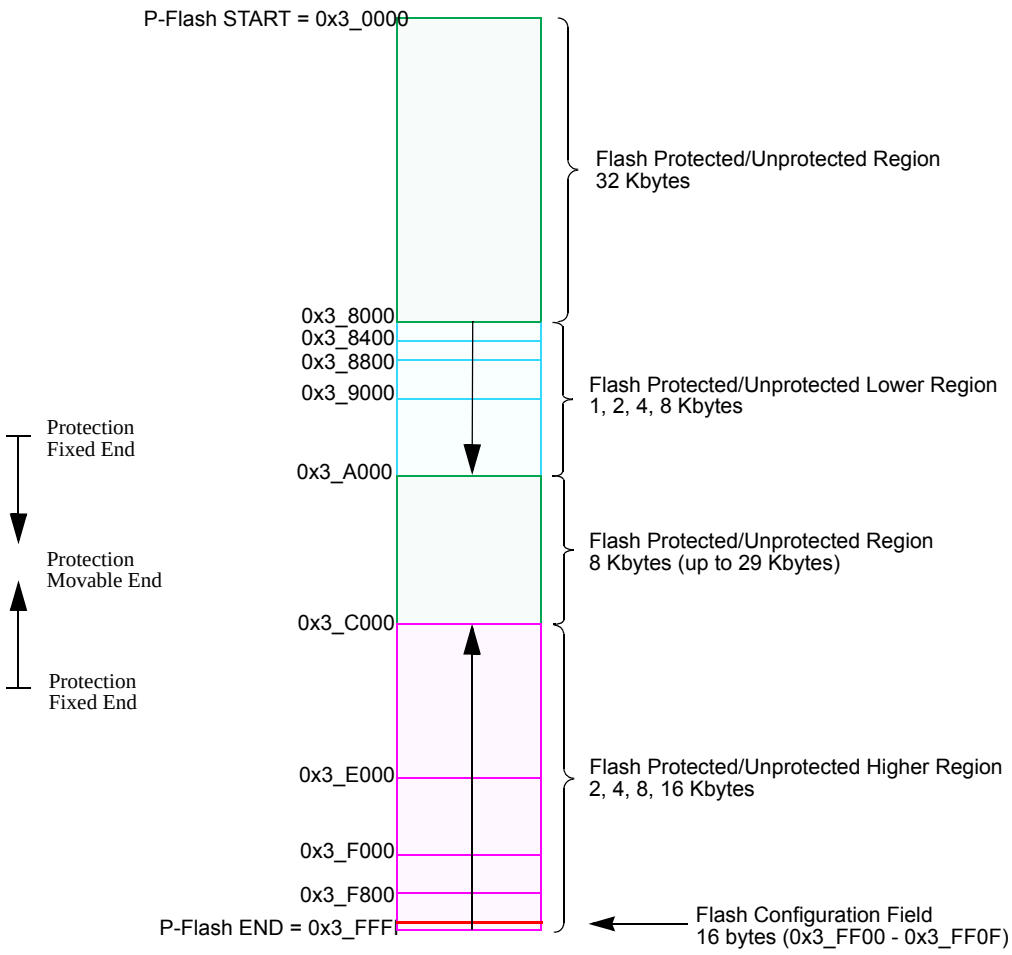

Figure 27-2. P-Flash Memory Map

Table 27-5. Program IFR Fields

Global Address	Size (Bytes)	Field Description
0x0_4000 – 0x0_4007	8	Reserved
0x0_4008 – 0x0_40B5	174	Reserved
0x0_40B6 – 0x0_40B7	2	Version ID[1]
0x0_40B8 – 0x0_40BF	8	Reserved
0x0_40C0 – 0x0_40FF	64	Program Once Field Refer to Section 27.4.6.6, “Program Once Command”

[1] Used to track firmware patch versions, see Section 27.4.2

The Flash memory may be read as bytes and aligned words. Read access time is one bus cycle for bytes and aligned words. For misaligned words access, the CPU has to perform twice the byte read access command. For Flash memory, an erased bit reads 1 and a programmed bit reads 0.

It is possible to read from P-Flash memory while some commands are executing on EEPROM memory. It is not possible to read from EEPROM memory while a command is executing on P-Flash memory. Simultaneous P-Flash and EEPROM operations are discussed in Section 28.4.5.

Both P-Flash and EEPROM memories are implemented with Error Correction Codes (ECC) that can resolve single bit faults and detect double bit faults. For P-Flash memory, the ECC implementation requires that programming be done on an aligned 8 byte basis (a Flash phrase). Since P-Flash memory is always read by half-phrase, only one single bit fault in an aligned 4 byte half-phrase containing the byte or word accessed will be corrected.

28.1.1 Glossary

Command Write Sequence — An MCU instruction sequence to execute built-in algorithms (including program and erase) on the Flash memory.

EEPROM Memory — The EEPROM memory constitutes the nonvolatile memory store for data.

EEPROM Sector — The EEPROM sector is the smallest portion of the EEPROM memory that can be erased. The EEPROM sector consists of 4 bytes.

NVM Command Mode — An NVM mode using the CPU to setup the FCCOB register to pass parameters required for Flash command execution.

Phrase — An aligned group of four 16-bit words within the P-Flash memory. Each phrase includes two sets of aligned double words with each set including 7 ECC bits for single bit fault correction and double bit fault detection within each double word.

P-Flash Memory — The P-Flash memory constitutes the main nonvolatile memory store for applications.

P-Flash Sector — The P-Flash sector is the smallest portion of the P-Flash memory that can be erased. Each P-Flash sector contains 512 bytes.

Program IFR — Nonvolatile information register located in the P-Flash block that contains the Version ID, and the Program Once field.

28.1.2 Features

28.1.2.1 P-Flash Features

- 96 Kbytes of P-Flash memory composed of one 96 Kbyte Flash block divided into 192 sectors of 512 bytes

Table 31-13. FCNFG Field Descriptions

Field	Description
7 CCIE	**Command Complete Interrupt Enable** — The CCIE bit controls interrupt generation when a Flash command has completed. 0 Command complete interrupt disabled 1 An interrupt will be requested whenever the CCIF flag in the FSTAT register is set (see Section 31.3.2.7)
4 IGNSF	**Ignore Single Bit Fault** — The IGNSF controls single bit fault reporting in the FERSTAT register (see Section 31.3.2.8). 0 All single bit faults detected during array reads are reported 1 Single bit faults detected during array reads are not reported and the single bit fault interrupt will not be generated
1 FDFD	**Force Double Bit Fault Detect** — The FDFD bit allows the user to simulate a double bit fault during Flash array read operations and check the associated interrupt routine. The FDFD bit is cleared by writing a 0 to FDFD. 0 Flash array read operations will set the DFDIF flag in the FERSTAT register only if a double bit fault is detected 1 Any Flash array read operation will force the DFDIF flag in the FERSTAT register to be set (see Section 31.3.2.7) and an interrupt will be generated as long as the DFDIE interrupt enable in the FERCNFG register is set (see Section 31.3.2.6)
0 FSFD	**Force Single Bit Fault Detect** — The FSFD bit allows the user to simulate a single bit fault during Flash array read operations and check the associated interrupt routine. The FSFD bit is cleared by writing a 0 to FSFD. 0 Flash array read operations will set the SFDIF flag in the FERSTAT register only if a single bit fault is detected 1 Flash array read operation will force the SFDIF flag in the FERSTAT register to be set (see Section 31.3.2.7) and an interrupt will be generated as long as the SFDIE interrupt enable in the FERCNFG register is set (see Section 31.3.2.6)

31.3.2.6 Flash Error Configuration Register (FERCNFG)

The FERCNFG register enables the Flash error interrupts for the FERSTAT flags.

Offset Module Base + 0x0005

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	DFDIE	SFDIE
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 31-10. Flash Error Configuration Register (FERCNFG)

All assigned bits in the FERCNFG register are readable and writable.

0x00A0–0x0C7 Pulse-Width-Modulator (PWM)

0x00B7	PWMPER3	R W	Bit 7	6	5	4	3	2	1	Bit 0
0x00B8	PWMPER4	R W	Bit 7	6	5	4	3	2	1	Bit 0
0x00B9	PWMPER5	R W	Bit 7	6	5	4	3	2	1	Bit 0
0x00BA	PWMPER6	R W	Bit 7	6	5	4	3	2	1	Bit 0
0x00BB	PWMPER7	R W	Bit 7	6	5	4	3	2	1	Bit 0
0x00BC	PWMDTY0	R W	Bit 7	6	5	4	3	2	1	Bit 0
0x00BD	PWMDTY1	R W	Bit 7	6	5	4	3	2	1	Bit 0
0x00BE	PWMDTY2	R W	Bit 7	6	5	4	3	2	1	Bit 0
0x00BF	PWMDTY3	R W	Bit 7	6	5	4	3	2	1	Bit 0
0x00C0	PWMDTY4	R W	Bit 7	6	5	4	3	2	1	Bit 0
0x00C1	PWMDTY5	R W	Bit 7	6	5	4	3	2	1	Bit 0
0x00C2	PWMDTY6	R W	Bit 7	6	5	4	3	2	1	Bit 0
0x00C3	PWMDTY7	R W	Bit 7	6	5	4	3	2	1	Bit 0
0x00C4- 0x00C7	Reserved	R W	0	0	0	0	0	0	0	0

0x00C8–0x0CF Serial Communication Interface (SCI0)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x00C8	SCI0BDH	R W	IREN	TNP1	TNP0	SBR12	SBR11	SBR10	SBR9	SBR8
0x00C8	SCI0ASR1	R W	RXEDGIF	0	0	0	0	BERRV	BERRIF	BKDIF
0x00C9	SCI0BDL	R W	SBR7	SBR6	SBR5	SBR4	SBR3	SBR2	SBR1	SBR0
0x00C9	SCI0ACR1	R W	RXEDGIE	0	0	0	0	0	BERRIE	BKDIE
0x00CA	SCI0CR1	R W	LOOPS	SCISWAI	RSRC	M	WAKE	ILT	PE	PT
0x00CA	SCI0ACR2	R W	0	0	0	0	0	BERRM1	BERRM0	BKDFE
0x00CB	SCI0CR2	R W	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK