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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | 12V1 |
| Core Size | 16-Bit |
| Speed | 25MHz |
| Connectivity | CANbus, IrDA, LINbus, SCI, SPI |
| Peripherals | LVD, POR, PWM, WDT |
| Number of I/O | 86 |
| Program Memory Size | 128KB (128K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 4K x 8 |
| RAM Size | 8K x 8 |
| Voltage - Supply (Vcc/Vdd) | 3.13V ~ 5.5V |
| Data Converters | A/D 12x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-LQFP |
| Supplier Device Package | 100-LQFP (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/s9s12g128f0cllr |

## Chapter 2
## Port Integration Module (S12GPIMV1)

## Chapter 19
## Pulse-Width Modulator (S12PWM8B8CV2)



## Chapter 20
## Serial Communication Interface (S12SCIV5)

- Four stage state sequencer

## 1.4 Key Performance Parameters

The key performance parameters of S12G devices feature:

- Continuous Operating voltage of 3.15 V to 5.5 V
- Operating temperature ($T_A$) of –40°C to 125°C
- Junction temperature ($T_J$) of up to 150°C
- Bus frequency ($f_{Bus}$) of dc to 25 MHz
- Packaging:
  - 100-pin LQFP, 0.5 mm pitch, 14 mm x 14 mm outline
  - 64-pin LQFP, 0.5 mm pitch, 10 mm x 10 mm outline
  - 48-pin LQFP, 0.5 mm pitch, 7 mm x 7 mm outline
  - 48-pin QFN, 0.5 mm pitch, 7 mm x 7 mm outline
  - 32-pin LQFP, 0.8 mm pitch, 7 mm x 7 mm outline
  - 20 TSSOP, 0.65 mm pitch, 4.4 mm x 6.5 mm outline
  - Known good die (KGD), unpackaged

## 1.5 Block Diagram

Figure 1-1 shows a block diagram of the MC9S12G-Family.

# 1.8 Device Pinouts

## 1.8.1 S12GN16 and S12GN32

### 1.8.1.1 Pinout 20-Pin TSSOP

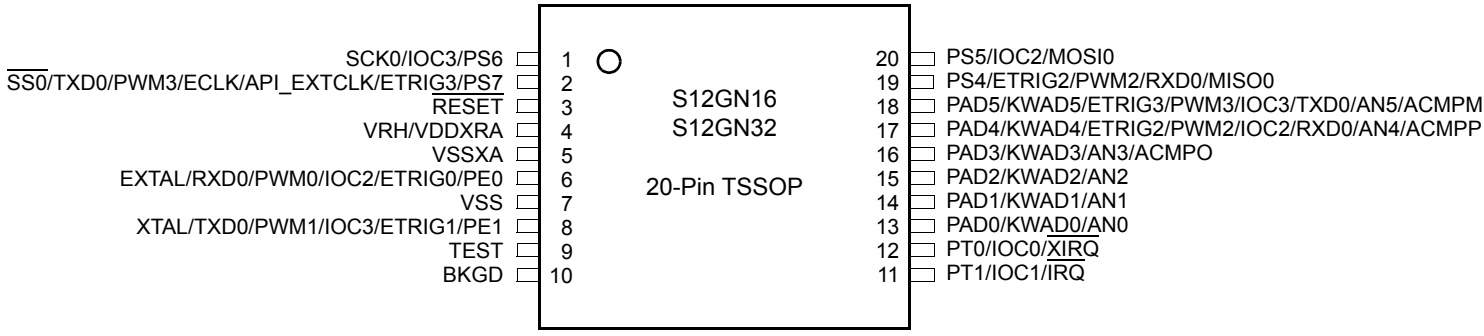


**Figure 1-3. 20-Pin TSSOP Pinout for S12GN16 and S12GN32**

**Table 1-8. 20-Pin TSSOP Pinout for S12GN16 and S12GN32**

| | Function <----lowest-----PRIORITY-----highest----> | | | | | | | | Power Supply | Internal Pull Resistor | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Package Pin | Pin | 2nd Func. | 3rd Func. | 4th Func | 5th Func | 6th Func | 7th Func | 8th Func | | CTRL | Reset State |
| 1 | PS6 | IOC3 | SCK0 | — | — | — | — | — | $V_{DDX}$ | PERS/PPSS | Up |
| 2 | PS7 | ETRIG3 | API_EXTCLK | ECLK | PWM3 | TXD0 | $\overline{SS0}$ | — | $V_{DDX}$ | PERS/PPSS | Up |
| 3 | RESET | — | — | — | — | — | — | — | $V_{DDX}$ | PULLUP | |
| 4 | VDDXRA | VRH | — | — | — | — | — | — | — | — | — |
| 5 | VSSXA | — | — | — | — | — | — | — | — | — | — |
| 6 | PE0[1] | ETRIG0 | PWM0 | IOC2 | RXD0 | EXTAL | — | — | $V_{DDX}$ | PUCR/PDPEE | Down |
| 7 | VSS | — | — | — | — | — | — | — | — | — | — |
| 8 | PE1[1] | ETRIG1 | PWM1 | IOC3 | TXD0 | XTAL | — | — | | PUCR/PDPEE | Down |
| 9 | TEST | — | — | — | — | — | — | — | N.A. | $\overline{RESET}$ pin | Down |
| 10 | BKGD | MODC | — | — | — | — | — | — | $V_{DDX}$ | Always on | Up |
| 11 | PT1 | IOC1 | $\overline{IRQ}$ | — | — | — | — | — | $V_{DDX}$ | PERT/PPST | Disabled |
| 12 | PT0 | IOC0 | $\overline{XIRQ}$ | — | — | — | — | — | $V_{DDX}$ | PERT/PPST | Disabled |
| 13 | PAD0 | KWAD0 | AN0 | — | — | — | — | — | $V_{DDA}$ | PER1AD/PPS1AD | Disabled |
| 14 | PAD1 | KWAD1 | AN1 | — | — | — | — | — | $V_{DDA}$ | PER1AD/PPS1AD | Disabled |
| 15 | PAD2 | KWAD2 | AN2 | — | — | — | — | — | $V_{DDA}$ | PER1AD/PPS1AD | Disabled |

**Table 1-15. 32-Pin LQFP Pinout for S12G48 and S12G64**

| | Function <----lowest-----PRIORITY-----highest----> | | | | | Power Supply | Internal Pull Resistor | |
|---|---|---|---|---|---|---|---|---|
| Package Pin | Pin | 2nd Func. | 3rd Func. | 4th Func | 5th Func | | CTRL | Reset State |
| 2 | VDDXRA | VRH | — | — | — | — | — | — |
| 3 | VSSXA | — | — | — | — | — | — | — |
| 4 | PE0[1] | EXTAL | — | — | — | — | PUCR/PDPEE | Down |
| 5 | VSS | — | — | — | — | — | — | — |
| 6 | PE1[1] | XTAL | — | — | — | — | PUCR/PDPEE | Down |
| 7 | TEST | — | — | — | — | N.A. | $\overline{\text{RESET}}$ pin | Down |
| 8 | BKGD | MODC | — | — | — | $V_{DDX}$ | PUCR/BKPUE | Up |
| 9 | PP0 | KWP0 | ETRIG0 | API_EXTCLK | PWM0 | $V_{DDX}$ | PERP/PPSP | Disabled |
| 10 | PP1 | KWP1 | ETRIG1 | ECLKX2 | PWM1 | $V_{DDX}$ | PERP/PPSP | Disabled |
| 11 | PP2 | KWP2 | ETRIG2 | PWM2 | — | $V_{DDX}$ | PERP/PPSP | Disabled |
| 12 | PP3 | KWP3 | ETRIG3 | PWM3 | — | $V_{DDX}$ | PERP/PPSP | Disabled |
| 13 | PT3 | IOC3 | — | — | — | $V_{DDX}$ | PERT/PPST | Disabled |
| 14 | PT2 | IOC2 | — | — | — | $V_{DDX}$ | PERT/PPST | Disabled |
| 15 | PT1 | IOC1 | $\overline{\text{IRQ}}$ | — | — | $V_{DDX}$ | PERT/PPST | Disabled |
| 16 | PT0 | IOC0 | $\overline{\text{XIRQ}}$ | — | — | $V_{DDX}$ | PERT/PPST | Disabled |
| 17 | PAD0 | KWAD0 | AN0 | — | — | $V_{DDA}$ | PER1AD/PPS1AD | Disabled |
| 18 | PAD1 | KWAD1 | AN1 | — | — | $V_{DDA}$ | PER1AD/PPS1AD | Disabled |
| 19 | PAD2 | KWAD2 | AN2 | — | — | $V_{DDA}$ | PER1AD/PPS1AD | Disabled |
| 20 | PAD3 | KWAD3 | AN3 | — | — | $V_{DDA}$ | PER1AD/PPS1AD | Disabled |
| 21 | PAD4 | KWAD4 | AN4 | — | — | $V_{DDA}$ | PER1AD/PPS1AD | Disabled |
| 22 | PAD5 | KWAD5 | AN5 | ACMPO | — | $V_{DDA}$ | PER1AD/PPS1AD | Disabled |
| 23 | PAD6 | KWAD6 | AN6 | ACMPP | — | $V_{DDA}$ | PER1AD/PPS1AD | Disabled |
| 24 | PAD7 | KWAD7 | AN7 | ACMPM | — | $V_{DDA}$ | PER1AD/PPS1AD | Disabled |
| 25 | PS0 | RXD0 | — | — | — | $V_{DDX}$ | PERS/PPSS | Up |
| 26 | PS1 | TXD0 | — | — | — | $V_{DDX}$ | PERS/PPSS | Up |
| 27 | PS4 | PWM4 | MISO0 | — | — | $V_{DDX}$ | PERS/PPSS | Up |
| 28 | PS5 | IOC4 | MOSI0 | — | — | $V_{DDX}$ | PERS/PPSS | Up |
| 29 | PS6 | IOC5 | SCK0 | — | — | $V_{DDX}$ | PERS/PPSS | Up |

**Table 1-16. 48-Pin LQFP Pinout for S12G48 and S12G64**

| | Function <----lowest-----PRIORITY-----highest----> | | | | | Power Supply | Internal Pull Resistor | |
|---|---|---|---|---|---|---|---|---|
| Package Pin | Pin | 2nd Func. | 3rd Func. | 4th Func | 5th Func | | CTRL | Reset State |
| 3 | VSSX | — | — | — | — | — | — | — |
| 4 | PE0[1] | EXTAL | — | — | — | $V_{DDX}$ | PUCR/PDPEE | Down |
| 5 | VSS | — | — | — | — | — | — | — |
| 6 | PE1[1] | XTAL | — | — | — | $V_{DDX}$ | PUCR/PDPEE | Down |
| 7 | TEST | — | — | — | — | N.A. | $\overline{\text{RESET}}$ pin | Down |
| 8 | PJ0 | KWJ0 | — | MISO1 | — | $V_{DDX}$ | PERJ/PPSJ | Up |
| 9 | PJ1 | KWJ1 | — | MOSI1 | — | $V_{DDX}$ | PERJ/PPSJ | Up |
| 10 | PJ2 | KWJ2 | — | SCK1 | — | $V_{DDX}$ | PERJ/PPSJ | Up |
| 11 | PJ3 | KWJ3 | — | $\overline{\text{SS1}}$ | — | $V_{DDX}$ | PERJ/PPSJ | Up |
| 12 | BKGD | MODC | — | — | — | $V_{DDX}$ | PUCR/BKPUE | Up |
| 13 | PP0 | KWP0 | ETRIG0 | API_EXTCLK | PWM0 | $V_{DDX}$ | PERP/PPSP | Disabled |
| 14 | PP1 | KWP1 | ETRIG1 | ECLKX2 | PWM1 | $V_{DDX}$ | PERP/PPSP | Disabled |
| 15 | PP2 | KWP2 | ETRIG2 | PWM2 | — | $V_{DDX}$ | PERP/PPSP | Disabled |
| 16 | PP3 | KWP3 | ETRIG3 | PWM3 | — | $V_{DDX}$ | PERP/PPSP | Disabled |
| 17 | PP4 | KWP4 | PWM4 | — | — | $V_{DDX}$ | PERP/PPSP | Disabled |
| 18 | PP5 | KWP5 | PWM5 | — | — | $V_{DDX}$ | PERP/PPSP | Disabled |
| 19 | PT5 | IOC5 | — | — | — | $V_{DDX}$ | PERT/PPST | Disabled |
| 20 | PT4 | IOC4 | — | — | — | $V_{DDX}$ | PERT/PPST | Disabled |
| 21 | PT3 | IOC3 | — | — | — | $V_{DDX}$ | PERT/PPST | Disabled |
| 22 | PT2 | IOC2 | — | — | — | $V_{DDX}$ | PERT/PPST | Disabled |
| 23 | PT1 | IOC1 | $\overline{\text{IRQ}}$ | — | — | $V_{DDX}$ | PERT/PPST | Disabled |
| 24 | PT0 | IOC0 | $\overline{\text{XIRQ}}$ | — | — | $V_{DDX}$ | PERT/PPST | Disabled |
| 25 | PAD0 | KWAD0 | AN0 | — | — | $V_{DDA}$ | PER1AD/PPS1AD | Disabled |
| 26 | PAD8 | KWAD8 | AN8 | — | — | $V_{DDA}$ | PER0AD/PPS0AD | Disabled |
| 27 | PAD1 | KWAD1 | AN1 | — | — | $V_{DDA}$ | PER1AD/PPS1AD | Disabled |
| 28 | PAD9 | KWAD9 | AN9 | ACMPO | — | $V_{DDA}$ | PER0AD/PPS0AD | Disabled |
| 29 | PAD2 | KWAD2 | AN2 | — | — | $V_{DDA}$ | PER1AD/PPS1AD | Disabled |
| 30 | PAD10 | KWAD10 | AN10 | ACMPP | | $V_{DDA}$ | PER0AD/PPS0AD | Disabled |

**Table 1-20. 48-Pin LQFP Pinout for S12G96 and S12G128**

| | Function <----lowest-----PRIORITY-----highest----> | | | | | Power Supply | Internal Pull Resistor | |
|---|---|---|---|---|---|---|---|---|
| Package Pin | Pin | 2nd Func. | 3rd Func. | 4th Func | 5th Func | | CTRL | Reset State |
| 30 | PAD10 | KWAD10 | AN10 | | | $V_{DDA}$ | PER0AD/PPS0AD | Disabled |
| 31 | PAD3 | KWAD3 | AN3 | — | — | $V_{DDA}$ | PER1AD/PPS1AD | Disabled |
| 32 | PAD11 | KWAD11 | AN11 | — | — | $V_{DDA}$ | PER0AD/PPS0AD | Disabled |
| 33 | PAD4 | KWAD4 | AN4 | — | — | $V_{DDA}$ | PER1AD/PPS1AD | Disabled |
| 34 | PAD5 | KWAD5 | AN5 | — | — | $V_{DDA}$ | PER1AD/PPS0AD | Disabled |
| 35 | PAD6 | KWAD6 | AN6 | — | — | $V_{DDA}$ | PER1AD/PPS1AD | Disabled |
| 36 | PAD7 | KWAD7 | AN7 | — | — | $V_{DDA}$ | PER1AD/PPS1AD | Disabled |
| 37 | VDDA | VRH | — | — | — | — | — | — |
| 38 | VSSA | — | — | — | — | — | — | — |
| 39 | PS0 | RXD0 | — | — | — | $V_{DDX}$ | PERS/PPSS | Up |
| 40 | PS1 | TXD0 | — | — | — | $V_{DDX}$ | PERS/PPSS | Up |
| 41 | PS2 | RXD1 | — | — | — | $V_{DDX}$ | PERS/PPSS | Up |
| 42 | PS3 | TXD1 | — | — | — | $V_{DDX}$ | PERS/PPSS | Up |
| 43 | PS4 | MISO0 | — | — | — | $V_{DDX}$ | PERS/PPSS | Up |
| 44 | PS5 | MOSI0 | — | — | — | $V_{DDX}$ | PERS/PPSS | Up |
| 45 | PS6 | SCK0 | — | — | — | $V_{DDX}$ | PERS/PPSS | Up |
| 46 | PS7 | API_EXTCLK | ECLK | $\overline{SS0}$ | — | $V_{DDX}$ | PERS/PPSS | Up |
| 47 | PM0 | RXD2 | RXCAN | — | — | $V_{DDX}$ | PERM/PPSM | Disabled |
| 48 | PM1 | TXD2 | TXCAN | — | — | $V_{DDX}$ | PERM/PPSM | Disabled |

[1] The regular I/O characteristics (see Section A.2, “I/O Characteristics”) apply if the EXTAL/XTAL function is disabled

# Chapter 3
# 5V Analog Comparator (ACMPV1)

## Revision History

| Rev. No. (Item No.) | Date (Submitted By) | Sections Affected | Substantial Change(s) |
|---|---|---|---|
| V00.08 | 13 Aug 2010 | | • Added register name to every bitfield reference |
| V00.09 | 10 Sep 2010 | | • Internal updates<br>• |
| V01.00 | 18 Oct 2010 | | • Initial version<br>• |

## 3.1 Introduction

The analog comparator (ACMP) provides a circuit for comparing two analog input voltages. Refer to the device overview section for availability on a specific device.

## 3.2 Features

The ACMP has the following features:

- Low offset, low long-term offset drift
- Selectable interrupt on rising, falling, or rising and falling edges of comparator output
- Option to output comparator signal on an external pin ACMPO
- Option to trigger timer input capture events

## 3.3 Block Diagram

The block diagram of the ACMP is shown below.

## 11.3.2 Register Descriptions

This section describes in address order all the ADC10B8C registers and their individual bits.

### 11.3.2.1 ATD Control Register 0 (ATDCTL0)

Writes to this register will abort current conversion sequence.

Module Base + 0x0000

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R | Reserved | 0 | 0 | 0 | WRAP3 | WRAP2 | WRAP1 | WRAP0 |
| W | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |

= Unimplemented or Reserved

**Figure 11-3. ATD Control Register 0 (ATDCTL0)**

Read: Anytime

Write: Anytime, in special modes always write 0 to Reserved Bit 7.

**Table 11-1. ATDCTL0 Field Descriptions**

| Field | Description |
|---|---|
| | |
| 3-0 WRAP[3-0] | **Wrap Around Channel Select Bits** — These bits determine the channel for wrap around when doing multi-channel conversions. The coding is summarized in Table 11-2. |

**Table 11-2. Multi-Channel Wrap Around Coding**

| WRAP3 | WRAP2 | WRAP1 | WRAP0 | Multiple Channel Conversions (MULT = 1) Wraparound to AN0 after Converting |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Reserved[1] |
| 0 | 0 | 0 | 1 | AN1 |
| 0 | 0 | 1 | 0 | AN2 |
| 0 | 0 | 1 | 1 | AN3 |
| 0 | 1 | 0 | 0 | AN4 |
| 0 | 1 | 0 | 1 | AN5 |
| 0 | 1 | 1 | 0 | AN6 |
| 0 | 1 | 1 | 1 | AN7 |
| 1 | 0 | 0 | 0 | AN7 |
| 1 | 0 | 0 | 1 | AN7 |
| 1 | 0 | 1 | 0 | AN7 |
| 1 | 0 | 1 | 1 | AN7 |
| 1 | 1 | 0 | 0 | AN7 |
| 1 | 1 | 0 | 1 | AN7 |
| 1 | 1 | 1 | 0 | AN7 |
| 1 | 1 | 1 | 1 | AN7 |

Module Base + 0x00X2

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R<br>W | ID14 | ID13 | ID12 | ID11 | ID10 | ID9 | ID8 | ID7 |
| Reset: | x | x | x | x | x | x | x | x |

**Figure 18-28. Identifier Register 2 (IDR2) — Extended Identifier Mapping**

**Table 18-29. IDR2 Register Field Descriptions — Extended**

| Field | Description |
|---|---|
| 7-0<br>ID[14:7] | **Extended Format Identifier —** The identifiers consist of 29 bits (ID[28:0]) for the extended format. ID28 is the most significant bit and is transmitted first on the CAN bus during the arbitration procedure. The priority of an identifier is defined to be highest for the smallest binary number. |

Module Base + 0x00X3

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R<br>W | ID6 | ID5 | ID4 | ID3 | ID2 | ID1 | ID0 | RTR |
| Reset: | x | x | x | x | x | x | x | x |

**Figure 18-29. Identifier Register 3 (IDR3) — Extended Identifier Mapping**

**Table 18-30. IDR3 Register Field Descriptions — Extended**

| Field | Description |
|---|---|
| 7-1<br>ID[6:0] | **Extended Format Identifier —** The identifiers consist of 29 bits (ID[28:0]) for the extended format. ID28 is the most significant bit and is transmitted first on the CAN bus during the arbitration procedure. The priority of an identifier is defined to be highest for the smallest binary number. |
| 0<br>RTR | **Remote Transmission Request** — This flag reflects the status of the remote transmission request bit in the CAN frame. In the case of a receive buffer, it indicates the status of the received frame and supports the transmission of an answering frame in software. In the case of a transmit buffer, this flag defines the setting of the RTR bit to be sent.<br>0 Data frame<br>1 Remote frame |

**Table 20-2. SCIBDH and SCIBDL Field Descriptions**

| Field | Description |
|---|---|
| 7<br>IREN | **Infrared Enable Bit** — This bit enables/disables the infrared modulation/demodulation submodule.<br>0 IR disabled<br>1 IR enabled |
| 6:5<br>TNP[1:0] | **Transmitter Narrow Pulse Bits** — These bits enable whether the SCI transmits a 1/16, 3/16, 1/32 or 1/4 narrow pulse. See Table 20-3. |
| 4:0<br>7:0<br>SBR[12:0] | **SCI Baud Rate Bits** — The baud rate for the SCI is determined by the bits in this register. The baud rate is calculated two different ways depending on the state of the IREN bit.<br>The formulas for calculating the baud rate are:<br>When IREN = 0 then,<br>SCI baud rate = SCI bus clock / (16 x SBR[12:0])<br>When IREN = 1 then,<br>SCI baud rate = SCI bus clock / (32 x SBR[12:1])<br>**Note:** The baud rate generator is disabled after reset and not started until the TE bit or the RE bit is set for the first time. The baud rate generator is disabled when (SBR[12:0] = 0 and IREN = 0) or (SBR[12:1] = 0 and IREN = 1).<br>**Note:** Writing to SCIBDH has no effect without writing to SCIBDL, because writing to SCIBDH puts the data in a temporary location until SCIBDL is written to. |

**Table 20-3. IRSCI Transmit Pulse Width**

| TNP[1:0] | Narrow Pulse Width |
|---|---|
| 11 | 1/4 |
| 10 | 1/32 |
| 01 | 1/16 |
| 00 | 3/16 |

## 20.3.2.2 SCI Control Register 1 (SCICR1)

Module Base + 0x0002

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R<br>W | LOOPS | SCISWAI | RSRC | M | WAKE | ILT | PE | PT |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Figure 20-5. SCI Control Register 1 (SCICR1)**

Read: Anytime, if AMAP = 0.

Write: Anytime, if AMAP = 0.

**NOTE**

This register is only visible in the memory map if AMAP = 0 (reset condition).

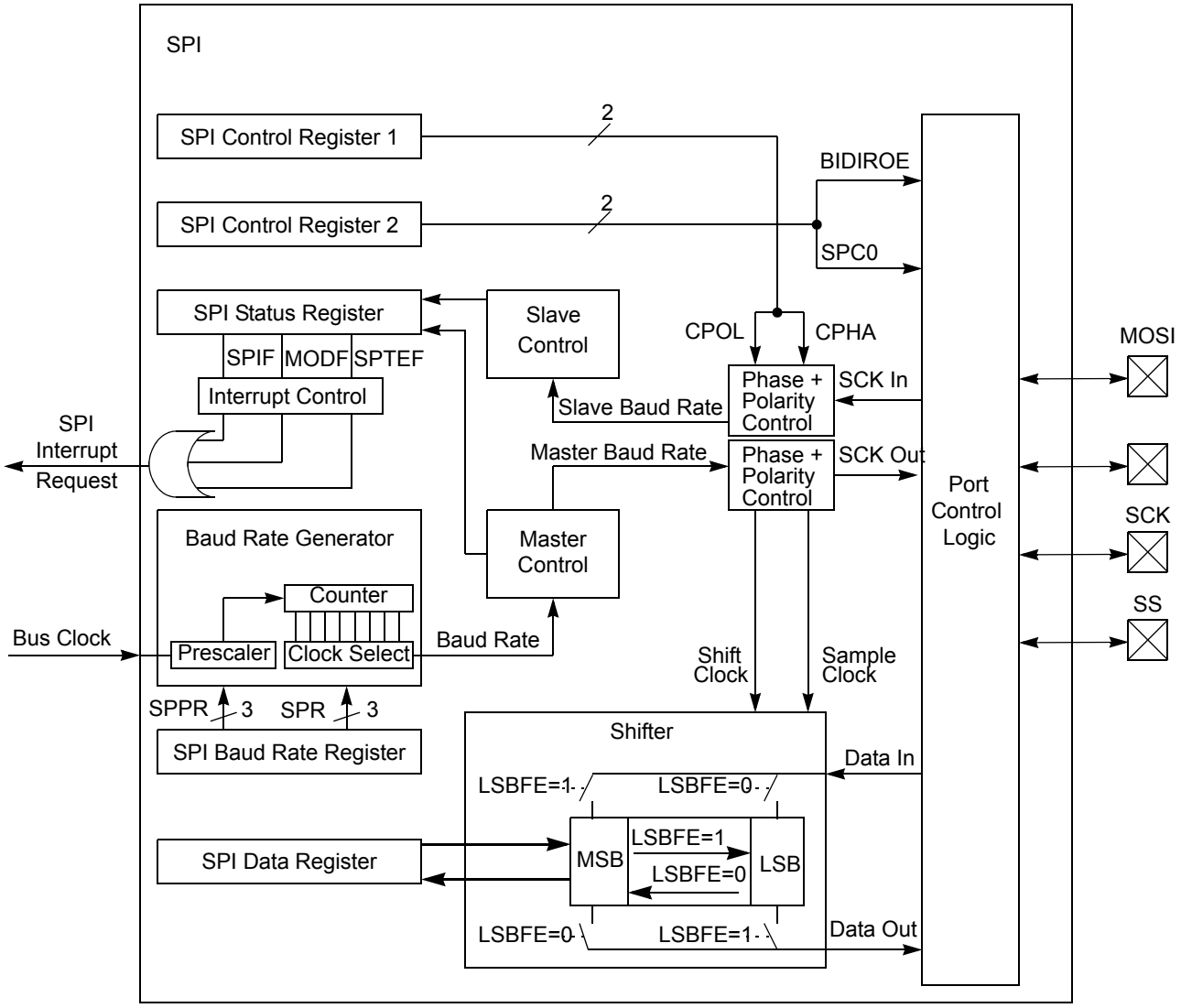


**Figure 21-1. SPI Block Diagram**

## 21.2 External Signal Description

This section lists the name and description of all ports including inputs and outputs that do, or may, connect off chip. The SPI module has a total of four external pins.

### 21.2.1 MOSI — Master Out/Slave In Pin

This pin is used to transmit data out of the SPI module when it is configured as a master and receive data when it is configured as slave.

**Table 21-3. SPICR2 Field Descriptions**

| Field | Description |
|---|---|
| 6<br>XFRW | **Transfer Width —** This bit is used for selecting the data transfer width. If 8-bit transfer width is selected, SPIDRL becomes the dedicated data register and SPIDRH is unused. If 16-bit transfer width is selected, SPIDRH and SPIDRL form a 16-bit data register. Please refer to Section 21.3.2.4, “SPI Status Register (SPISR) for information about transmit/receive data handling and the interrupt flag clearing mechanism. In master mode, a change of this bit will abort a transmission in progress and force the SPI system into idle state.<br>0 8-bit Transfer Width (n = 8)[1]<br>1 16-bit Transfer Width (n = 16)[1] |
| 4<br>MODFEN | **Mode Fault Enable Bit** — This bit allows the MODF failure to be detected. If the SPI is in master mode and MODFEN is cleared, then the $\overline{SS}$ port pin is not used by the SPI. In slave mode, the $\overline{SS}$ is available only as an input regardless of the value of MODFEN. For an overview on the impact of the MODFEN bit on the $\overline{SS}$ port pin configuration, refer to Table 21-2. In master mode, a change of this bit will abort a transmission in progress and force the SPI system into idle state.<br>0 $\overline{SS}$ port pin is not used by the SPI.<br>1 $\overline{SS}$ port pin with MODF feature. |
| 3<br>BIDIROE | **Output Enable in the Bidirectional Mode of Operation** — This bit controls the MOSI and MISO output buffer of the SPI, when in bidirectional mode of operation (SPC0 is set). In master mode, this bit controls the output buffer of the MOSI port, in slave mode it controls the output buffer of the MISO port. In master mode, with SPC0 set, a change of this bit will abort a transmission in progress and force the SPI into idle state.<br>0 Output buffer disabled.<br>1 Output buffer enabled. |
| 1<br>SPISWAI | **SPI Stop in Wait Mode Bit** — This bit is used for power conservation while in wait mode.<br>0 SPI clock operates normally in wait mode.<br>1 Stop SPI clock generation when in wait mode. |
| 0<br>SPC0 | **Serial Pin Control Bit 0** — This bit enables bidirectional pin configurations as shown in Table 21-4. In master mode, a change of this bit will abort a transmission in progress and force the SPI system into idle state. |

[1] n is used later in this document as a placeholder for the selected transfer width.

**Table 21-4. Bidirectional Pin Configurations**

| Pin Mode | SPC0 | BIDIROE | MISO | MOSI |
|---|---|---|---|---|
| **Master Mode of Operation** | | | | |
| Normal | 0 | X | Master In | Master Out |
| Bidirectional | 1 | 0 | MISO not used by SPI | Master In |
| | | 1 | | Master I/O |
| **Slave Mode of Operation** | | | | |
| Normal | 0 | X | Slave Out | Slave In |
| Bidirectional | 1 | 0 | Slave In | MOSI not used by SPI |
| | | 1 | Slave I/O | |

### 23.3.2.2 Timer Compare Force Register (CFORC)

Module Base + 0x0001

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| W | FOC7 | FOC6 | FOC5 | FOC4 | FOC3 | FOC2 | FOC1 | FOC0 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Figure 23-7. Timer Compare Force Register (CFORC)**

Read: Anytime but will always return 0x0000 (1 state is transient)

Write: Anytime

**Table 23-3. CFORC Field Descriptions**

**Note:** Writing to unavailable bits has no effect. Reading from unavailable bits return a zero.

| Field | Description |
|---|---|
| 7:0<br>FOC[7:0] | **Note: Force Output Compare Action for Channel 7:0** — A write to this register with the corresponding data bit(s) set causes the action which is programmed for output compare “x” to occur immediately. The action taken is the same as if a successful comparison had just taken place with the TCx register except the interrupt flag does not get set. A channel 7 event, which can be a counter overflow when TTOV[7] is set or a successful output compare on channel 7, overrides any channel 6:0 compares. If forced output compare on any channel occurs at the same time as the successful output compare then forced output compare action will take precedence and interrupt flag won’t get set. |

### 23.3.2.3 Output Compare 7 Mask Register (OC7M)

Module Base + 0x0002

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R<br>W | OC7M7 | OC7M6 | OC7M5 | OC7M4 | OC7M3 | OC7M2 | OC7M1 | OC7M0 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Figure 23-8. Output Compare 7 Mask Register (OC7M)**

Read: Anytime

Write: Anytime

- Fast sector erase and phrase program operation
- Ability to read the P-Flash memory while programming a word in the EEPROM memory
- Flexible protection scheme to prevent accidental program or erase of P-Flash memory

#### 25.1.2.2 EEPROM Features

- 1 Kbyte of EEPROM memory composed of one 1 Kbyte Flash block divided into 256 sectors of 4 bytes
- Single bit fault correction and double bit fault detection within a word during read operations
- Automated program and erase algorithm with verify and generation of ECC parity bits
- Fast sector erase and word program operation
- Protection scheme to prevent accidental program or erase of EEPROM memory
- Ability to program up to four words in a burst sequence

#### 25.1.2.3 Other Flash Module Features

- No external high-voltage power supply required for Flash memory program and erase operations
- Interrupt generation on Flash command completion and Flash error detection
- Security mechanism to prevent unauthorized access to the Flash memory

### 25.1.3 Block Diagram

The block diagram of the Flash module is shown in Figure 25-1.

During the reset sequence, fields DPOPEN and DPS of the EEPROT register are loaded with the contents of the EEPROM protection byte in the Flash configuration field at global address 0x3_FF0D located in P-Flash memory (see Table 25-4) as indicated by reset condition F in Table 25-23. To change the EEPROM protection that will be loaded during the reset sequence, the P-Flash sector containing the EEPROM protection byte must be unprotected, then the EEPROM protection byte must be programmed. If a double bit fault is detected while reading the P-Flash phrase containing the EEPROM protection byte during the reset sequence, the DPOPEN bit will be cleared and DPS bits will be set to leave the EEPROM memory fully protected.

Trying to alter data in any protected area in the EEPROM memory will result in a protection violation error and the FPVIOL bit will be set in the FSTAT register. Block erase of the EEPROM memory is not possible if any of the EEPROM sectors are protected.

**Table 25-22. EEPROT Field Descriptions**

| Field | Description |
|---|---|
| 7<br>DPOPEN | EEPROM Protection Control<br>0 Enables EEPROM memory protection from program and erase with protected address range defined by DPS bits<br>1 Disables EEPROM memory protection from program and erase |
| 4–0<br>DPS[4:0] | **EEPROM Protection Size** — The DPS[4:0] bits determine the size of the protected area in the EEPROM memory as shown inTable 25-23 . |

**Table 25-23. EEPROM Protection Address Range**

| DPS[4:0] | Global Address Range | Protected Size |
|---|---|---|
| 00000 | 0x0_0400 – 0x0_041F | 32 bytes |
| 00001 | 0x0_0400 – 0x0_043F | 64 bytes |
| 00010 | 0x0_0400 – 0x0_045F | 96 bytes |
| 00011 | 0x0_0400 – 0x0_047F | 128 bytes |
| 00100 | 0x0_0400 – 0x0_049F | 160 bytes |
| 00101 | 0x0_0400 – 0x0_04BF | 192 bytes |
| The Protection Size goes on enlarging in step of 32 bytes, for each DPS value increasing of one.<br>.<br>.<br>. | | |
| 11111 - to - 11111 | 0x0_0400 – 0x0_07FF | 1,024 bytes |

**Table 25-29. EEPROM Commands**

| FCMD | Command | Function on EEPROM Memory |
|---|---|---|
| 0x08 | Erase All Blocks | Erase all EEPROM (and P-Flash) blocks.<br>An erase of all Flash blocks is only possible when the FPLDIS, FPHDIS, and FPOPEN bits in the FPROT register and the DPOPEN bit in the EEPROT register are set prior to launching the command. |
| 0x09 | Erase Flash Block | Erase a EEPROM (or P-Flash) block.<br>An erase of the full EEPROM block is only possible when DPOPEN bit in the EEPROT register is set prior to launching the command. |
| 0x0B | Unsecure Flash | Supports a method of releasing MCU security by erasing all EEPROM (and P-Flash) blocks and verifying that all EEPROM (and P-Flash) blocks are erased. |
| 0x0D | Set User Margin Level | Specifies a user margin read level for the EEPROM block. |
| 0x0E | Set Field Margin Level | Specifies a field margin read level for the EEPROM block (special modes only). |
| 0x10 | Erase Verify EEPROM Section | Verify that a given number of words starting at the address provided are erased. |
| 0x11 | Program EEPROM | Program up to four words in the EEPROM block. |
| 0x12 | Erase EEPROM Sector | Erase all bytes in a sector of the EEPROM block. |

## 25.4.5 Allowed Simultaneous P-Flash and EEPROM Operations

Only the operations marked ‘OK’ in Table 25-30 are permitted to be run simultaneously on the Program Flash and EEPROM blocks. Some operations cannot be executed simultaneously because certain hardware resources are shared by the two memories. The priority has been placed on permitting Program Flash reads while program and erase operations execute on the EEPROM, providing read (P-Flash) while write (EEPROM) functionality.

**Table 25-30. Allowed P-Flash and EEPROM Simultaneous Operations**

| | EEPROM | | | | |
|---|---|---|---|---|---|
| **Program Flash** | **Read** | **Margin Read[1]** | **Program** | **Sector Erase** | **Mass Erase[2]** |
| **Read** | | OK | OK | OK | |
| **Margin Read[1]** | | | | | |
| **Program** | | | | | |
| **Sector Erase** | | | | | |
| **Mass Erase[2]** | | | | | OK |

1 A ‘Margin Read’ is any read after executing the margin setting commands ‘Set User Margin Level’ or ‘Set Field Margin Level’ with anything but the ‘normal’ level specified. See the Note on margin settings in Section 25.4.6.12 and Section 25.4.6.13.

2 The ‘Mass Erase’ operations are commands ‘Erase All Blocks’ and ‘Erase Flash Block’

## 27.3 Memory Map and Registers

This section describes the memory map and registers for the Flash module. Read data from unimplemented memory space in the Flash module is undefined. Write access to unimplemented or reserved memory space in the Flash module will be ignored by the Flash module.

**CAUTION**

Writing to the Flash registers while a Flash command is executing (that is indicated when the value of flag CCIF reads as ’0’) is not allowed. If such action is attempted the write operation will not change the register value.

Writing to the Flash registers is allowed when the Flash is not busy executing commands (CCIF = 1) and during initialization right after reset, despite the value of flag CCIF in that case (refer to Section 27.6 for a complete description of the reset sequence).

.

**Table 27-2. FTMRG Memory Map**

| Global Address (in Bytes) | Size (Bytes) | Description |
|---|---|---|
| 0x0_0000 - 0x0_03FF | 1,024 | Register Space |
| 0x0_0400 – 0x0_0BFF | 2,048 | EEPROM Memory |
| 0x0_4000 – 0x0_7FFF | 16,284 | NVMRES[1]=1 : NVM Resource area (see Figure 27-3) |
| 0x3_0000 – 0x3_FFFF | 65,536 | P-Flash Memory |

[1] See NVMRES description in Section 27.4.3

### 27.3.1 Module Memory Map

The S12 architecture places the P-Flash memory between global addresses 0x3_0000 and 0x3_FFFF as shown in Table 27-3.The P-Flash memory map is shown in Figure 27-2.

**Table 27-3. P-Flash Memory Addressing**

| Global Address | Size (Bytes) | Description |
|---|---|---|
| 0x3_0000 – 0x3_FFFF | 64 K | P-Flash Block<br>Contains Flash Configuration Field<br>(see Table 27-4) |

## 28.4.7 Interrupts

The Flash module can generate an interrupt when a Flash command operation has completed or when a Flash command operation has detected an ECC fault.

**Table 28-66. Flash Interrupt Sources**

| Interrupt Source | Interrupt Flag | Local Enable | Global (CCR) Mask |
|---|---|---|---|
| Flash Command Complete | CCIF (FSTAT register) | CCIE (FCNFG register) | I Bit |
| ECC Double Bit Fault on Flash Read | DFDIF (FERSTAT register) | DFDIE (FERCNFG register) | I Bit |
| ECC Single Bit Fault on Flash Read | SFDIF (FERSTAT register) | SFDIE (FERCNFG register) | I Bit |

**NOTE**

Vector addresses and their relative interrupt priority are determined at the MCU level.

### 28.4.7.1 Description of Flash Interrupt Operation

The Flash module uses the CCIF flag in combination with the CCIE interrupt enable bit to generate the Flash command interrupt request. The Flash module uses the DFDIF and SFDIF flags in combination with the DFDIE and SFDIE interrupt enable bits to generate the Flash error interrupt request. For a detailed description of the register bits involved, refer to Section 28.3.2.5, “Flash Configuration Register (FCNFG)”, Section 28.3.2.6, “Flash Error Configuration Register (FERCNFG)”, Section 28.3.2.7, “Flash Status Register (FSTAT)”, and Section 28.3.2.8, “Flash Error Status Register (FERSTAT)”.

The logic used for generating the Flash module interrupts is shown in Figure 28-27.

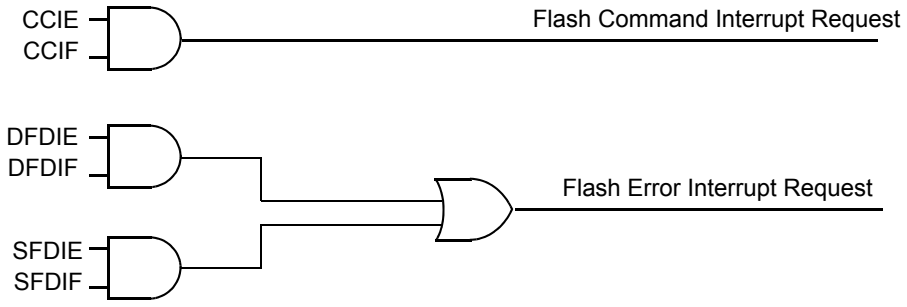


**Figure 28-27. Flash Module Interrupts Implementation**

### 28.4.8 Wait Mode

The Flash module is not affected if the MCU enters wait mode. The Flash module can recover the MCU from wait via the CCIF interrupt (see Section 28.4.7, “Interrupts”).

### 28.4.9 Stop Mode

If a Flash command is active (CCIF = 0) when the MCU requests stop mode, the current Flash operation will be completed before the MCU is allowed to enter stop mode.

## 28.5 Security

The Flash module provides security information to the MCU. The Flash security state is defined by the SEC bits of the FSEC register (see Table 28-11). During reset, the Flash module initializes the FSEC register using data read from the security byte of the Flash configuration field at global address 0x3_FF0F. The security state out of reset can be permanently changed by programming the security byte assuming that the MCU is starting from a mode where the necessary P-Flash erase and program commands are available and that the upper region of the P-Flash is unprotected. If the Flash security byte is successfully programmed, its new value will take affect after the next MCU reset.

The following subsections describe these security-related subjects:

- Unsecuring the MCU using Backdoor Key Access
- Unsecuring the MCU in Special Single Chip Mode using BDM
- Mode and Security Effects on Flash Command Availability

### 28.5.1 Unsecuring the MCU using Backdoor Key Access

The MCU may be unsecured by using the backdoor key access feature which requires knowledge of the contents of the backdoor keys (four 16-bit words programmed at addresses 0x3_FF00-0x3_FF07). If the KEYEN[1:0] bits are in the enabled state (see Section 28.3.2.2), the Verify Backdoor Access Key command (see Section 28.4.6.11) allows the user to present four prospective keys for comparison to the keys stored in the Flash memory via the Memory Controller. If the keys presented in the Verify Backdoor Access Key command match the backdoor keys stored in the Flash memory, the SEC bits in the FSEC register (see Table 28-11) will be changed to unsecure the MCU. Key values of 0x0000 and 0xFFFF are not permitted as backdoor keys. While the Verify Backdoor Access Key command is active, P-Flash memory and EEPROM memory will not be available for read access and will return invalid data.