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Details	
Product Status	Active
Core Processor	12V1
Core Size	16-Bit
Speed	25MHz
Connectivity	CANbus, IrDA, LINbus, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	54
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3.13V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s9s12g128f0mlhr

Table 1-25. 100-Pin LQFP Pinout for S12GA96 and S12GA128

	Function <----lowest-----PRIORITY-----highest---->				Power Supply	Internal Pull Resistor	
Package Pin	Pin	2nd Func.	3rd Func.	4th Func.		CTRL	Reset State
86	PS4	MISO0	—	—	V_{DDX}	PERS/PPSS	Up
87	PS5	MOSI0	—	—	V_{DDX}	PERS/PPSS	Up
88	PS6	SCK0	—	—	V_{DDX}	PERS/PPSS	Up
89	PS7	API_EXTCLK	$\overline{SS0}$	—	V_{DDX}	PERS/PPSS	Up
90	VSSX2	—	—	—	—	—	—
91	VDDX2	—	—	—	—	—	—
92	PM0	RXCAN	—	—	V_{DDX}	PERM/PPSM	Disabled
93	PM1	TXCAN	—	—	V_{DDX}	PERM/PPSM	Disabled
94	PD4	—	—	—	V_{DDX}	PUCR/PUPDE	Disabled
95	PD5	—	—	—	V_{DDX}	PUCR/PUPDE	Disabled
96	PD6	—	—	—	V_{DDX}	PUCR/PUPDE	Disabled
97	PD7	—	—	—	V_{DDX}	PUCR/PUPDE	Disabled
98	PM2	RXD2	—	—	V_{DDX}	PERM/PPSM	Disabled
99	PM3	TXD2	—	—	V_{DDX}	PERM/PPSM	Disabled
100	PJ7	KWJ7	$\overline{SS2}$	—	V_{DDX}	PERJ/PPSJ	Up

[1] The regular I/O characteristics (see Section A.2, “I/O Characteristics”) apply if the EXTAL/XTAL function is disabled

Table 2-14. Port P Pins PP7-0 (continued)

PP3-PP2	• Except 20 TSSOP: The PWM channels 3 and 2 signal are mapped to these pins when used with the PWM function. The enabled PWM channel forces the I/O state to be an output. • Except 20 TSSOP: The ADC ETRIG 3 and 2 signal are mapped to these pins when used with the ADC function. The enabled external trigger function has no effect on the I/O state. Refer to Section 2.6.4, “ADC External Triggers ETRIG3-0”. • Except 20 TSSOP: Pin interrupts can be generated if enabled in input or output mode. • Signal priority: Except 20 TSSOP: PWM > GPO
PP1	• Except 20 TSSOP: The PWM channel 1 signal is mapped to this pin when used with the PWM function. The enabled PWM channel forces the I/O state to be an output. • Except 100 LQFP and 20 TSSOP: The ECLKX2 signal is mapped to this pin when used with the external clock function. The enabled ECLKX2 forces the I/O state to an output. • Except 20 TSSOP: The ADC ETRIG1 signal is mapped to this pin when used with the ADC function. The enabled external trigger function has no effect on the I/O state. Refer to Section 2.6.4, “ADC External Triggers ETRIG3-0”. • Except 20 TSSOP: Pin interrupts can be generated if enabled in input or output mode. • Signal priority: Except 100 LQFP and 20 TSSOP: PWM1 > ECLKX2 > GPO 100 LQFP: PWM1 > GPO
PP0	• Except 20 TSSOP: The PWM channel 0 signal is mapped to this pin when used with the PWM function. The enabled PWM channel forces the I/O state to be an output. • Except 100 LQFP and 20 TSSOP: The API_EXTCLK signal is mapped to this pin when used with the external clock function. If the Autonomous Periodic Interrupt clock is enabled and routed here the I/O state is forced to output. • Except 20 TSSOP: The ADC ETRIG0 signal is mapped to this pin when used with the ADC function. The enabled external trigger function has no effect on the I/O state. Refer to Section 2.6.4, “ADC External Triggers ETRIG3-0”. • Except 20 TSSOP: Pin interrupts can be generated if enabled in input or output mode. • Signal priority: Except 100 LQFP and 20 TSSOP: PWM0 > API_EXTCLK > GPO 100 LQFP: PWM0 > GPO

2.4.3.58 Port AD Pull Enable Register (PER1AD)

Address 0x0279 Access: User read/write[1]

	7	6	5	4	3	2	1	0
R W	PER1AD7	PER1AD6	PER1AD5	PER1AD4	PER1AD3	PER1AD2	PER1AD1	PER1AD0
Reset	0	0	0	0	0	0	0	0

Figure 2-57. Port AD Pullup Enable Register (PER1AD)

[1] Read: Anytime
Write: Anytime

Table 2-84. PER1AD Register Field Descriptions

Field	Description
7-0 PER1AD	**Port AD pull enable**—Enable pull device on input pin This bit controls whether a pull device on the associated port input pin is active. If a pin is used as output this bit has no effect. The polarity is selected by the related polarity select register bit. 1 Pull device enabled 0 Pull device disabled

2.4.3.59 Port AD Polarity Select Register (PPS0AD)

Address 0x027A (G1, G2) Access: User read/write[1]

	7	6	5	4	3	2	1	0
R W	PPS0AD7	PPS0AD6	PPS0AD5	PPS0AD4	PPS0AD3	PPS0AD2	PPS0AD1	PPS0AD0
Reset	0	0	0	0	0	0	0	0

Address 0x027A (G3) Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	0	0	0	0	PPS0AD3	PPS0AD2	PPS0AD1	PPS0AD0
W								
Reset	0	0	0	0	0	0	0	0

Figure 2-58. Port AD Polarity Select Register (PPS0AD)

[1] Read: Anytime
Write: Anytime

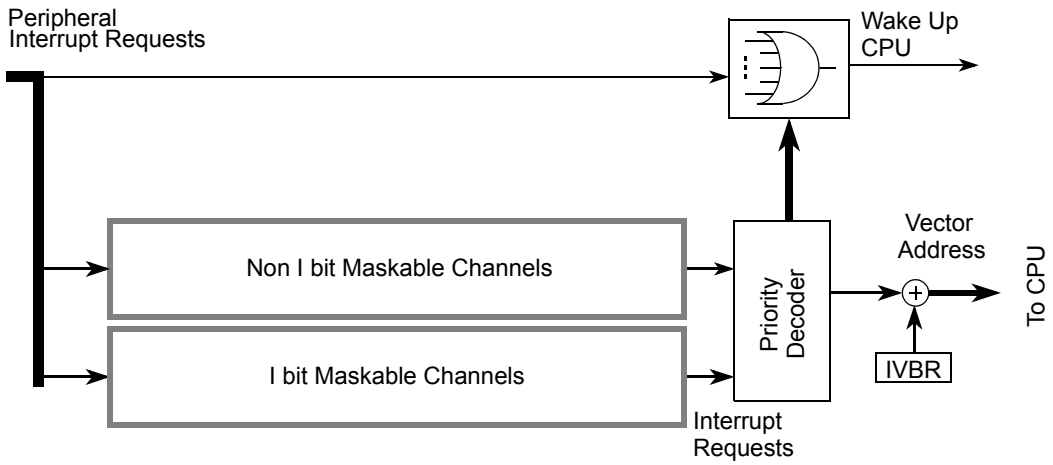

Figure 6-1. INT Block Diagram

6.2 External Signal Description

The INT module has no external signals.

6.3 Memory Map and Register Definition

This section provides a detailed description of all registers accessible in the INT module.

6.3.1 Register Descriptions

This section describes in address order all the INT registers and their individual bits.

6.3.1.1 Interrupt Vector Base Register (IVBR)

Address: 0x0120

	7	6	5	4	3	2	1	0
R W	IVB_ADDR[7:0]							
Reset	1	1	1	1	1	1	1	1

Figure 6-2. Interrupt Vector Base Register (IVBR)

Read: Anytime

Write: Anytime

Global Address	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x3_FF09	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x3_FF0A	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x3_FF0B	Reserved	R	0	0	0	0	0	0	0	0
		W								

= Unimplemented, Reserved

= Implemented (do not alter)

X = Indeterminate

0 = Always read zero

Figure 7-2. BDM Register Summary (continued)

7.3.2.1 BDM Status Register (BDMSTS)

Register Global Address 0x3_FF01

	7	6	5	4	3	2	1	0
R	ENBDM	BDMACT	0	SDV	TRACE	0	UNSEC	0
W								
Reset								
Special Single-Chip Mode	0[1]	1	0	0	0	0	0[2]	0
All Other Modes	0	0	0	0	0	0	0	0

= Unimplemented, Reserved

= Implemented (do not alter)

0 = Always read zero

1 ENBDM is read as 1 by a debugging environment in special single chip mode when the device is not secured or secured but fully erased (Flash). This is because the ENBDM bit is set by the standard BDM firmware before a BDM command can be fully transmitted and executed.

2 UNSEC is read as 1 by a debugging environment in special single chip mode when the device is secured and fully erased, else it is 0 and can only be read if not secure (see also bit description).

Figure 7-3. BDM Status Register (BDMSTS)

Read: All modes through BDM operation when not secured

Write: All modes through BDM operation when not secured, but subject to the following:

— ENBDM should only be set via a BDM hardware command if the BDM firmware commands are needed. (This does not apply in special single chip mode).

— BDMACT can only be set by BDM hardware upon entry into BDM. It can only be cleared by the standard BDM firmware lookup table upon exit from BDM active mode.

— All other bits, while writable via BDM hardware or standard BDM firmware write commands, should only be altered by the BDM hardware or standard firmware lookup table as part of BDM command execution.

7.4.7 Serial Interface Hardware Handshake Protocol

BDM commands that require CPU execution are ultimately treated at the MCU bus rate. Since the BDM clock source can be modified when changing the settings for the VCO frequency (CPMUSYNR), it is very helpful to provide a handshake protocol in which the host could determine when an issued command is executed by the CPU. The BDM clock frequency is always VCO frequency divided by 8. The alternative is to always wait the amount of time equal to the appropriate number of cycles at the slowest possible rate the clock could be running. This sub-section will describe the hardware handshake protocol.

The hardware handshake protocol signals to the host controller when an issued command was successfully executed by the target. This protocol is implemented by a 16 serial clock cycle low pulse followed by a brief speedup pulse in the BKGD pin. This pulse is generated by the target MCU when a command, issued by the host, has been successfully executed (see Figure 7-10). This pulse is referred to as the ACK pulse. After the ACK pulse has finished: the host can start the bit retrieval if the last issued command was a read command, or start a new command if the last command was a write command or a control command (BACKGROUND, GO, GO_UNTIL or TRACE1). The ACK pulse is not issued earlier than 32 serial clock cycles after the BDM command was issued. The end of the BDM command is assumed to be the 16th tick of the last bit. This minimum delay assures enough time for the host to perceive the ACK pulse. Note also that, there is no upper limit for the delay between the command and the related ACK pulse, since the command execution depends upon the CPU bus, which in some cases could be very slow due to long accesses taking place.This protocol allows a great flexibility for the POD designers, since it does not rely on any accurate time measurement or short response time to any event in the serial communication.

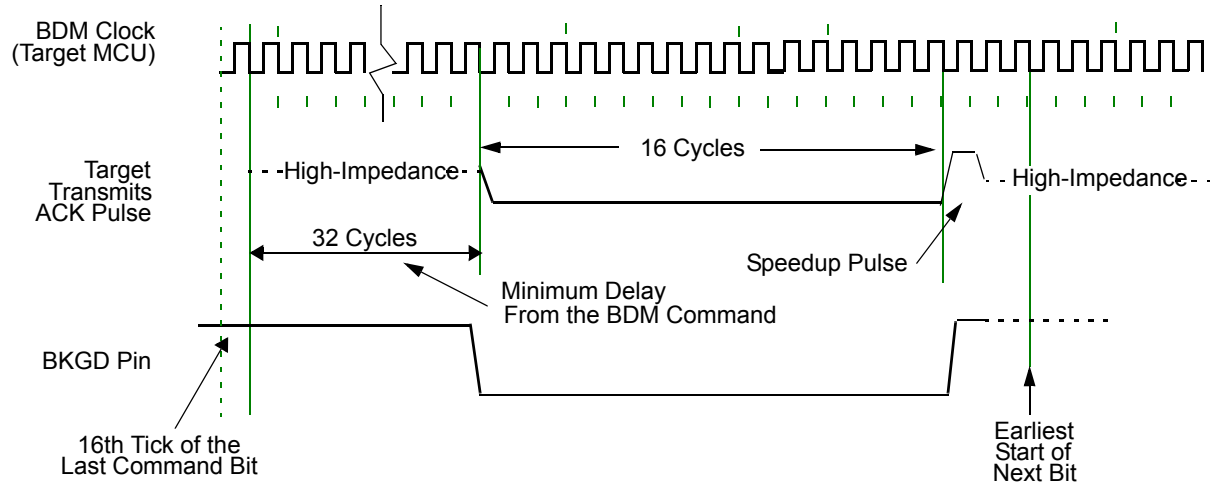

Figure 7-10. Target Acknowledge Pulse (ACK)

NOTE

If the ACK pulse was issued by the target, the host assumes the previous command was executed. If the CPU enters wait or stop prior to executing a hardware command, the ACK pulse will not be issued meaning that the BDM command was not executed. After entering wait or stop mode, the BDM command is no longer pending.

- 4-stage state sequencer for trace buffer control
  - — Tracing session trigger linked to Final State of state sequencer
  - — Begin and End alignment of tracing to trigger

8.1.4 Modes of Operation

The DBG module can be used in all MCU functional modes.

During BDM hardware accesses and whilst the BDM module is active, CPU monitoring is disabled. When the CPU enters active BDM Mode through a BACKGROUND command, the DBG module, if already armed, remains armed.

The DBG module tracing is disabled if the MCU is secure, however, breakpoints can still be generated.

Table 8-2. Mode Dependent Restriction Summary

BDM Enable	BDM Active	MCU Secure	Comparator Matches Enabled	Breakpoints Possible	Tagging Possible	Tracing Possible
x	x	1	Yes	Yes	Yes	No
0	0	0	Yes	Only SWI	Yes	Yes
0	1	0	Active BDM not possible when not enabled			
1	0	0	Yes	Yes	Yes	Yes
1	1	0	No	No	No	No

8.1.5 Block Diagram

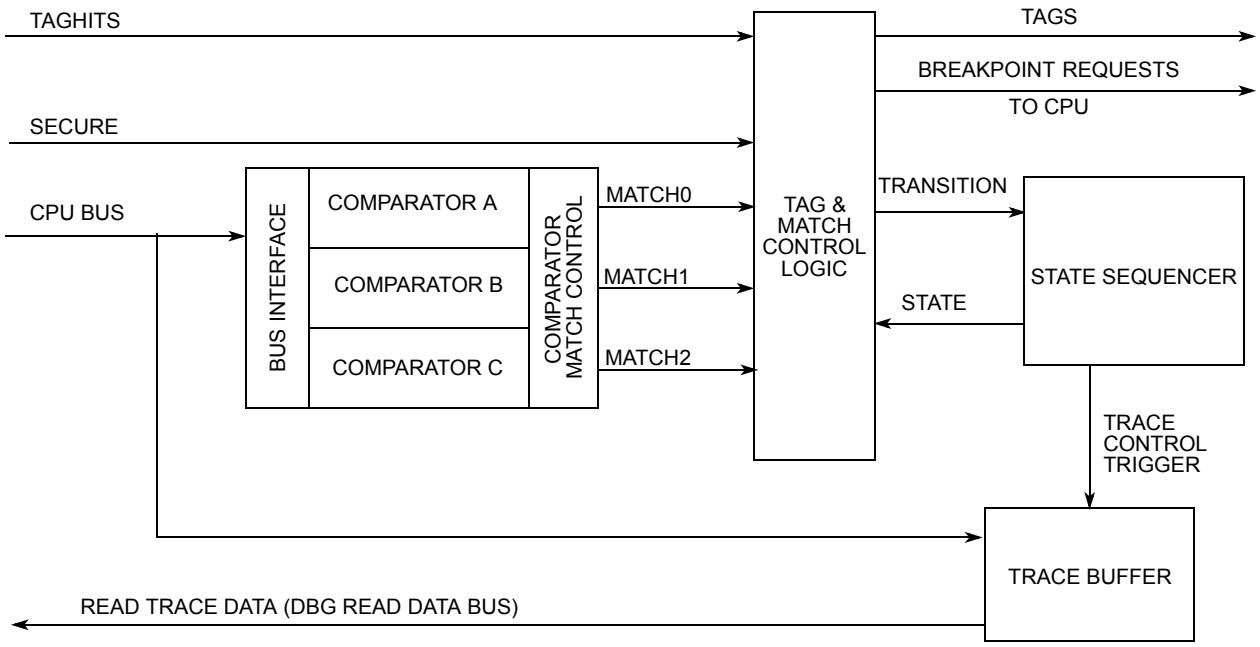

Figure 8-1. Debug Module Block Diagram

Table 8-39. PCH Field Descriptions (continued)

Bit	Description
0 PC16	**Program Counter bit 16**— In Normal and Loop1 mode this bit corresponds to program counter bit 16.

8.4.5.4 Trace Buffer Organization (Compressed Pure PC mode)

Table 8-40. Trace Buffer Organization Example (Compressed PurePC mode)

Mode	Line Number	2-bits	6-bits	6-bits	6-bits
		Field 3	Field 2	Field 1	Field 0
Compressed Pure PC Mode	Line 1	00	PC1 (Initial 18-bit PC Base Address)		
	Line 2	11	PC4	PC3	PC2
	Line 3	01	0	0	PC5
	Line 4	00	PC6 (New 18-bit PC Base Address)		
	Line 5	10	0	PC8	PC7
	Line 6	00	PC9 (New 18-bit PC Base Address)		

NOTE

Configured for end aligned triggering in compressed PurePC mode, then after rollover it is possible that the oldest base address is overwritten. In this case all entries between the pointer and the next base address have lost their base address following rollover. For example in Table 8-40 if one line of rollover has occurred, Line 1, PC1, is overwritten with a new entry. Thus the entries on Lines 2 and 3 have lost their base address. For reconstruction of program flow the first base address following the pointer must be used, in the example, Line 4. The pointer points to the oldest entry, Line 2.

Field3 Bits in Compressed Pure PC Modes

Table 8-41. Compressed Pure PC Mode Field 3 Information Bit Encoding

INF1	INF0	TRACE BUFFER ROW CONTENT
0	0	Base PC address TB[17:0] contains a full PC[17:0] value
0	1	Trace Buffer[5:0] contain incremental PC relative to base address zero value
1	0	Trace Buffer[11:0] contain next 2 incremental PCs relative to base address zero value
1	1	Trace Buffer[17:0] contain next 3 incremental PCs relative to base address zero value

Each time that PC[17:6] differs from the previous base PC[17:6], then a new base address is stored. The base address zero value is the lowest address in the 64 address range

The first line of the trace buffer always gets a base PC address, this applies also on rollover.

12.3.2.12.2 Right Justified Result Data (DJM=1)

Module Base +
0x0010 = ATDDR0, 0x0012 = ATDDR1, 0x0014 = ATDDR2, 0x0016 = ATDDR3
0x0018 = ATDDR4, 0x001A = ATDDR5, 0x001C = ATDDR6, 0x001E = ATDDR7

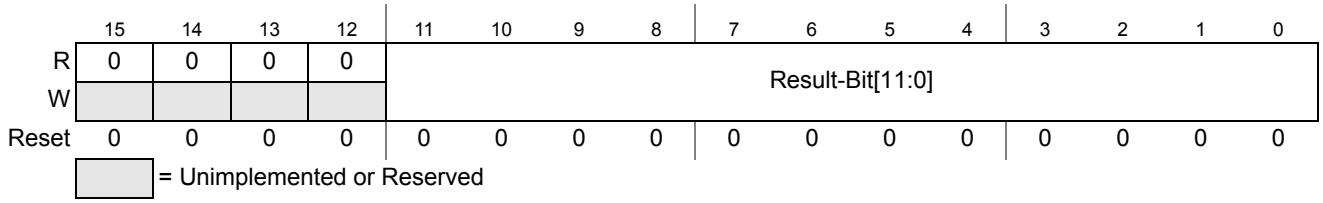

Figure 12-15. Right justified ATD conversion result register (ATDDR*n*)

Table 12-22 shows how depending on the A/D resolution the conversion result is transferred to the ATD result registers for right justified data. Compare is always done using all 12 bits of both the conversion result and the compare value in ATDDRn.

Table 12-22. Conversion result mapping to ATDDRn

A/D resolution	DJM	conversion result mapping to ATDDR*n*
8-bit data	1	Result-Bit[7:0] = result, Result-Bit[11:8]=0000
10-bit data	1	Result-Bit[9:0] = result, Result-Bit[11:10]=00
12-bit data	1	Result-Bit[11:0] = result

14.3.2.12.2 Right Justified Result Data (DJM=1)

Module Base +
0x0010 = ATDDR0, 0x0012 = ATDDR1, 0x0014 = ATDDR2, 0x0016 = ATDDR3
0x0018 = ATDDR4, 0x001A = ATDDR5, 0x001C = ATDDR6, 0x001E = ATDDR7
0x0020 = ATDDR8, 0x0022 = ATDDR9, 0x0024 = ATDDR10, 0x0026 = ATDDR11

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0	0	0	0	Result-Bit[11:0]											
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 14-15. Right justified ATD conversion result register (ATDDR*n*)

Table 14-22 shows how depending on the A/D resolution the conversion result is transferred to the ATD result registers for right justified data. Compare is always done using all 12 bits of both the conversion result and the compare value in ATDDRn.

Table 14-22. Conversion result mapping to ATDDRn

A/D resolution	DJM	conversion result mapping to ATDDR*n*
8-bit data	1	Result-Bit[11:8]=0000, Result-Bit[7:0] = conversion result
10-bit data	1	Result-Bit[11:10]=00, Result-Bit[9:0] = conversion result
12-bit data	1	Result-Bit[11:0] = result

Table 21-3. SPICR2 Field Descriptions

Field	Description
6 XFRW	**Transfer Width —** This bit is used for selecting the data transfer width. If 8-bit transfer width is selected, SPIDRL becomes the dedicated data register and SPIDRH is unused. If 16-bit transfer width is selected, SPIDRH and SPIDRL form a 16-bit data register. Please refer to Section 21.3.2.4, “SPI Status Register (SPISR) for information about transmit/receive data handling and the interrupt flag clearing mechanism. In master mode, a change of this bit will abort a transmission in progress and force the SPI system into idle state. 0 8-bit Transfer Width (n = 8)[1] 1 16-bit Transfer Width (n = 16)[1]
4 MODFEN	**Mode Fault Enable Bit** — This bit allows the MODF failure to be detected. If the SPI is in master mode and MODFEN is cleared, then the $\overline{SS}$ port pin is not used by the SPI. In slave mode, the $\overline{SS}$ is available only as an input regardless of the value of MODFEN. For an overview on the impact of the MODFEN bit on the $\overline{SS}$ port pin configuration, refer to Table 21-2. In master mode, a change of this bit will abort a transmission in progress and force the SPI system into idle state. 0 $\overline{SS}$ port pin is not used by the SPI. 1 $\overline{SS}$ port pin with MODF feature.
3 BIDIROE	**Output Enable in the Bidirectional Mode of Operation** — This bit controls the MOSI and MISO output buffer of the SPI, when in bidirectional mode of operation (SPC0 is set). In master mode, this bit controls the output buffer of the MOSI port, in slave mode it controls the output buffer of the MISO port. In master mode, with SPC0 set, a change of this bit will abort a transmission in progress and force the SPI into idle state. 0 Output buffer disabled. 1 Output buffer enabled.
1 SPISWAI	**SPI Stop in Wait Mode Bit** — This bit is used for power conservation while in wait mode. 0 SPI clock operates normally in wait mode. 1 Stop SPI clock generation when in wait mode.
0 SPC0	**Serial Pin Control Bit 0** — This bit enables bidirectional pin configurations as shown in Table 21-4. In master mode, a change of this bit will abort a transmission in progress and force the SPI system into idle state.

[1] n is used later in this document as a placeholder for the selected transfer width.

Table 21-4. Bidirectional Pin Configurations

Pin Mode	SPC0	BIDIROE	MISO	MOSI
Master Mode of Operation				
Normal	0	X	Master In	Master Out
Bidirectional	1	0	MISO not used by SPI	Master In
		1		Master I/O
Slave Mode of Operation				
Normal	0	X	Slave Out	Slave In
Bidirectional	1	0	Slave In	MOSI not used by SPI
		1	Slave I/O	

Any access to TCNT will clear TFLG2 register if the TFFCA bit in TSCR register is set.

Table 23-17. TRLG2 Field Descriptions

Field	Description
7 TOF	**Timer Overflow Flag** — Set when 16-bit free-running timer overflows from 0xFFFF to 0x0000. Clearing this bit requires writing a one to bit 7 of TFLG2 register while the TEN bit of TSCR1 or PAEN bit of PACTL is set to one (See also TCRE control bit explanation) .

23.3.2.14 Timer Input Capture/Output Compare Registers High and Low 0–7(TCxH and TCxL)

Module Base + 0x0010 = TC0H 0x0018=TC4H
0x0012 = TC1H 0x001A=TC5H
0x0014=TC2H 0x001C=TC6H
0x0016=TC3H 0x001E=TC7H

	15	14	13	12	11	10	9	0
R W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Reset	0	0	0	0	0	0	0	0

Figure 23-22. Timer Input Capture/Output Compare Register x High (TCxH)

Module Base + 0x0011 = TC0L 0x0019 =TC4L
0x0013 = TC1L 0x001B=TC5L
0x0015 =TC2L 0x001D=TC6L
0x0017=TC3L 0x001F=TC7L

	7	6	5	4	3	2	1	0
R W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reset	0	0	0	0	0	0	0	0

Figure 23-23. Timer Input Capture/Output Compare Register x Low (TCxL)

[1] This register is available only when the corresponding channel exists and is reserved if that channel does not exist. Writes to a reserved register have no functional effect. Reads from a reserved register return zeroes.

Depending on the TIOS bit for the corresponding channel, these registers are used to latch the value of the free-running counter when a defined transition is sensed by the corresponding input capture edge detector or to trigger an output action for output compare.

Read: Anytime

Write: Anytime for output compare function.Writes to these registers have no meaning or effect during input capture. All timer input capture/output compare registers are reset to 0x0000.

NOTE

Read/Write access in byte mode for high byte should take place before low byte otherwise it will give a different result.

Table 24-57. Set Field Margin Level Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 001 at command launch
		Set if command not available in current mode (see Table 24-25)
		Set if an invalid FlashBlockSelectionCode[1:0] is supplied (See Table 24-32)[1]
		Set if an invalid margin level setting is supplied
	FPVIOL	None
	MGSTAT1	None
	MGSTAT0	None

1 As defined by the memory map for FTMRG32K1.

CAUTION

Field margin levels must only be used during verify of the initial factory programming.

NOTE

Field margin levels can be used to check that Flash memory contents have adequate margin for data retention at the normal level setting. If unexpected results are encountered when checking Flash memory contents at field margin levels, the Flash memory contents should be erased and reprogrammed.

24.4.6.14 Erase Verify EEPROM Section Command

The Erase Verify EEPROM Section command will verify that a section of code in the EEPROM is erased. The Erase Verify EEPROM Section command defines the starting point of the data to be verified and the number of words.

Table 24-58. Erase Verify EEPROM Section Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x10	Global address [17:16] to identify the EEPROM block
001	Global address [15:0] of the first word to be verified	
010	Number of words to be verified	

Upon clearing CCIF to launch the Erase Verify EEPROM Section command, the Memory Controller will verify the selected section of EEPROM memory is erased. The CCIF flag will set after the Erase Verify EEPROM Section operation has completed. If the section is not erased, it means blank check failed, both MGSTAT bits will be set.

Offset Module Base + 0x000E

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 28-20. Flash Reserved3 Register (FRSV3)

All bits in the FRSV3 register read 0 and are not writable.

28.3.2.15 Flash Reserved4 Register (FRSV4)

This Flash register is reserved for factory testing.

Offset Module Base + 0x000F

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 28-21. Flash Reserved4 Register (FRSV4)

All bits in the FRSV4 register read 0 and are not writable.

28.3.2.16 Flash Option Register (FOPT)

The FOPT register is the Flash option register.

Offset Module Base + 0x0010

	7	6	5	4	3	2	1	0
R	NV[7:0]							
W								
Reset	F[1]	F[1]	F[1]	F[1]	F[1]	F[1]	F[1]	F[1]

= Unimplemented or Reserved

Figure 28-22. Flash Option Register (FOPT)

1 Loaded from IFR Flash configuration field, during reset sequence.

All bits in the FOPT register are readable but are not writable.

During the reset sequence, the FOPT register is loaded from the Flash nonvolatile byte in the Flash configuration field at global address 0x3_FF0E located in P-Flash memory (see Table 28-4) as indicated by reset condition F in Figure 28-22. If a double bit fault is detected while reading the P-Flash phrase containing the Flash nonvolatile byte during the reset sequence, all bits in the FOPT register will be set.

NOTE

User margin levels can be used to check that Flash memory contents have adequate margin for normal level read operations. If unexpected results are encountered when checking Flash memory contents at user margin levels, a potential loss of information has been detected.

28.4.6.13 Set Field Margin Level Command

The Set Field Margin Level command, valid in special modes only, causes the Memory Controller to set the margin level specified for future read operations of the P-Flash or EEPROM block.

Upon clearing CCIF to launch the Set Field Margin Level command, the Memory Controller will set the

Table 28-57. Set Field Margin Level Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x0E	Flash block selection code [1:0]. See Table 28-34
001	Margin level setting.	

field margin level for the targeted block and then set the CCIF flag.

NOTE

When the EEPROM block is targeted, the EEPROM field margin levels are applied only to the EEPROM reads. However, when the P-Flash block is targeted, the P-Flash field margin levels are applied to both P-Flash and EEPROM reads. It is not possible to apply field margin levels to the P-Flash block only.

Valid margin level settings for the Set Field Margin Level command are defined in Table 28-58.

Table 28-58. Valid Set Field Margin Level Settings

CCOB (CCOBIX=001)	Level Description
0x0000	Return to Normal Level
0x0001	User Margin-1 Level[1]
0x0002	User Margin-0 Level[2]
0x0003	Field Margin-1 Level[1]
0x0004	Field Margin-0 Level[2]

[1] Read margin to the erased state

[2] Read margin to the programmed state

Chapter 31
240 KByte Flash Module (S12FTMRG240K2V1)

Table 31-1. Revision History

Revision Number	Revision Date	Sections Affected	Description of Changes
V01.06	23 Jun 2010	31.4.6.2/31-1159 31.4.6.12/31-1166 31.4.6.13/31-1167	Updated description of the commands RD1BLK, MLOADU and MLOADF
V01.07	20 aug 2010	31.4.6.2/31-1159 31.4.6.12/31-1166 31.4.6.13/31-1167	Updated description of the commands RD1BLK, MLOADU and MLOADF
Rev.1.27	31 Jan 2011	31.3.2.9/31-1142	Updated description of protection on Section 31.3.2.9

31.1 Introduction

The FTMRG240K2 module implements the following:

- 240Kbytes of P-Flash (Program Flash) memory
- 4Kbytes of EEPROM memory

The Flash memory is ideal for single-supply applications allowing for field reprogramming without requiring external high voltage sources for program or erase operations. The Flash module includes a memory controller that executes commands to modify Flash memory contents. The user interface to the memory controller consists of the indexed Flash Common Command Object (FCCOB) register which is written to with the command, global address, data, and any required command parameters. The memory controller must complete the execution of a command before the FCCOB register can be written to with a new command.

CAUTION

A Flash word or phrase must be in the erased state before being programmed. Cumulative programming of bits within a Flash word or phrase is not allowed.

31.3.2.9.1 P-Flash Protection Restrictions

The general guideline is that P-Flash protection can only be added and not removed. Table 31-21 specifies all valid transitions between P-Flash protection scenarios. Any attempt to write an invalid scenario to the FPROT register will be ignored. The contents of the FPROT register reflect the active protection scenario. See the FPHS and FPLS bit descriptions for additional restrictions.

Table 31-21. P-Flash Protection Scenario Transitions

From Protection Scenario	To Protection Scenario[1]							
	0	1	2	3	4	5	6	7
0	X	X	X	X				
1		X		X				
2			X	X				
3				X				
4				X	X			
5			X	X	X	X		
6		X		X	X		X	
7	X	X	X	X	X	X	X	X

1 Allowed transitions marked with X, see Figure 31-14 for a definition of the scenarios.

31.3.2.10 EEPROM Protection Register (EEPROT)

The EEPROT register defines which EEPROM sectors are protected against program and erase operations.

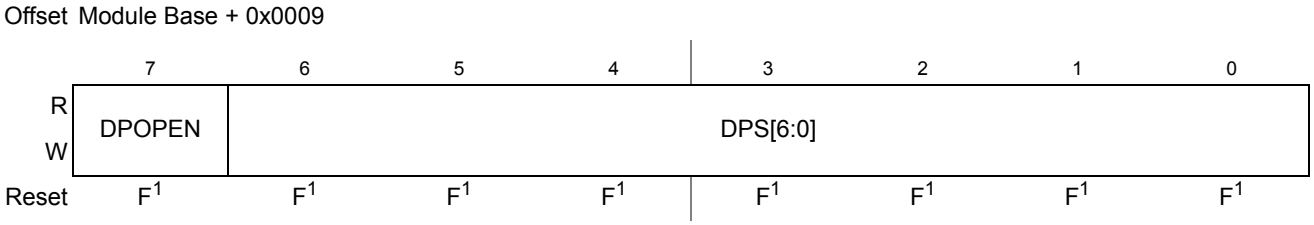

Figure 31-15. EEPROM Protection Register (EEPROT)

1 Loaded from IFR Flash configuration field, during reset sequence.

The (unreserved) bits of the EEPROT register are writable with the restriction that protection can be added but not removed. Writes must increase the DPS value and the DPOPEN bit can only be written from 1 (protection disabled) to 0 (protection enabled). If the DPOPEN bit is set, the state of the DPS bits is irrelevant.

During the reset sequence, fields DPOPEN and DPS of the EEPROT register are loaded with the contents of the EEPROM protection byte in the Flash configuration field at global address 0x3_FF0D located in

0x0020–0x002F Debug Module (DBG)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0029	DBGXAH	R	0	0	0	0	0	0	Bit 17	Bit 16
		W								
0x002A	DBGXAM	R	Bit 15	14	13	12	11	10	9	Bit 8
		W								
0x002B	DBGXAL	R	Bit 7	6	5	4	3	2	1	Bit 0
		W								
0x002C	DBGADH	R	Bit 15	14	13	12	11	10	9	Bit 8
		W								
0x002D	DBGADL	R	Bit 7	6	5	4	3	2	1	Bit 0
		W								
0x002E	DBGADHM	R	Bit 15	14	13	12	11	10	9	Bit 8
		W								
0x002F	DBGADLM	R	Bit 7	6	5	4	3	2	1	Bit 0
		W								

0x0030–0x033 Reserved

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0030-0x0033	Reserved	R	0	0	0	0	0	0	0	0
		W								

0x0034–0x003F Clock and Power Management (CPMU) Map 1 of 2

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0034	CPMU SYNR	R	VCOFRQ[1:0]		SYNDIV[5:0]					
		W								
0x0035	CPMU REFDIV	R	REFFRQ[1:0]		0	0	REFDIV[3:0]			
		W								
0x0036	CPMU POSTDIV	R	0	0	0	POSTDIV[4:0]				
		W								
0x0037	CPMUFLG	R	RTIF	PORF	LVRF	LOCKIF	LOCK	ILAF	OSCIF	UPOSC
		W								
0x0038	CPMUINT	R	RTIE	0	0	LOCKIE	0	0	OSCIE	0
		W								
0x0039	CPMUCLKS	R	PLLSEL	PSTP	0	0	PRE	PCE	RTI OSCSEL	COP OSCSEL
		W								
0x003A	CPMUPLL	R	0	0	FM1	FM0	0	0	0	0
		W								
0x003B	CPMURTI	R	RTDEC	RTR6	RTR5	RTR4	RTR3	RTR2	RTR1	RTR0
		W								
0x003C	CPMUCOP	R	WCOP	RSBCK	0	0	0	CR2	CR1	CR0
		W			WRTMASK					

0x0070–0x09F Analog to Digital Converter (ADC)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x007A	ATDSTAT2H	R	CCF[15:8]							
		W								
0x007B	ATDSTAT2L	R	CCF[7:0]							
		W								
0x007C	ATDDIENH	R	IEN[15:8]							
		W								
0x007D	ATDDIENL	R	IEN[7:0]							
		W								
0x007E	ATDCMPHTH	R	CMPHT[15:8]							
		W								
0x007F	ATDCMPHTL	R	CMPHT[7:0]							
		W								
0x0080-0x0091	ATDDR0	R	See Section 16.3.2.12.1, “Left Justified Result Data (DJM=0)” and Section 16.3.2.12.2, “Right Justified Result Data (DJM=1)”							
		W								
0x0082-0x0083	ATDDR1	R	See Section 16.3.2.12.1, “Left Justified Result Data (DJM=0)” and Section 16.3.2.12.2, “Right Justified Result Data (DJM=1)”							
		W								
0x0084-0x0085	ATDDR2	R	See Section 16.3.2.12.1, “Left Justified Result Data (DJM=0)” and Section 16.3.2.12.2, “Right Justified Result Data (DJM=1)”							
		W								
0x0086-0x0087	ATDDR3	R	See Section 16.3.2.12.1, “Left Justified Result Data (DJM=0)” and Section 16.3.2.12.2, “Right Justified Result Data (DJM=1)”							
		W								
0x0088-0x0089	ATDDR4	R	See Section 16.3.2.12.1, “Left Justified Result Data (DJM=0)” and Section 16.3.2.12.2, “Right Justified Result Data (DJM=1)”							
		W								
0x008A-0x008B	ATDDR5	R	See Section 16.3.2.12.1, “Left Justified Result Data (DJM=0)” and Section 16.3.2.12.2, “Right Justified Result Data (DJM=1)”							
		W								
0x008C-0x008D	ATDDR6	R	See Section 16.3.2.12.1, “Left Justified Result Data (DJM=0)” and Section 16.3.2.12.2, “Right Justified Result Data (DJM=1)”							
		W								
0x008E-0x008F	ATDDR7	R	See Section 16.3.2.12.1, “Left Justified Result Data (DJM=0)” and Section 16.3.2.12.2, “Right Justified Result Data (DJM=1)”							
		W								
0x0090-0x0091	ATDDR8	R	See Section 16.3.2.12.1, “Left Justified Result Data (DJM=0)” and Section 16.3.2.12.2, “Right Justified Result Data (DJM=1)”							
		W								
0x0092-0x0093	ATDDR9	R	See Section 16.3.2.12.1, “Left Justified Result Data (DJM=0)” and Section 16.3.2.12.2, “Right Justified Result Data (DJM=1)”							
		W								
0x0094-0x0095	ATDDR10	R	See Section 16.3.2.12.1, “Left Justified Result Data (DJM=0)” and Section 16.3.2.12.2, “Right Justified Result Data (DJM=1)”							
		W								
0x0096-0x0097	ATDDR11	R	See Section 16.3.2.12.1, “Left Justified Result Data (DJM=0)” and Section 16.3.2.12.2, “Right Justified Result Data (DJM=1)”							
		W								
0x0098-0x0099	ATDDR12	R	See Section 16.3.2.12.1, “Left Justified Result Data (DJM=0)” and Section 16.3.2.12.2, “Right Justified Result Data (DJM=1)”							
		W								
0x009A-0x009B	ATDDR13	R	See Section 16.3.2.12.1, “Left Justified Result Data (DJM=0)” and Section 16.3.2.12.2, “Right Justified Result Data (DJM=1)”							
		W								
0x009C-0x009D	ATDDR14	R	See Section 16.3.2.12.1, “Left Justified Result Data (DJM=0)” and Section 16.3.2.12.2, “Right Justified Result Data (DJM=1)”							
		W								
0x009E-0x009F	ATDDR15	R	See Section 16.3.2.12.1, “Left Justified Result Data (DJM=0)” and Section 16.3.2.12.2, “Right Justified Result Data (DJM=1)”							
		W								