Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	12V1
Core Size	16-Bit
Speed	25MHz
Connectivity	CANbus, IrDA, LINbus, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	54
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3.13V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s9s12g128f0vlhr

The MC9S12G-Family is optimized for lower program memory sizes down to 16k. In order to simplify customer use it features an EEPROM with a small 4 bytes erase sector size.

The MC9S12G-Family deliver all the advantages and efficiencies of a 16-bit MCU while retaining the low cost, power consumption, EMC, and code-size efficiency advantages currently enjoyed by users of NXP's existing 8-bit and 16-bit MCU families. Like the MC9S12XS-Family, the MC9S12G-Family run 16-bit wide accesses without wait states for all peripherals and memories. The MC9S12G-Family is available in 100-pin LQFP, 64-pin LQFP, 48-pin LQFP/QFN, 32-pin LQFP and 20-pin TSSOP package options and aims to maximize the amount of functionality especially for the lower pin count packages. In addition to the I/O ports available in each module, further I/O ports are available with interrupt capability allowing wake-up from stop or wait modes.

1.2 Features

This section describes the key features of the MC9S12G-Family.

1.2.1 MC9S12G-Family Comparison

Table 1-1 provides a summary of different members of the MC9S12G-Family and their features. This information is intended to provide an understanding of the range of functionality offered by this microcontroller family.

Table 1-1. MC9S12G-Family Overview[1]

Feature	S12GN16	S12GNA16	S12GN32	S12GNA32	S12GN48	S12G48	S12GA48	S12G64	S12GA64	S12G96	S12GA96	S12G128	S12GA128	S12G192	S12GA192	S12G240	S12GA240
CPU	CPU12V1																
Flash memory [kBytes]	16	16	32	32	48	48	48	64	64	96	96	128	128	192	192	240	240
EEPROM [kBytes]	0.5	0.5	1	1	1.5	1.5	1.5	2	2	3	3	4	4	4	4	4	4
RAM [kBytes]	1	1	2	2	4	4	4	4	4	8	8	8	8	11	11	11	11
MSCAN	—	—	—	—	—	1	1	1	1	1	1	1	1	1	1	1	1
SCI	1	1	1	1	2	2	2	2	2	3	3	3	3	3	3	3	3
SPI	1	1	1	1	2	2	2	2	2	3	3	3	3	3	3	3	3
16-Bit Timer channels	6	6	6	6	6	6	6	6	6	8	8	8	8	8	8	8	8
8-Bit PWM channels	6	6	6	6	6	6	6	6	6	8	8	8	8	8	8	8	8
10-Bit ADC channels	8	—	8	—	12	12	—	12	—	12	—	12	—	16	—	16	—
12-Bit ADC channels	—	8	—	8	—	—	12	—	12	—	12	—	12	—	16	—	16
Temperature Sensor	—	—	—	—	—	—	—	—	—	—	—	—	—	—	Yes	—	Yes
RVA	—	—	—	—	—	—	—	—	—	—	—	—	—	—	YES	—	YES
8-Bit DAC	—	—	—	—	—	—	—	—	—	—	—	—	—	—	2	—	2

Table 1-1. MC9S12G-Family Overview[1]

Feature	S12GN16	S12GNA16	S12GN32	S12GNA32	S12GN48	S12G48	S12GA48	S12G64	S12GA64	S12G96	S12GA96	S12G128	S12GA128	S12G192	S12GA192	S12G240	S12GA240
ACMP (analog comparator)	1	1	1	1	1	1	1	1	1	—	—	—	—	—	—	—	—
PLL	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
External osc	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Internal 1 MHz RC oscillator	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
20-pin TSSOP	Yes	—	Yes	—	—	—	—	—	—	—	—	—	—	—	—	—	—
32-pin LQFP	Yes	—	Yes	—	Yes	Yes	—	Yes	—	—	—	—	—	—	—	—	—
48-pin LQFP	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
48-pin QFN	Yes	Yes	Yes	Yes	—	—	—	—	—	—	—	—	—	—	—	—	—
64-pin LQFP	—	—	—	—	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
100-pin LQFP	—	—	—	—	—	—	—	—	—	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
KGD	—	—	—	—	—	—	—	—	—	—	—	—	—	—	Yes	—	Yes
Supply voltage	3.13 V – 5.5 V																
Execution speed	Static – 25 MHz																

[1] Not all peripherals are available in all package types

Table 1-2shows the maximum number of peripherals or peripheral channels per package type. Not all peripherals are available at the same time. The maximum number of peripherals is also limited by the device chosen as per Table 1-1.

Table 1-2. Maximum Peripheral Availability per Package

Peripheral	20 TSSOP	32 LQFP	48 QFN	48 LQFP	64 LQFP	100 LQFP	KGD (Die)
MSCAN	—	Yes	—	Yes	Yes	Yes	Yes
SCI0	Yes	Yes	Yes	Yes	Yes	Yes	Yes
SCI1	—	Yes	Yes	Yes	Yes	Yes	Yes
SCI2	—	—	—	Yes	Yes	Yes	Yes
SPI0	Yes	Yes	Yes	Yes	Yes	Yes	Yes
SPI1	—	—	—	Yes	Yes	Yes	Yes
SPI2	—	—	—	—	Yes	Yes	Yes
Timer Channels	4 = 0 … 3	6 = 0 … 5	6 = 0 … 5	8 = 0 … 7	8 = 0 … 7	8 = 0 … 7	8 = 0 … 7
8-Bit PWM Channels	4 = 0 … 3	6 = 0 … 5	6 = 0 … 5	8 = 0 … 7	8 = 0 … 7	8 = 0 … 7	8 = 0 … 7
ADC channels	6 = 0 … 5	8 = 0 … 7	8 = 0 … 7	12 = 0 … 11	16 = 0 … 15	16 = 0 … 15	16 = 0 … 15

1.3.1 S12 16-Bit Central Processor Unit (CPU)

S12 CPU is a high-speed 16-bit processing unit:

- Full 16-bit data paths supports efficient arithmetic operation and high-speed math execution
- Includes many single-byte instructions. This allows much more efficient use of ROM space.
- Extensive set of indexed addressing capabilities, including:
  - Using the stack pointer as an indexing register in all indexed operations
  - Using the program counter as an indexing register in all but auto increment/decrement mode
  - Accumulator offsets using A, B, or D accumulators
  - Automatic index predecrement, preincrement, postdecrement, and postincrement (by –8 to +8)

1.3.2 On-Chip Flash with ECC

On-chip flash memory on the MC9S12G-Family family features the following:

- Up to 240 Kbyte of program flash memory
  - 32 data bits plus 7 syndrome ECC (error correction code) bits allow single bit error correction and double fault detection
  - Erase sector size 512 bytes
  - Automated program and erase algorithm
  - User margin level setting for reads
  - Protection scheme to prevent accidental program or erase
- Up to 4 Kbyte EEPROM
  - 16 data bits plus 6 syndrome ECC (error correction code) bits allow single bit error correction and double fault detection
  - Erase sector size 4 bytes
  - Automated program and erase algorithm
  - User margin level setting for reads

1.3.3 On-Chip SRAM

- Up to 11 Kbytes of general-purpose RAM

1.3.4 Port Integration Module (PIM)

- Data registers and data direction registers for ports A, B, C, D, E, T, S, M, P, J and AD when used as general-purpose I/O
- Control registers to enable/disable pull devices and select pullups/pulldowns on ports T, S, M, P, J and AD on per-pin basis
- Single control register to enable/disable pull devices on ports A, B, C, D and E, on per-port basis and on BKGD pin
- Control registers to enable/disable open-drain (wired-or) mode on ports S and M

Table 1-17. 64-Pin LQFP Pinout for S12G48 and S12G64

	Function <----lowest-----PRIORITY-----highest---->					Power Supply	Internal Pull Resistor	
Package Pin	Pin	2nd Func.	3rd Func.	4th Func	5th Func		CTRL	Reset State
28	PT4	IOC4	—	—	—	V_{DDX}	PERT/PPST	Disabled
29	PT3	IOC3	—	—	—	V_{DDX}	PERT/PPST	Disabled
30	PT2	IOC2	—	—	—	V_{DDX}	PERT/PPST	Disabled
31	PT1	IOC1	$\overline{IRQ}$	—	—	V_{DDX}	PERT/PPST	Disabled
32	PT0	IOC0	$\overline{XIRQ}$	—	—	V_{DDX}	PERT/PPST	Disabled
33	PAD0	KWAD0	AN0	—	—	V_{DDA}	PER1AD/PPS1AD	Disabled
34	PAD8	KWAD8	AN8	—	—	V_{DDA}	PER0AD/PPS0AD	Disabled
35	PAD1	KWAD1	AN1	—	—	V_{DDA}	PER1AD/PPS1AD	Disabled
36	PAD9	KWAD9	AN9	ACMPO	—	V_{DDA}	PER0ADPPS0AD	Disabled
37	PAD2	KWAD2	AN2	—	—	V_{DDA}	PER1AD/PPS1AD	Disabled
38	PAD10	KWAD10	AN10	ACMPP		V_{DDA}	PER0AD/PPS0AD	Disabled
39	PAD3	KWAD3	AN3	—	—	V_{DDA}	PER1AD/PPS1AD	Disabled
40	PAD11	KWAD11	AN11	ACMPM		V_{DDA}	PER0AD/PPS0AD	Disabled
41	PAD4	KWAD4	AN4	—	—	V_{DDA}	PER1AD/PPS1AD	Disabled
42	PAD12	KWAD12	—	—	—	V_{DDA}	PER0AD/PPS0AD	Disabled
43	PAD5	KWAD5	AN5	—	—	V_{DDA}	PER1AD/PPS1AD	Disabled
44	PAD13	KWAD13	—	—	—	V_{DDA}	PER0AD/PPS0AD	Disabled
45	PAD6	KWAD6	AN6	—	—	V_{DDA}	PER1AD/PPS1AD	Disabled
46	PAD14	KWAD14	—	—	—	V_{DDA}	PER0AD/PPS0AD	Disabled
47	PAD7	KWAD7	AN7	—	—	V_{DDA}	PER1AD/PPS1AD	Disabled
48	PAD15	KWAD15	—	—	—	V_{DDA}	PER0AD/PPS0AD	Disabled
49	VRH	—	—	—	—	—	—	—
50	VDDA	—	—	—	—	—	—	—
51	VSSA	—	—	—	—	—	—	—
52	PS0	RXD0	—	—	—	V_{DDX}	PERS/PPSS	Up
53	PS1	TXD0	—	—	—	V_{DDX}	PERS/PPSS	Up
54	PS2	RXD1	—	—	—	V_{DDX}	PERS/PPSS	Up
55	PS3	TXD1	—	—	—	V_{DDX}	PERS/PPSS	Up
56	PS4	MISO0	—	—	—	V_{DDX}	PERS/PPSS	Up

1.8.7.2 Pinout 64-Pin LQFP

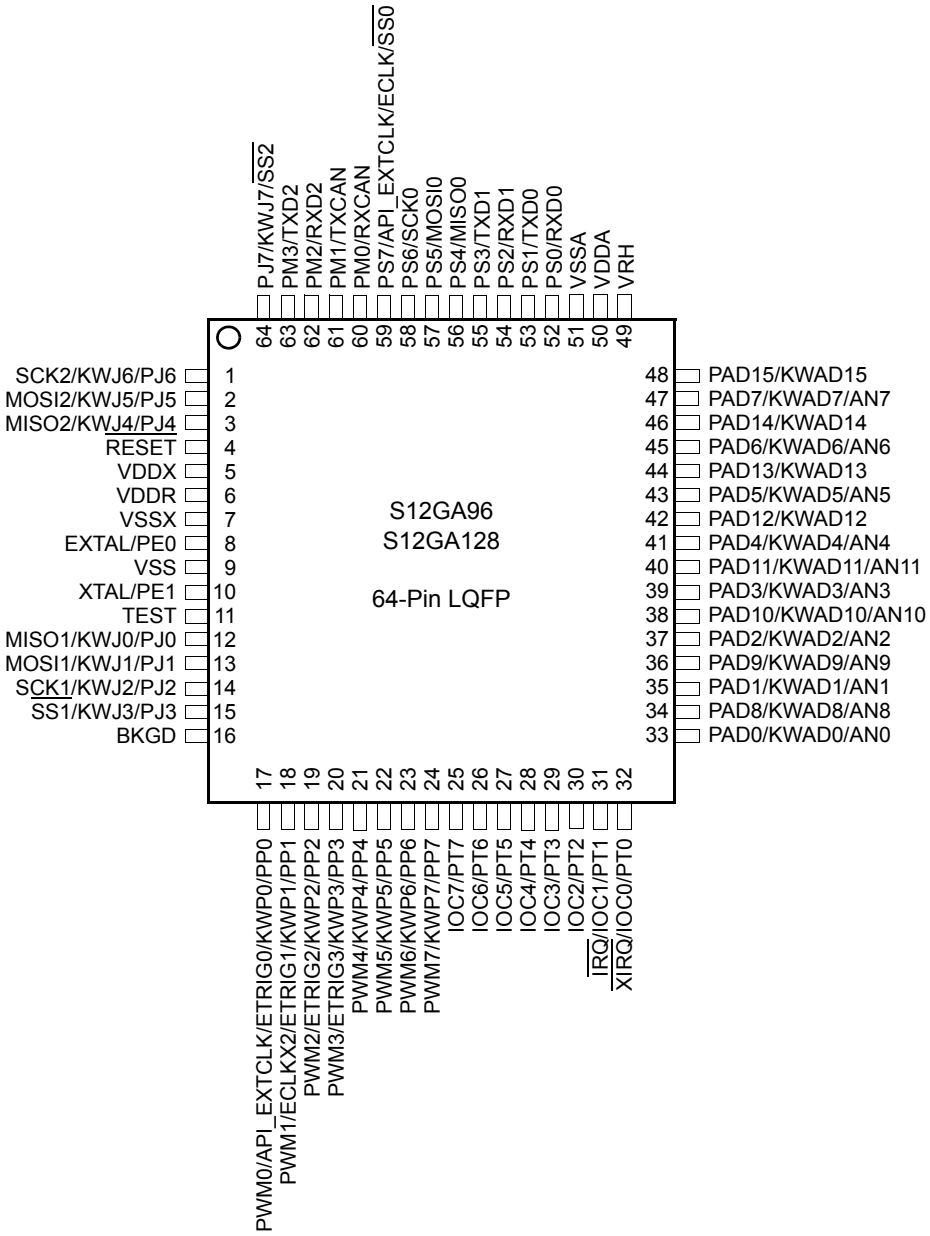

Figure 1-19. 64-Pin LQFP Pinout for S12GA96 and S12GA128

1.8.9.3 Pinout 100-Pin LQFP

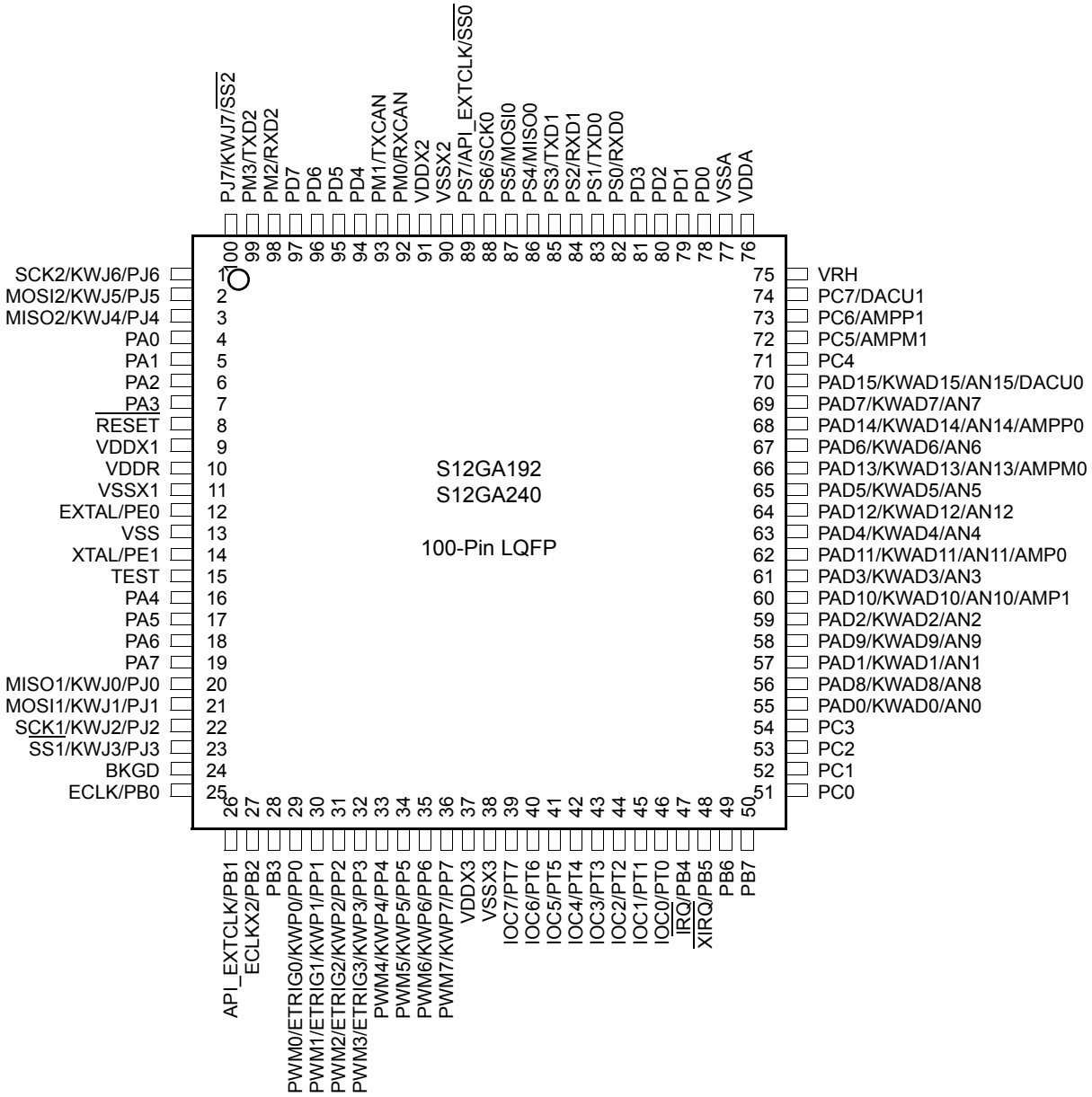

Figure 1-26. 100-Pin LQFP Pinout for S12GA192 and S12GA240

Table 2-21. Block Register Map (G3) (continued)

Global Address Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0258 PTP	R	0	0	PTP5	PTP4	PTP3	PTP2	PTP1	PTP0
	W								
0x0259 PTIP	R	0	0	PTIP5	PTIP4	PTIP3	PTIP2	PTIP1	PTIP0
	W								
0x025A DDRP	R	0	0	DDRP5	DDRP4	DDRP3	DDRP2	DDRP1	DDRP0
	W								
0x025B Reserved	R	0	0	0	0	0	0	0	0
	W								
0x025C PERP	R	0	0	PERP5	PERP4	PERP3	PERP2	PERP1	PERP0
	W								
0x025D PPSP	R	0	0	PPSP5	PPSP4	PPSP3	PPSP2	PPSP1	PPSP0
	W								
0x025E PIEP	R	0	0	PIEP5	PIEP4	PIEP3	PIEP2	PIEP1	PIEP0
	W								
0x025F PIFP	R	0	0	PIFP5	PIFP4	PIFP3	PIFP2	PIFP1	PIFP0
	W								
0x0260–0x0261 Reserved	R	Reserved for ACMP							
	W								
0x0262–0x0267 Reserved	R	0	0	0	0	0	0	0	0
	W								
0x0268 PTJ	R	0	0	0	0	PTJ3	PTJ2	PTJ1	PTJ0
	W								
0x0269 PTIJ	R	0	0	0	0	PTIJ3	PTIJ2	PTIJ1	PTIJ0
	W								
0x026A DDRJ	R	0	0	0	0	DDRJ3	DDRJ2	DDRJ1	DDRJ0
	W								
0x026B Reserved	R	0	0	0	0	0	0	0	0
	W								
0x026C PERJ	R	0	0	0	0	PERJ3	PERJ2	PERJ1	PERJ0
	W								

= Unimplemented or Reserved

The page value for the program page window is stored in the PPAGE register. The value of the PPAGE register can be read or written by normal memory accesses as well as by the CALL and RTC instructions.

Control registers, vector space and parts of the on-chip memories are located in unpaged portions of the 64KB local CPU address space.

The starting address of an interrupt service routine must be located in unpaged memory unless the user is certain that the PPAGE register will be set to the appropriate value when the service routine is called. However an interrupt service routine can call other routines that are in paged memory. The upper 16KB block of the local CPU memory space (0xC000–0xFFFF) is unpaged. It is recommended that all reset and interrupt vectors point to locations in this area or to the other unmapped pages sections of the local CPU memory map.

Expansion of the BDM Local Address Map

PPAGE and BDMPPR register is also used for the expansion of the BDM local address to the global address. These registers can be read and written by the BDM.

The BDM expansion scheme is the same as the CPU expansion scheme.

The four BDMPPR Program Page index bits allow access to the full 256KB address map that can be accessed with 18 address bits.

The BDM program page index register (BDMPPR) is used only when the feature is enabled in BDM and, in the case the CPU is executing a firmware command which uses CPU instructions, or by a BDM hardware commands. See the BDM Block Guide for further details. (see Figure 5-10).

11.2 Signal Description

This section lists all inputs to the ADC10B8C block.

11.2.1 Detailed Signal Descriptions

11.2.1.1 AN*x* (*x* = 7, 6, 5, 4, 3, 2, 1, 0)

This pin serves as the analog input Channel *x*. It can also be configured as digital port or external trigger for the ATD conversion.

11.2.1.2 ETRIG3, ETRIG2, ETRIG1, ETRIG0

These inputs can be configured to serve as an external trigger for the ATD conversion.

Refer to device specification for availability and connectivity of these inputs!

11.2.1.3 VRH, VRL

VRH is the high reference voltage, VRL is the low reference voltage for ATD conversion.

11.2.1.4 VDDA, VSSA

These pins are the power supplies for the analog circuitry of the ADC10B8C block.

11.3 Memory Map and Register Definition

This section provides a detailed description of all registers accessible in the ADC10B8C.

11.3.1 Module Memory Map

Figure 11-2 gives an overview on all ADC10B8C registers.

NOTE

Register Address = Base Address + Address Offset, where the Base Address is defined at the MCU level and the Address Offset is defined at the module level.

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0000	ATDCTL0	R W	Reserved	0	0	0	WRAP3	WRAP2	WRAP1	WRAP0
0x0001	ATDCTL1	R W	ETRIGSEL	SRES1	SRES0	SMP_DIS	ETRIGCH3	ETRIGCH2	ETRIGCH1	ETRIGCH0
0x0002	ATDCTL2	R W	0	AFFC	Reserved	ETRIGLE	ETRIGP	ETRIGE	ASCIE	ACMPIE

= Unimplemented or Reserved

Figure 11-2. ADC10B8C Register Summary (Sheet 1 of 2)

11.3.2.12.2 Right Justified Result Data (DJM=1)

Module Base +
0x0010 = ATDDR0, 0x0012 = ATDDR1, 0x0014 = ATDDR2, 0x0016 = ATDDR3
0x0018 = ATDDR4, 0x001A = ATDDR5, 0x001C = ATDDR6, 0x001E = ATDDR7

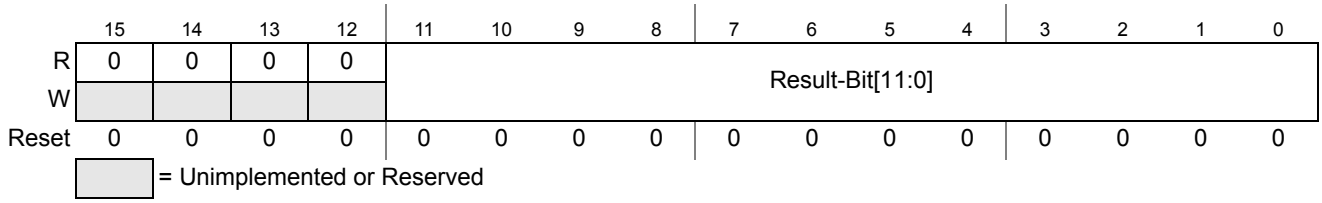

Figure 11-15. Right justified ATD conversion result register (ATDDR*n*)

Table 11-22 shows how depending on the A/D resolution the conversion result is transferred to the ATD result registers for right justified data. Compare is always done using all 12 bits of both the conversion result and the compare value in ATDDRn.

Table 11-22. Conversion result mapping to ATDDRn

A/D resolution	DJM	conversion result mapping to ATDDR*n*
8-bit data	1	Result-Bit[7:0] = result, Result-Bit[11:8]=0000
10-bit data	1	Result-Bit[9:0] = result, Result-Bit[11:10]=00

Table 12-9. Examples of ideal decimal ATD Results

Input Signal VRL = 0 Volts VRH = 5.12 Volts	8-Bit Codes (resolution=20mV)	10-Bit Codes (resolution=5mV)	12-Bit Codes (transfer curve has 1.25mV offset) (resolution=1.25mV)
5.120 Volts	255	1023	4095
...	...	...	...
0.022	1	4	17
0.020	1	4	16
0.018	1	4	14
0.016	1	3	12
0.014	1	3	11
0.012	1	2	9
0.010	1	2	8
0.008	0	2	6
0.006	0	1	4
0.004	0	1	3
0.003	0	1	2
0.002	0	0	1
0.000	0	0	0

Table 12-10. Conversion Sequence Length Coding

S8C	S4C	S2C	S1C	Number of Conversions per Sequence
0	0	0	0	8
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	8
1	0	1	0	8
1	0	1	1	8
1	1	0	0	8
1	1	0	1	8
1	1	1	0	8
1	1	1	1	8

13.3.2.4 ATD Control Register 3 (ATDCTL3)

Writes to this register will abort current conversion sequence.

Module Base + 0x0003

	7	6	5	4	3	2	1	0
R W	DJM	S8C	S4C	S2C	S1C	FIFO	FRZ1	FRZ0
Reset	0	0	1	0	0	0	0	0

= Unimplemented or Reserved

Figure 13-6. ATD Control Register 3 (ATDCTL3)

Read: Anytime

Write: Anytime

Table 13-8. ATDCTL3 Field Descriptions

Field	Description
7 DJM	**Result Register Data Justification** — Result data format is always unsigned. This bit controls justification of conversion data in the result registers. 0 Left justified data in the result registers. 1 Right justified data in the result registers. Table 13-9 gives example ATD results for an input signal range between 0 and 5.12 Volts.
6–3 S8C, S4C, S2C, S1C	**Conversion Sequence Length** — These bits control the number of conversions per sequence. Table 13-10 shows all combinations. At reset, S4C is set to 1 (sequence length is 4). This is to maintain software continuity to HC12 family.
2 FIFO	**Result Register FIFO Mode** — If this bit is zero (non-FIFO mode), the A/D conversion results map into the result registers based on the conversion sequence; the result of the first conversion appears in the first result register (ATDDR0), the second result in the second result register (ATDDR1), and so on. If this bit is one (FIFO mode) the conversion counter is not reset at the beginning or end of a conversion sequence; sequential conversion results are placed in consecutive result registers. In a continuously scanning conversion sequence, the result register counter will wrap around when it reaches the end of the result register file. The conversion counter value (CC3-0 in ATDSTAT0) can be used to determine where in the result register file, the current conversion result will be placed. Aborting a conversion or starting a new conversion clears the conversion counter even if FIFO=1. So the first result of a new conversion sequence, started by writing to ATDCTL5, will always be place in the first result register (ATDDDR0). Intended usage of FIFO mode is continuos conversion (SCAN=1) or triggered conversion (ETRIG=1). Which result registers hold valid data can be tracked using the conversion complete flags. Fast flag clear mode may be useful in a particular application to track valid data. If this bit is one, automatic compare of result registers is always disabled, that is ADC10B12C will behave as if ACMPIE and all CPME[*n*] were zero. 0 Conversion results are placed in the corresponding result register up to the selected sequence length. 1 Conversion results are placed in consecutive result registers (wrap around at end).
1–0 FRZ[1:0]	**Background Debug Freeze Enable** — When debugging an application, it is useful in many cases to have the ATD pause when a breakpoint (Freeze Mode) is encountered. These 2 bits determine how the ATD will respond to a breakpoint as shown in Table 13-11. Leakage onto the storage node and comparator reference capacitors may compromise the accuracy of an immediately frozen conversion depending on the length of the freeze period.

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0024	ATDDR10	R W	See Section 14.3.2.12.1, “Left Justified Result Data (DJM=0)” and Section 14.3.2.12.2, “Right Justified Result Data (DJM=1)”							
0x0026	ATDDR11	R W	See Section 14.3.2.12.1, “Left Justified Result Data (DJM=0)” and Section 14.3.2.12.2, “Right Justified Result Data (DJM=1)”							
0x0028 - 0x002F	Unimple-mented	R	0	0	0	0	0	0	0	0
		W								

= Unimplemented or Reserved

Figure 14-2. ADC12B12C Register Summary (Sheet 3 of 3)

[1]If only AN0 should be converted use MULT=0.

15.3.2.2 ATD Control Register 1 (ATDCTL1)

Writes to this register will abort current conversion sequence.

Module Base + 0x0001

	7	6	5	4	3	2	1	0
R W	ETRIGSEL	SRES1	SRES0	SMP_DIS	ETRIGCH3	ETRIGCH2	ETRIGCH1	ETRIGCH0
Reset	0	0	1	0	1	1	1	1

Figure 15-4. ATD Control Register 1 (ATDCTL1)

Read: Anytime

Write: Anytime

Table 15-3. ATDCTL1 Field Descriptions

Field	Description
7 ETRIGSEL	**External Trigger Source Select** — This bit selects the external trigger source to be either one of the AD channels or one of the ETRIG3-0 inputs. See device specification for availability and connectivity of ETRIG3-0 inputs. If a particular ETRIG3-0 input option is not available, writing a 1 to ETRISEL only sets the bit but has no effect, this means that one of the AD channels (selected by ETRIGCH3-0) is configured as the source for external trigger. The coding is summarized in Table 15-5.
6–5 SRES[1:0]	**A/D Resolution Select** — These bits select the resolution of A/D conversion results. See Table 15-4 for coding.
4 SMP_DIS	**Discharge Before Sampling Bit** 0 No discharge before sampling. 1 The internal sample capacitor is discharged before sampling the channel. This adds 2 ATD clock cycles to the sampling time. This can help to detect an open circuit instead of measuring the previous sampled channel.
3–0 ETRIGCH[3:0]	**External Trigger Channel Select** — These bits select one of the AD channels or one of the ETRIG3-0 inputs as source for the external trigger. The coding is summarized in Table 15-5.

Table 15-4. A/D Resolution Coding

SRES1	SRES0	A/D Resolution
0	0	8-bit data
0	1	10-bit data
1	0	Reserved
1	1	Reserved

23.3.2.11 Timer System Control Register 2 (TSCR2)

Module Base + 0x000D

	7	6	5	4	3	2	1	0
R	TOI	0	0	0	TCRE	PR2	PR1	PR0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 23-19. Timer System Control Register 2 (TSCR2)

Read: Anytime

Write: Anytime.

Table 23-14. TSCR2 Field Descriptions

Field	Description
7 TOI	Timer Overflow Interrupt Enable 0 Interrupt inhibited. 1 Hardware interrupt requested when TOF flag set.
3 TCRE	**Timer Counter Reset Enable** — This bit allows the timer counter to be reset by a successful output compare 7 event. This mode of operation is similar to an up-counting modulus counter. 0 Counter reset inhibited and counter free runs. 1 Counter reset by a successful output compare 7. **Note:** If TC7 = 0x0000 and TCRE = 1, TCNT will stay at 0x0000 continuously. If TC7 = 0xFFFF and TCRE = 1, TOF will never be set when TCNT is reset from 0xFFFF to 0x0000. **Note:** TCRE=1 and TC7!=0, the TCNT cycle period will be TC7 x "prescaler counter width" + "1 Bus Clock", for a more detail explanation please refer to Section 23.4.3, “Output Compare **Note:** This bit and feature is available only when channel 7 exists. If channel 7 doesn’t exist, this bit is reserved. Writing to reserved bit has no effect. Read from reserved bit return a zero.
2:0 PR[2:0]	**Timer Prescaler Select** — These three bits select the frequency of the timer prescaler clock derived from the Bus Clock as shown in Table 23-15.

Table 23-15. Timer Clock Selection

PR2	PR1	PR0	Timer Clock
0	0	0	Bus Clock / 1
0	0	1	Bus Clock / 2
0	1	0	Bus Clock / 4
0	1	1	Bus Clock / 8
1	0	0	Bus Clock / 16
1	0	1	Bus Clock / 32
1	1	0	Bus Clock / 64
1	1	1	Bus Clock / 128

24.4.4.3 Valid Flash Module Commands

Table 24-25 present the valid Flash commands, as enabled by the combination of the functional MCU mode (Normal SingleChip NS, Special Singlechip SS) with the MCU security state (Unsecured, Secured).

Special Singlechip mode is selected by input mmc_ss_mode_ts2 asserted. MCU Secured state is selected by input mmc_secure input asserted.

Table 24-25. Flash Commands by Mode and Security State

FCMD	Command	Unsecured		Secured	
		NS[1]	SS[2]	NS[3]	SS[4]
0x01	Erase Verify All Blocks	*	*	*	*
0x02	Erase Verify Block	*	*	*	*
0x03	Erase Verify P-Flash Section	*	*	*	
0x04	Read Once	*	*	*	
0x06	Program P-Flash	*	*	*	
0x07	Program Once	*	*	*	
0x08	Erase All Blocks		*		*
0x09	Erase Flash Block	*	*	*	
0x0A	Erase P-Flash Sector	*	*	*	
0x0B	Unsecure Flash		*		*
0x0C	Verify Backdoor Access Key	*		*	
0x0D	Set User Margin Level	*	*	*	
0x0E	Set Field Margin Level		*		
0x10	Erase Verify EEPROM Section	*	*	*	
0x11	Program EEPROM	*	*	*	
0x12	Erase EEPROM Sector	*	*	*	

1 Unsecured Normal Single Chip mode
2 Unsecured Special Single Chip mode.
3 Secured Normal Single Chip mode.
4 Secured Special Single Chip mode.

24.4.4.4 P-Flash Commands

Table 24-26 summarizes the valid P-Flash commands along with the effects of the commands on the P-Flash block and other resources within the Flash module.

Table 24-26. P-Flash Commands

FCMD	Command	Function on P-Flash Memory
0x01	Erase Verify All Blocks	Verify that all P-Flash (and EEPROM) blocks are erased.

30.4.4.2.1 Define FCCOB Contents

The FCCOB parameter fields must be loaded with all required parameters for the Flash command being executed. Access to the FCCOB parameter fields is controlled via the CCOBIX bits in the FCCOBIX register (see Section 30.3.2.3).

The contents of the FCCOB parameter fields are transferred to the Memory Controller when the user clears the CCIF command completion flag in the FSTAT register (writing 1 clears the CCIF to 0). The CCIF flag will remain clear until the Flash command has completed. Upon completion, the Memory Controller will return CCIF to 1 and the FCCOB register will be used to communicate any results. The flow for a generic command write sequence is shown in Figure 30-26.

A.8.2 Electrical Characteristics for the PLL

Table A-40. PLL Characteristics

Conditions are shown in Table A-15 unless otherwise noted							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	D	VCO frequency during system reset	f_{VCORST}	8		25	MHz
2	C	VCO locking range	f_{VCO}	32		50	MHz
3	C	Reference Clock	f_{REF}	1			MHz
4	D	Lock Detection	$\|\Delta_{Lock}\|$	0		1.5	%[1]
5	D	Un-Lock Detection	$\|\Delta_{unl}\|$	0.5		2.5	%[1]
6	C	Time to lock	t_{lock}			150 + $256/f_{REF}$	µs
7	C	Jitter fit parameter 1[2] IRC as reference clock source	j_{irc}			1.4	%
8	C	Jitter fit parameter 1[3] XOSCLCP as reference clock source	j_{ext}			1.0	%

1 % deviation from target frequency

2 f_{REF} = 1MHz (IRC), f_{BUS} = 25MHz equivalent f_{PLL} = 50MHz, CPMUSYNR=0x58, CPMUREFDIV=0x00, CPMUPOSTDIV=0x00

3 f_{REF} = 4MHz (XOSCLCP), f_{BUS} = 24MHz equivalent f_{PLL} = 48MHz, CPMUSYNR=0x05, CPMUREFDIV=0x40, CPMUPOSTDIV=0x00

A.9 Electrical Characteristics for the IRC1M

Table A-41. IRC1M Characteristics (Junction Temperature From –40°C To +150°C, all packages)

Conditions are: Temperature option C, V, or M (see Table A-4)							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	P	Internal Reference Frequency, factory trimmed	f_{IRC1M_TRIM}	0.987	1	1.013	MHz

Table A-42. IRC1M Characteristics (Junction Temperature From –40°C To +150°C, KGD)

Conditions are: Temperature option C, V, or M (see Table A-4)							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	P	Internal Reference Frequency, factory trimmed	f_{IRC1M_TRIM}	0.980	1	1.020	MHz

D.7 KGD Information

Bondpad Coordinates

Table D-1. Bondpad Coordinates

Die Pad	Bond Post	Die Pad X Coordinate	Die Pad Y Coordinate	Function
1	1	-1832.06	1347.5	PJ[6]
2	2	-1832.06	1223.5	PJ[5]
3	3	-1832.06	1116.5	PJ[4]
4	4	-1832.06	1009.5	PA[0]
5	5	-1832.06	902.5	PA[1]
6	6	-1832.06	795.5	PA[2]
7	7	-1832.06	688.5	PA[3]
8	8	-1832.06	603.5	RESET
9	9	-1832.06	496.5	VDDX1
10	10	-1832.06	369	VDDR
11	11	-1832.06	241.5	VSSX1
12	12	-1832.06	136.5	PE[0]
13	13	-1832.06	22.5	VSS1
14	14	-1832.06	-91.5	PE[1]
15	15	-1832.06	-201.5	TEST
16	16	-1832.06	-311.5	PA[4]
17	17	-1832.06	-396.5	PA[5]
18	18	-1832.06	-483.5	PA[6]
19	19	-1832.06	-578.5	PA[7]
20	20	-1832.06	-683.5	PJ[0]
21	21	-1832.06	-797.5	PJ[1]
22	22	-1832.06	-921.5	PJ[2]
23	23	-1832.06	-1054.5	PJ[3]
24	24	-1832.06	-1196.5	BKGD
25	25	-1832.06	-1347.5	PB[0]
26	26	-1707.5	-1472.06	PB[1]
27	27	-1506.5	-1472.06	PB[2]

How to Reach Us:

Home Page:

nxp.com

Web Support

nxp.com/support

Document Number: document number???
Rev.1.27
October 28, 2016