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Details	
Product Status	Active
Core Processor	12V1
Core Size	16-Bit
Speed	25MHz
Connectivity	CANbus, IrDA, LINbus, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	86
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3.13V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s9s12g128f0vll

1.8.4.3 Pinout 64-Pin LQFP

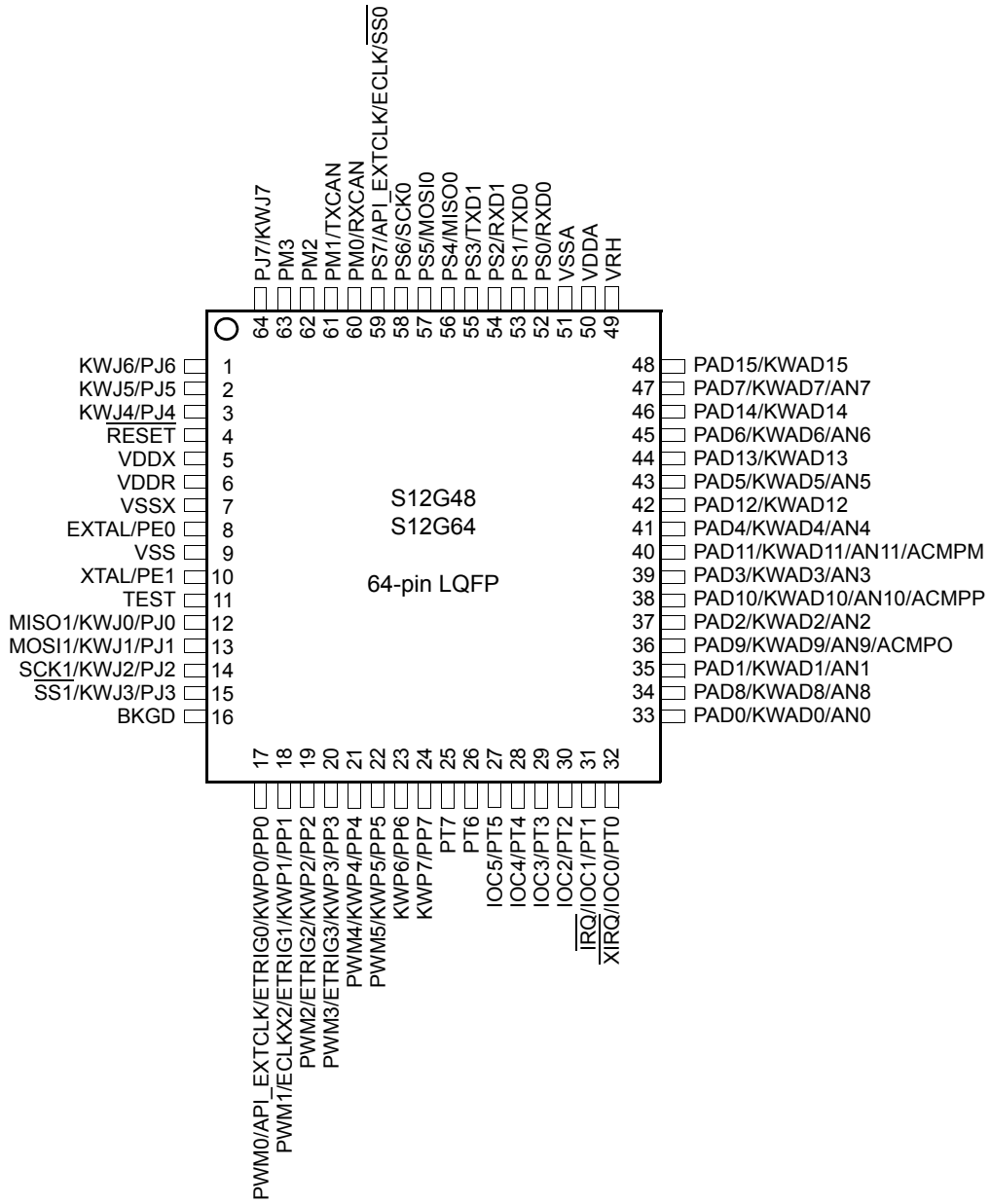


Figure 1-12. 64-Pin LQFP Pinout for S12G48 and S12G64

Table 1-28. 100-Pin LQFP Pinout for S12G192 and S12G240

	Function <----lowest-----PRIORITY-----highest---->				Power Supply	Internal Pull Resistor	
Package Pin	Pin	2nd Func.	3rd Func.	4th Func.		CTRL	Reset State
57	PAD1	KWAD1	AN1	—	V_{DDA}	PER1AD/PPS1AD	Disabled
58	PAD9	KWAD9	AN9	—	V_{DDA}	PER0AD/PPS0AD	Disabled
59	PAD2	KWAD2	AN2	—	V_{DDA}	PER1AD/PPS1AD	Disabled
60	PAD10	KWAD10	AN10	—	V_{DDA}	PER0AD/PPS0AD	Disabled
61	PAD3	KWAD3	AN3	—	V_{DDA}	PER1AD/PPS1AD	Disabled
62	PAD11	KWAD11	AN11	—	V_{DDA}	PER0AD/PPS0AD	Disabled
63	PAD4	KWAD4	AN4	—	V_{DDA}	PER1AD/PPS1AD	Disabled
64	PAD12	KWAD12	AN12	—	V_{DDA}	PER0AD/PPS0AD	Disabled
65	PAD5	KWAD5	AN5	—	V_{DDA}	PER1AD/PPS1AD	Disabled
66	PAD13	KWAD13	AN13	—	V_{DDA}	PER0AD/PPS0AD	Disabled
67	PAD6	KWAD6	AN6	—	V_{DDA}	PER1AD/PPS1AD	Disabled
68	PAD14	KWAD14	AN14	—	V_{DDA}	PER0AD/PPS0AD	Disabled
69	PAD7	KWAD7	AN7	—	V_{DDA}	PER1AD/PPS1AD	Disabled
70	PAD15	KWAD15	AN15	—	V_{DDA}	PER0AD/PPS0AD	Disabled
71	PC4	—	—	—	V_{DDA}	PUCR/PUPCE	Disabled
72	PC5	—	—	—	V_{DDA}	PUCR/PUPCE	Disabled
73	PC6	—	—	—	V_{DDA}	PUCR/PUPCE	Disabled
74	PC7	—	—	—	V_{DDA}	PUCR/PUPCE	Disabled
75	VRH	—	—	—	—	—	—
76	VDDA	—	—	—	—	—	—
77	VSSA	—	—	—	—	—	—
78	PD0	—	—	—	V_{DDX}	PUCR/PUPDE	Disabled
79	PD1	—	—	—	V_{DDX}	PUCR/PUPDE	Disabled
80	PD2	—	—	—	V_{DDX}	PUCR/PUPDE	Disabled
81	PD3	—	—	—	V_{DDX}	PUCR/PUPDE	Disabled
82	PS0	RXD0	—	—	V_{DDX}	PERS/PPSS	Up
83	PS1	TXD0	—	—	V_{DDX}	PERS/PPSS	Up
84	PS2	RXD1	—	—	V_{DDX}	PERS/PPSS	Up
85	PS3	TXD1	—	—	V_{DDX}	PERS/PPSS	Up

2.3.11 Pins PJ7-0

Table 2-15. Port J Pins PJ7-0

PJ7	• 64/100 LQFP: The SPI2 $\overline{SS}$ signal is mapped to this pin when used with the SPI function. Depending on the configuration of the enabled SPI2 the I/O state is forced to be input or output. • 64/100 LQFP: Pin interrupts can be generated if enabled in input or output mode. • Signal priority: 64/100 LQFP: $\overline{SS2}$ > GPO
PJ6	• 64/100 LQFP: The SPI2 SCK signal is mapped to this pin when used with the SPI function. Depending on the configuration of the enabled SPI2 the I/O state is forced to be input or output. • 64/100 LQFP: Pin interrupts can be generated if enabled in input or output mode. • Signal priority: 64/100 LQFP: SCK2 > GPO
PJ5	• 64/100 LQFP: The SPI2 MOSI signal is mapped to this pin when used with the SPI function. Depending on the configuration of the enabled SPI2 the I/O state is forced to be input or output. • 64/100 LQFP: Pin interrupts can be generated if enabled in input or output mode. • Signal priority: 64/100 LQFP: MOSI2 > GPO
PJ4	• 64/100 LQFP: The SPI2 MISO signal is mapped to this pin when used with the SPI function.Depending on the configuration of the enabled SPI2 the I/O state is forced to be input or output. • 64/100 LQFP: Pin interrupts can be generated if enabled in input or output mode. • Signal priority: 64/100 LQFP: MISO2 > GPO
PJ3	• Except 20 TSSOP and 32 LQFP: The SPI1 $\overline{SS}$ signal is mapped to this pin when used with the SPI function. Depending on the configuration of the enabled SPI1 the I/O state is forced to be input or output. • 48 LQFP: The PWM channel 7 signal is mapped to this pin when used with the PWM function. The enabled PWM channel forces the I/O state to be an output. • Except 20 TSSOP and 32 LQFP: Pin interrupts can be generated if enabled in input or output mode. • Signal priority: 48 LQFP: $\overline{SS1}$ > PWM7 > GPO 64/100 LQFP: $\overline{SS1}$ > GPO
PJ2	• Except 20 TSSOP and 32 LQFP: The SPI1 SCK signal is mapped to this pin when used with the SPI function. Depending on the configuration of the enabled SPI1 the I/O state is forced to be input or output. • 48 LQFP: The TIM channel 7 signal is mapped to this pin when used with the TIM function. The TIM forces the I/O state to be an output for a timer port associated with an enabled output. • Except 20 TSSOP and 32 LQFP: Pin interrupts can be generated if enabled in input or output mode. • Signal priority: 48 LQFP: SCK1 > IOC7 > GPO 64/100 LQFP: SCK1 > GPO

The reset value of 0xE ensures that there is linear Flash space available between addresses 0x0000 and 0xFFFF out of reset.

The fixed 16KB page from 0xC000-0xFFFF is the page number 0xF.

5.4 Functional Description

The S12GMMC block performs several basic functions of the S12G sub-system operation: MCU operation modes, priority control, address mapping, select signal generation and access limitations for the system. Each aspect is described in the following subsections.

5.4.1 MCU Operating Modes

- Normal single chip mode

  This is the operation mode for running application code. There is no external bus in this mode.
- Special single chip mode

  This mode is generally used for debugging operation, boot-strapping or security related operations. The active background debug mode is in control of the CPU code execution and the BDM firmware is waiting for serial commands sent through the BKGD pin.

5.4.2 Memory Map Scheme

5.4.2.1 CPU and BDM Memory Map Scheme

The BDM firmware lookup tables and BDM register memory locations share addresses with other modules; however they are not visible in the memory map during user's code execution. The BDM memory resources are enabled only during the READ_BD and WRITE_BD access cycles to distinguish between accesses to the BDM memory area and accesses to the other modules. (Refer to BDM Block Guide for further details).

When the MCU enters active BDM mode, the BDM firmware lookup tables and the BDM registers become visible in the local memory map in the range 0xFF00-0xFFFF (global address 0x3_FF00 - 0x3_FFFF) and the CPU begins execution of firmware commands or the BDM begins execution of hardware commands. The resources which share memory space with the BDM module will not be visible in the memory map during active BDM mode.

Please note that after the MCU enters active BDM mode the BDM firmware lookup tables and the BDM registers will also be visible between addresses 0xBF00 and 0xBFFF if the PPAGE register contains value of 0x0F.

5.4.2.1.1 Expansion of the Local Address Map

Expansion of the CPU Local Address Map

The program page index register in S12GMMC allows accessing up to 256KB of address space in the global memory map by using the four index bits (PPAGE[3:0]) to page 16x16 KB blocks into the program page window located from address 0x8000 to address 0xBFFF in the local CPU memory map.

Table 12-9. Examples of ideal decimal ATD Results

Input Signal VRL = 0 Volts VRH = 5.12 Volts	8-Bit Codes (resolution=20mV)	10-Bit Codes (resolution=5mV)	12-Bit Codes (transfer curve has 1.25mV offset) (resolution=1.25mV)
5.120 Volts	255	1023	4095
...	...	...	...
0.022	1	4	17
0.020	1	4	16
0.018	1	4	14
0.016	1	3	12
0.014	1	3	11
0.012	1	2	9
0.010	1	2	8
0.008	0	2	6
0.006	0	1	4
0.004	0	1	3
0.003	0	1	2
0.002	0	0	1
0.000	0	0	0

Table 12-10. Conversion Sequence Length Coding

S8C	S4C	S2C	S1C	Number of Conversions per Sequence
0	0	0	0	8
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	8
1	0	1	0	8
1	0	1	1	8
1	1	0	0	8
1	1	0	1	8
1	1	1	0	8
1	1	1	1	8

13.2 Signal Description

This section lists all inputs to the ADC10B12C block.

13.2.1 Detailed Signal Descriptions

13.2.1.1 AN*x* (*x* = 11, 10, 9, 8, 7, 6, 5, 4, 3, 2, 1, 0)

This pin serves as the analog input Channel *x*. It can also be configured as digital port or external trigger for the ATD conversion.

13.2.1.2 ETRIG3, ETRIG2, ETRIG1, ETRIG0

These inputs can be configured to serve as an external trigger for the ATD conversion.

Refer to device specification for availability and connectivity of these inputs!

13.2.1.3 VRH, VRL

VRH is the high reference voltage, VRL is the low reference voltage for ATD conversion.

13.2.1.4 VDDA, VSSA

These pins are the power supplies for the analog circuitry of the ADC10B12C block.

13.3 Memory Map and Register Definition

This section provides a detailed description of all registers accessible in the ADC10B12C.

13.3.1 Module Memory Map

Figure 13-2 gives an overview on all ADC10B12C registers.

NOTE

Register Address = Base Address + Address Offset, where the Base Address is defined at the MCU level and the Address Offset is defined at the module level.

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0000	ATDCTL0	R W	Reserved	0	0	0	WRAP3	WRAP2	WRAP1	WRAP0
0x0001	ATDCTL1	R W	ETRIGSEL	SRES1	SRES0	SMP_DIS	ETRIGCH3	ETRIGCH2	ETRIGCH1	ETRIGCH0
0x0002	ATDCTL2	R W	0	AFFC	Reserved	ETRIGLE	ETRIGP	ETRIGE	ASCIE	ACMPIE

= Unimplemented or Reserved

Figure 13-2. ADC10B12C Register Summary (Sheet 1 of 3)

14.1.3 Block Diagram

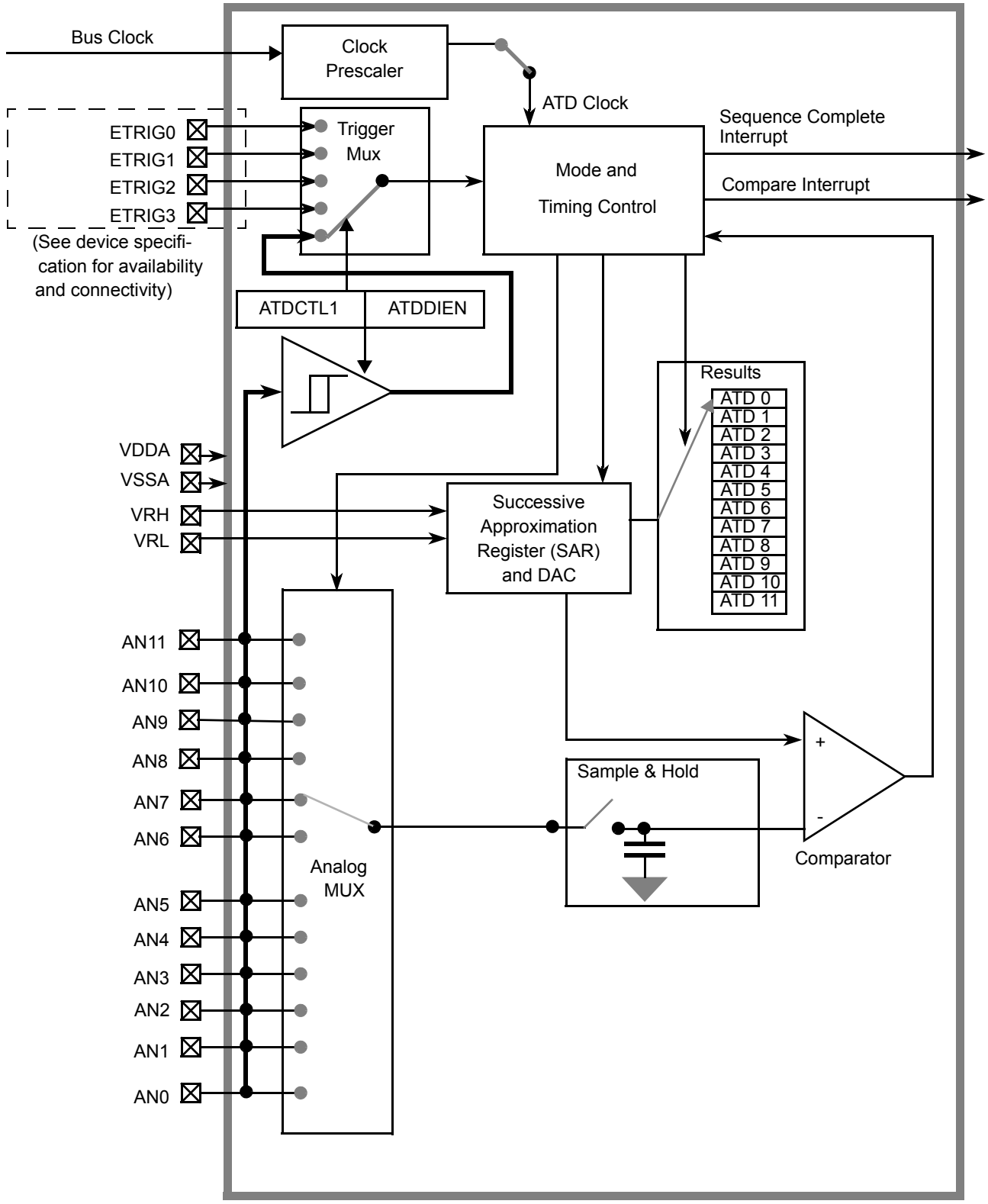


Figure 14-1. ADC12B12C Block Diagram

Module Base + 0x0006 Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	TXE2	TXE1	TXE0
W								
Reset:	0	0	0	0	0	1	1	1

= Unimplemented

Figure 18-10. MSCAN Transmitter Flag Register (CANTFLG)

[1] Read: Anytime
Write: Anytime when not in initialization mode; write of 1 clears flag, write of 0 is ignored

NOTE

The CANTFLG register is held in the reset state when the initialization mode is active (INITRQ = 1 and INITAK = 1). This register is writable when not in initialization mode (INITRQ = 0 and INITAK = 0).

Table 18-13. CANTFLG Register Field Descriptions

Field	Description
2-0 TXE[2:0]	**Transmitter Buffer Empty** — This flag indicates that the associated transmit message buffer is empty, and thus not scheduled for transmission. The CPU must clear the flag after a message is set up in the transmit buffer and is due for transmission. The MSCAN sets the flag after the message is sent successfully. The flag is also set by the MSCAN when the transmission request is successfully aborted due to a pending abort request (see Section 18.3.2.9, “MSCAN Transmitter Message Abort Request Register (CANTARQ)”). If not masked, a transmit interrupt is pending while this flag is set. Clearing a TXEx flag also clears the corresponding ABTAKx (see Section 18.3.2.10, “MSCAN Transmitter Message Abort Acknowledge Register (CANTAAK)”). When a TXEx flag is set, the corresponding ABTRQx bit is cleared (see Section 18.3.2.9, “MSCAN Transmitter Message Abort Request Register (CANTARQ)”). When listen-mode is active (see Section 18.3.2.2, “MSCAN Control Register 1 (CANCTL1)”) the TXEx flags cannot be cleared and no transmission is started. Read and write accesses to the transmit buffer will be blocked, if the corresponding TXEx bit is cleared (TXEx = 0) and the buffer is scheduled for transmission. 0 The associated message buffer is full (loaded with a message due for transmission) 1 The associated message buffer is empty (not scheduled)

18.3.2.8 MSCAN Transmitter Interrupt Enable Register (CANTIER)

This register contains the interrupt enable bits for the transmit buffer empty interrupt flags.

18.4.2 Message Storage

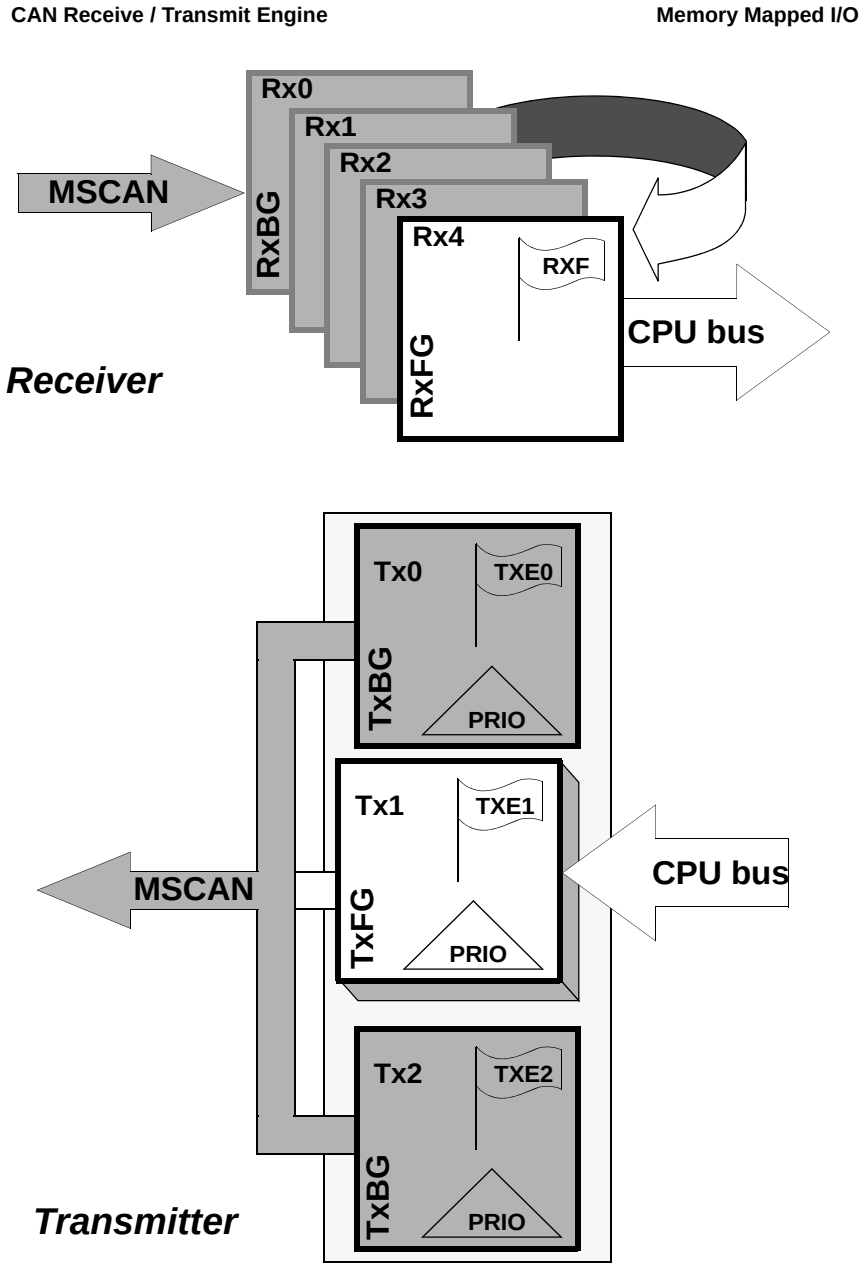


Figure 18-39. User Model for Message Buffer Organization

The MSCAN facilitates a sophisticated message storage system which addresses the requirements of a broad range of network applications.

18.4.2.1 Message Transmit Background

Modern application layer software is built upon two fundamental assumptions:

Table 22-5. TTOV Field Descriptions

Note: Writing to unavailable bits has no effect. Reading from unavailable bits return a zero.

Field	Description
5:0 TOV[5:0]	**Toggle On Overflow Bits** — TOVx toggles output compare pin on overflow. This feature only takes effect when in output compare mode. When set, it takes precedence over forced output compare 0 Toggle output compare pin on overflow feature disabled. 1 Toggle output compare pin on overflow feature enabled.

22.3.2.6 Timer Control Register 1/Timer Control Register 2 (TCTL1/TCTL2)

Module Base + 0x0008

	7	6	5	4	3	2	1	0
R W	RESERVED	RESERVED	RESERVED	RESERVED	OM5	OL5	OM4	OL4
Reset	0	0	0	0	0	0	0	0

Figure 22-10. Timer Control Register 1 (TCTL1)

Module Base + 0x0009

	7	6	5	4	3	2	1	0
R W	OM3	OL3	OM2	OL2	OM1	OL1	OM0	OL0
Reset	0	0	0	0	0	0	0	0

Figure 22-11. Timer Control Register 2 (TCTL2)

Read: Anytime

Write: Anytime

Table 22-6. TCTL1/TCTL2 Field Descriptions

Note: Writing to unavailable bits has no effect. Reading from unavailable bits return a zero

Field	Description
5:0 OMx	**Output Mode** — These six pairs of control bits are encoded to specify the output action to be taken as a result of a successful OCx compare. When either OMx or OLx is 1, the pin associated with OCx becomes an output tied to OCx. **Note:** For an output line to be driven by an OCx the OCPDx must be cleared.
5:0 OLx	**Output Level** — These sixpairs of control bits are encoded to specify the output action to be taken as a result of a successful OCx compare. When either OMx or OLx is 1, the pin associated with OCx becomes an output tied to OCx. **Note:** For an output line to be driven by an OCx the OCPDx must be cleared.

By enabling the PRNT bit of the TSCR1 register, the performance of the timer can be enhanced. In this case, it is possible to set additional prescaler settings for the main timer counter in the present timer by using PTPSR[7:0] bits of PTPSR register generating divide by 1, 2, 3, 4,....20, 21, 22, 23,.....255, or 256.

22.4.2 Input Capture

Clearing the I/O (input/output) select bit, IOSx, configures channel x as an input capture channel. The input capture function captures the time at which an external event occurs. When an active edge occurs on the pin of an input capture channel, the timer transfers the value in the timer counter into the timer channel registers, TCx.

The minimum pulse width for the input capture input is greater than two Bus clocks.

An input capture on channel x sets the CxF flag. The CxI bit enables the CxF flag to generate interrupt requests. Timer module must stay enabled (TEN bit of TSCR1 register must be set to one) while clearing CxF (writing one to CxF).

22.4.3 Output Compare

Setting the I/O select bit, IOSx, configures channel x when available as an output compare channel. The output compare function can generate a periodic pulse with a programmable polarity, duration, and frequency. When the timer counter reaches the value in the channel registers of an output compare channel, the timer can set, clear, or toggle the channel pin if the corresponding OCPDx bit is set to zero. An output compare on channel x sets the CxF flag. The CxI bit enables the CxF flag to generate interrupt requests. Timer module must stay enabled (TEN bit of TSCR1 register must be set to one) while clearing CxF (writing one to CxF).

The output mode and level bits, OMx and OLx, select set, clear, toggle on output compare. Clearing both OMx and OLx results in no output compare action on the output compare channel pin.

Setting a force output compare bit, FOCx, causes an output compare on channel x. A forced output compare does not set the channel flag.

Writing to the timer port bit of an output compare pin does not affect the pin state. The value written is stored in an internal latch. When the pin becomes available for general-purpose output, the last value written to the bit appears at the pin.

22.4.3.1 OC Channel Initialization

The internal register whose output drives OCx can be programmed before the timer drives OCx. The desired state can be programmed to this internal register by writing a one to CFORCx bit with TIOSx, OCPDx and TEN bits set to one.

Set OCx: Write a 1 to FOCx while TEN=1, IOSx=1, OMx=1, OLx=1 and OCPDx=1

Clear OCx: Write a 1 to FOCx while TEN=1, IOSx=1, OMx=1, OLx=0 and OCPDx=1

Setting OCPDx to zero allows the internal register to drive the programmed state to OCx. This allows a glitch free switch over of port from general purpose I/O to timer output once the OCPDx bit is set to zero.

22.5 Resets

The reset state of each individual bit is listed within Section 22.3, “Memory Map and Register Definition” which details the registers and their bit fields

22.6 Interrupts

This section describes interrupts originated by the TIM16B6CV3 block. Table 22-18 lists the interrupts generated by the TIM16B6CV3 to communicate with the MCU.

Table 22-18. TIM16B6CV3 Interrupts

Interrupt	Offset	Vector	Priority	Source	Description
C[5:0]F	—	—	—	Timer Channel 5–0	Active high timer channel interrupts 5–0
TOF	—	—	—	Timer Overflow	Timer Overflow interrupt

The TIM16B6CV3 could use up to 7 interrupt vectors. The interrupt vector offsets and interrupt numbers are chip dependent.

22.6.1 Channel [5:0] Interrupt (C[5:0]F)

This active high outputs will be asserted by the module to request a timer channel 7 – 0 interrupt. The TIM block only generates the interrupt and does not service it. Only bits related to implemented channels are valid.

22.6.2 Timer Overflow Interrupt (TOF)

This active high output will be asserted by the module to request a timer overflow interrupt. The TIM block only generates the interrupt and does not service it.

Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0021 PAFLG	R	0	0	0	0	0	0	PAOVF	PAIF
	W								
0x0022 PACNTH	R	PACNT15	PACNT14	PACNT13	PACNT12	PACNT11	PACNT10	PACNT9	PACNT8
	W								
0x0023 PACNTL	R	PACNT7	PACNT6	PACNT5	PACNT4	PACNT3	PACNT2	PACNT1	PACNT0
	W								
0x0024–0x002B Reserved	R								
	W								
0x002C OCPD	R	OCPD7	OCPD6	OCPD5	OCPD4	OCPD3	OCPD2	OCPD1	OCPD0
	W								
0x002D Reserved	R								
0x002E PTPSR	R	PTPS7	PTPS6	PTPS5	PTPS4	PTPS3	PTPS2	PTPS1	PTPS0
	W								
0x002F Reserved	R								
	W								

Figure 23-5. TIM16B8CV3 Register Summary (Sheet 2 of 2)

[1] The register is available only if corresponding channel exists.

23.3.2.1 Timer Input Capture/Output Compare Select (TIOS)

Module Base + 0x0000

	7	6	5	4	3	2	1	0
R W	IOS7	IOS6	IOS5	IOS4	IOS3	IOS2	IOS1	IOS0
Reset	0	0	0	0	0	0	0	0

Figure 23-6. Timer Input Capture/Output Compare Select (TIOS)

Read: Anytime

Write: Anytime

Table 23-2. TIOS Field Descriptions

Note: Writing to unavailable bits has no effect. Reading from unavailable bits return a zero.

Field	Description
7:0 IOS[7:0]	Input Capture or Output Compare Channel Configuration 0 The corresponding implemented channel acts as an input capture. 1 The corresponding implemented channel acts as an output compare.

Address & Name		7	6	5	4	3	2	1	0
0x0003 FRSV0	R	0	0	0	0	0	0	0	0
	W								
0x0004 FCNFG	R	CCIE	0	0	IGNSF	0	0	FDFD	FSFD
	W								
0x0005 FERCNFG	R	0	0	0	0	0	0	DFDIE	SFDIE
	W								
0x0006 FSTAT	R	CCIF	0	ACCERR	FPVIOL	MGBUSY	RSVD	MGSTAT1	MGSTAT0
	W								
0x0007 FERSTAT	R	0	0	0	0	0	0	DFDIF	SFDIF
	W								
0x0008 FPROT	R	FPOPEN	RNV6	FPHDIS	FPHS1	FPHS0	RNV2	RNV1	RNV0
	W								
0x0009 EEPROT	R	DPOPEN	0	0	DPS4	DPS3	DPS2	DPS1	DPS0
	W								
0x000A FCCOBHI	R	CCOB15	CCOB14	CCOB13	CCOB12	CCOB11	CCOB10	CCOB9	CCOB8
	W								
0x000B FCCOBLO	R	CCOB7	CCOB6	CCOB5	CCOB4	CCOB3	CCOB2	CCOB1	CCOB0
	W								
0x000C FRSV1	R	0	0	0	0	0	0	0	0
	W								
0x000D FRSV2	R	0	0	0	0	0	0	0	0
	W								
0x000E FRSV3	R	0	0	0	0	0	0	0	0
	W								
0x000F FRSV4	R	0	0	0	0	0	0	0	0
	W								
0x0010 FOPT	R	NV7	NV6	NV5	NV4	NV3	NV2	NV1	NV0
	W								

Figure 24-4. FTMRG16K1 Register Summary (continued)

24.4 Functional Description

24.4.1 Modes of Operation

The FTMRG16K1 module provides the modes of operation normal and special . The operating mode is determined by module-level inputs and affects the FCLKDIV, FCNFG, and EEPROT registers (see Table 24-25).

24.4.2 IFR Version ID Word

The version ID word is stored in the IFR at address 0x0_40B6. The contents of the word are defined in Table 24-24.

Table 24-24. IFR Version ID Fields

[15:4]	[3:0]
Reserved	VERNUM

- VERNUM: Version number. The first version is number 0b_0001 with both 0b_0000 and 0b_1111 meaning ‘none’.

24.4.3 Internal NVM resource (NVMRES)

IFR is an internal NVM resource readable by CPU , when NVMRES is active. The IFR fields are shown in Table 24-5.

The NVMRES global address map is shown in Table 24-6.

24.4.4 Flash Command Operations

Flash command operations are used to modify Flash memory contents.

The next sections describe:

- How to write the FCLKDIV register that is used to generate a time base (FCLK) derived from BUSCLK for Flash program and erase command operations
- The command write sequence used to set Flash command parameters and launch execution
- Valid Flash commands available for execution, according to MCU functional mode and MCU security state.

24.4.4.1 Writing the FCLKDIV Register

Prior to issuing any Flash program or erase command after a reset, the user is required to write the FCLKDIV register to divide BUSCLK down to a target FCLK of 1 MHz. Table 24-8 shows recommended values for the FDIV field based on BUSCLK frequency.

Figure 26-2. P-Flash Memory Map

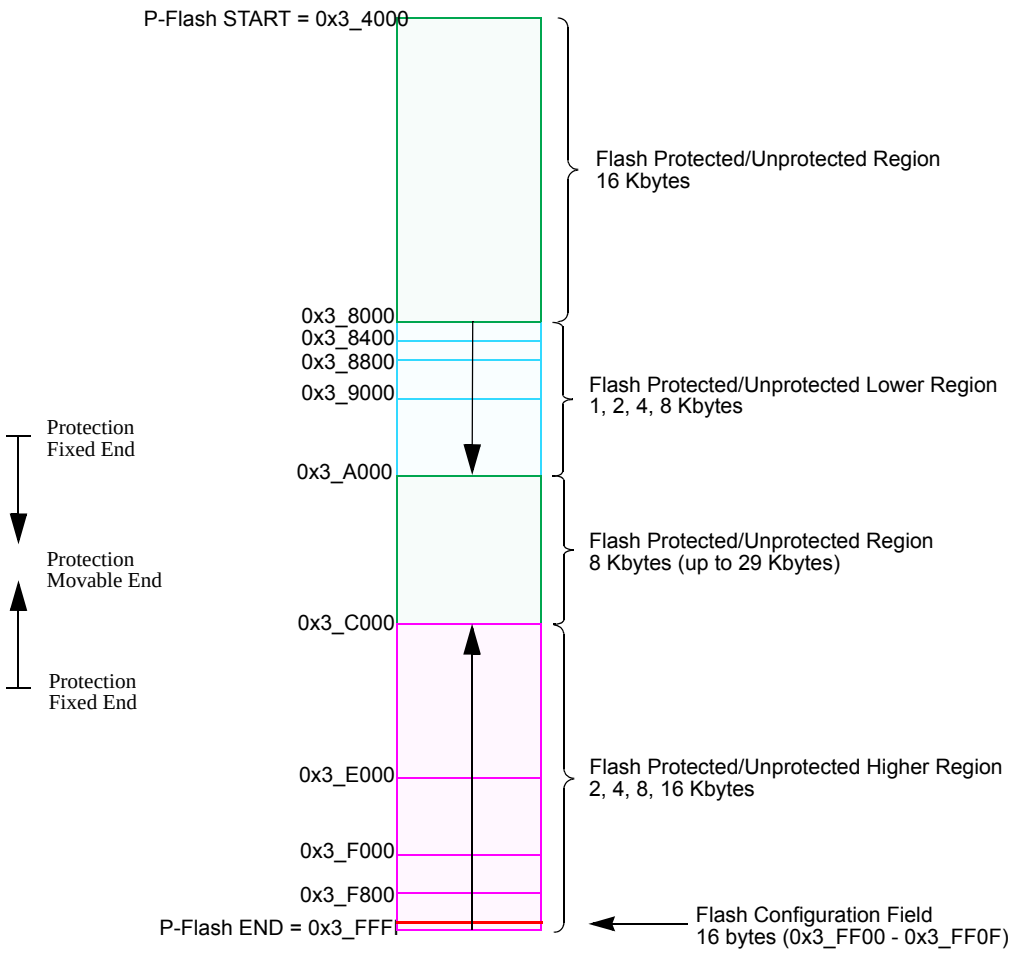


Table 26-5. Program IFR Fields

Global Address	Size (Bytes)	Field Description
0x0_4000 – 0x0_4007	8	Reserved
0x0_4008 – 0x0_40B5	174	Reserved
0x0_40B6 – 0x0_40B7	2	Version ID[1]
0x0_40B8 – 0x0_40BF	8	Reserved
0x0_40C0 – 0x0_40FF	64	Program Once Field Refer to Section 26.4.6.6, “Program Once Command”

[1] Used to track firmware patch versions, see Section 26.4.2

Table 27-29. EEPROM Commands

FCMD	Command	Function on EEPROM Memory
0x08	Erase All Blocks	Erase all EEPROM (and P-Flash) blocks. An erase of all Flash blocks is only possible when the FPLDIS, FPHDIS, and FPOPEN bits in the FPROT register and the DPOPEN bit in the EEPROT register are set prior to launching the command.
0x09	Erase Flash Block	Erase a EEPROM (or P-Flash) block. An erase of the full EEPROM block is only possible when DPOPEN bit in the EEPROT register is set prior to launching the command.
0x0B	Unsecure Flash	Supports a method of releasing MCU security by erasing all EEPROM (and P-Flash) blocks and verifying that all EEPROM (and P-Flash) blocks are erased.
0x0D	Set User Margin Level	Specifies a user margin read level for the EEPROM block.
0x0E	Set Field Margin Level	Specifies a field margin read level for the EEPROM block (special modes only).
0x10	Erase Verify EEPROM Section	Verify that a given number of words starting at the address provided are erased.
0x11	Program EEPROM	Program up to four words in the EEPROM block.
0x12	Erase EEPROM Sector	Erase all bytes in a sector of the EEPROM block.

27.4.5 Allowed Simultaneous P-Flash and EEPROM Operations

Only the operations marked ‘OK’ in Table 27-30 are permitted to be run simultaneously on the Program Flash and EEPROM blocks. Some operations cannot be executed simultaneously because certain hardware resources are shared by the two memories. The priority has been placed on permitting Program Flash reads while program and erase operations execute on the EEPROM, providing read (P-Flash) while write (EEPROM) functionality.

Table 27-30. Allowed P-Flash and EEPROM Simultaneous Operations

	EEPROM				
Program Flash	**Read**	**Margin Read[1]**	**Program**	**Sector Erase**	**Mass Erase[2]**
Read		OK	OK	OK	
Margin Read[1]					
Program					
Sector Erase					
Mass Erase[2]					OK

1 A ‘Margin Read’ is any read after executing the margin setting commands ‘Set User Margin Level’ or ‘Set Field Margin Level’ with anything but the ‘normal’ level specified. See the Note on margin settings in Section 27.4.6.12 and Section 27.4.6.13.

2 The ‘Mass Erase’ operations are commands ‘Erase All Blocks’ and ‘Erase Flash Block’

Table 29-43. Program Once Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 101 at command launch
		Set if command not available in current mode (see Table 29-27)
		Set if an invalid phrase index is supplied
		Set if the requested phrase has already been programmed[1]
	FPVIOL	None
	MGSTAT1	Set if any errors have been encountered during the verify operation
	MGSTAT0	Set if any non-correctable errors have been encountered during the verify operation

1 If a Program Once phrase is initially programmed to 0xFFFF_FFFF_FFFF_FFFF, the Program Once command will be allowed to execute again on that same phrase.

29.4.6.7 Erase All Blocks Command

The Erase All Blocks operation will erase the entire P-Flash and EEPROM memory space.

Table 29-44. Erase All Blocks Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x08	Not required

Upon clearing CCIF to launch the Erase All Blocks command, the Memory Controller will erase the entire Flash memory space and verify that it is erased. If the Memory Controller verifies that the entire Flash memory space was properly erased, security will be released. During the execution of this command (CCIF=0) the user must not write to any Flash module register. The CCIF flag will set after the Erase All Blocks operation has completed.

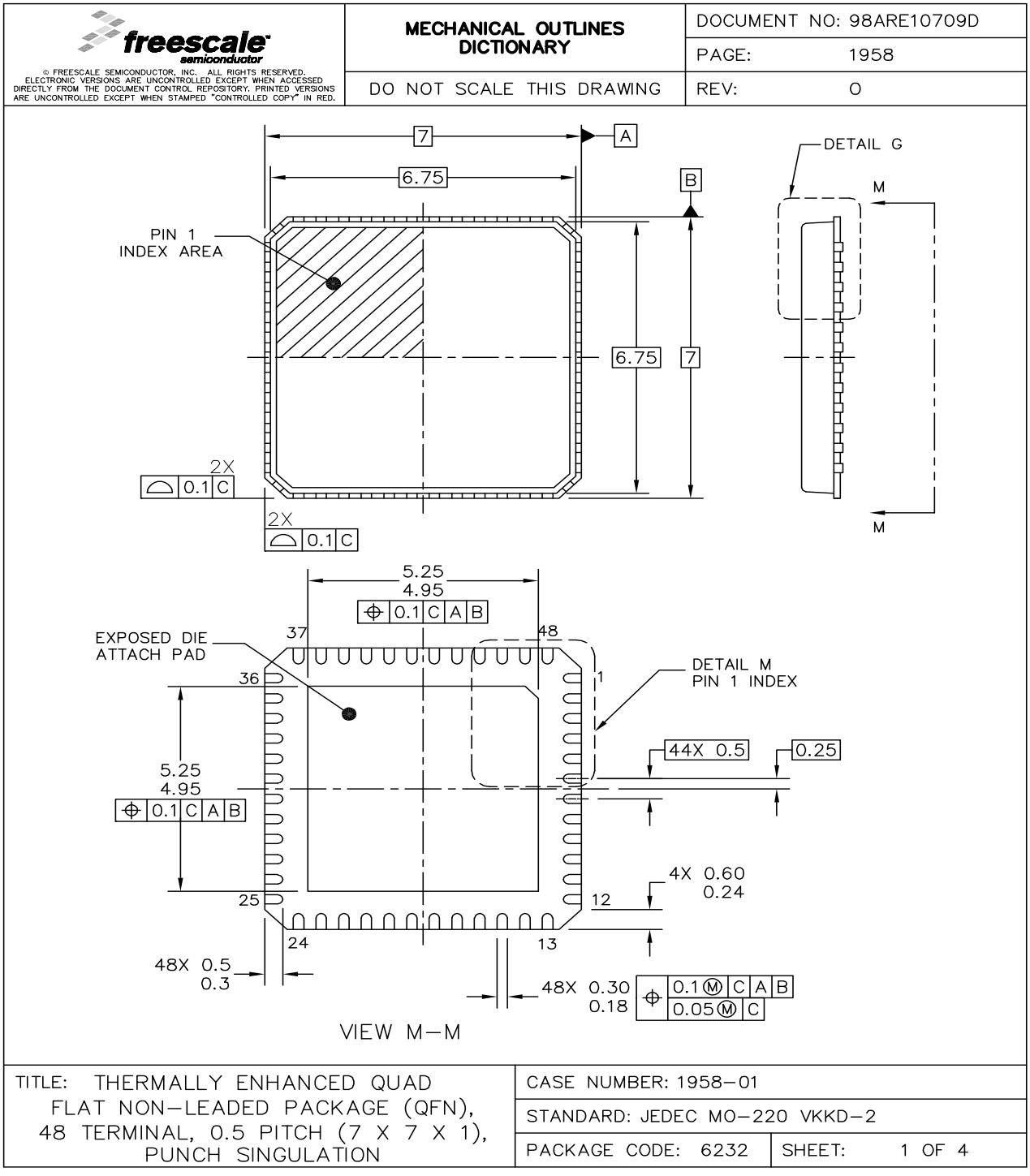
Table 29-45. Erase All Blocks Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 000 at command launch
		Set if command not available in current mode (see Table 29-27)
	FPVIOL	Set if any area of the P-Flash or EEPROM memory is protected
	MGSTAT1	Set if any errors have been encountered during the verify operation
	MGSTAT0	Set if any non-correctable errors have been encountered during the verify operation

29.4.6.8 Erase Flash Block Command

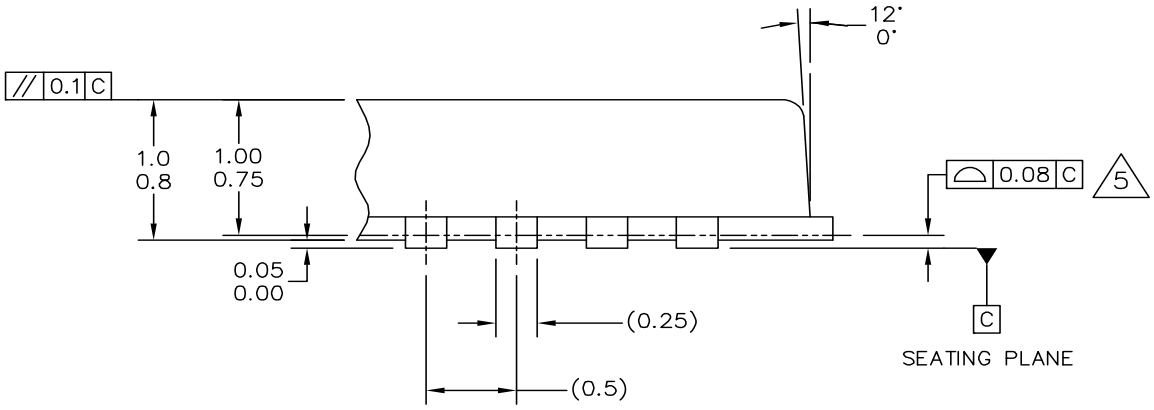
The Erase Flash Block operation will erase all addresses in a P-Flash or EEPROM block.

D.4 48 QFN Mechanical Dimensions

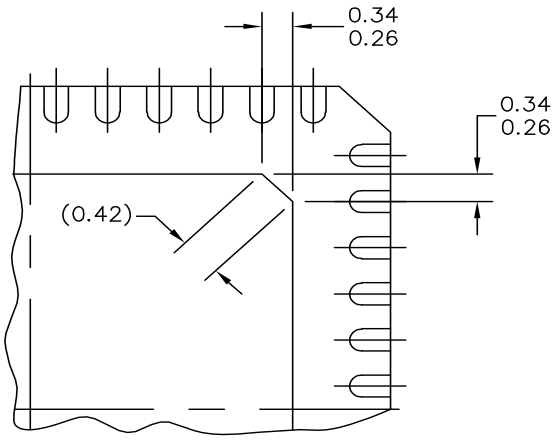


freescale semiconductor

MECHANICAL OUTLINES DICTIONARY	DOCUMENT NO: 98ARE10709D
	PAGE: 1958
DO NOT SCALE THIS DRAWING	REV: O



DETAIL G
VIEW ROTATED 90° CW



DETAIL M
BACKSIDE PIN 1 INDEX

TITLE: THERMALLY ENHANCED QUAD FLAT NON–LEADED PACKAGE (QFN), 48 TERMINAL, 0.5 PITCH (7 X 7 X 1), PUNCH SINGULATION	CASE NUMBER: 1958–01	
	STANDARD: JEDEC MO–220 VKKD–2	
	PACKAGE CODE: 6232	SHEET: 2 OF 4