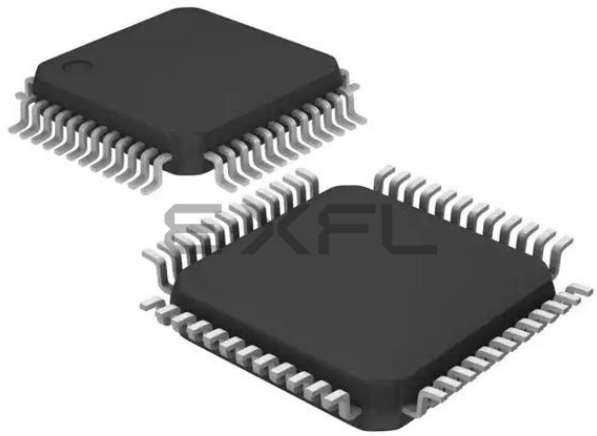

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Details	
Product Status	Active
Core Processor	12V1
Core Size	16-Bit
Speed	25MHz
Connectivity	CANbus, IrDA, LINbus, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	40
Program Memory Size	240KB (240K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	11K x 8
Voltage - Supply (Vcc/Vdd)	3.13V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s9s12g240f0mlf

Table 1-25. 100-Pin LQFP Pinout for S12GA96 and S12GA128

	Function <----lowest-----PRIORITY-----highest---->				Power Supply	Internal Pull Resistor	
Package Pin	Pin	2nd Func.	3rd Func.	4th Func.		CTRL	Reset State
86	PS4	MISO0	—	—	V_{DDX}	PERS/PPSS	Up
87	PS5	MOSI0	—	—	V_{DDX}	PERS/PPSS	Up
88	PS6	SCK0	—	—	V_{DDX}	PERS/PPSS	Up
89	PS7	API_EXTCLK	$\overline{SS0}$	—	V_{DDX}	PERS/PPSS	Up
90	VSSX2	—	—	—	—	—	—
91	VDDX2	—	—	—	—	—	—
92	PM0	RXCAN	—	—	V_{DDX}	PERM/PPSM	Disabled
93	PM1	TXCAN	—	—	V_{DDX}	PERM/PPSM	Disabled
94	PD4	—	—	—	V_{DDX}	PUCR/PUPDE	Disabled
95	PD5	—	—	—	V_{DDX}	PUCR/PUPDE	Disabled
96	PD6	—	—	—	V_{DDX}	PUCR/PUPDE	Disabled
97	PD7	—	—	—	V_{DDX}	PUCR/PUPDE	Disabled
98	PM2	RXD2	—	—	V_{DDX}	PERM/PPSM	Disabled
99	PM3	TXD2	—	—	V_{DDX}	PERM/PPSM	Disabled
100	PJ7	KWJ7	$\overline{SS2}$	—	V_{DDX}	PERJ/PPSJ	Up

[1] The regular I/O characteristics (see Section A.2, “I/O Characteristics”) apply if the EXTAL/XTAL function is disabled

Table 1-31. 100-Pin LQFP Pinout for S12GA192 and S12GA240

	Function <----lowest-----PRIORITY-----highest---->				Power Supply	Internal Pull Resistor	
Package Pin	Pin	2nd Func.	3rd Func.	4th Func.		CTRL	Reset State
57	PAD1	KWAD1	AN1	—	V_{DDA}	PER1AD/PPS1AD	Disabled
58	PAD9	KWAD9	AN9	—	V_{DDA}	PER0AD/PPS0AD	Disabled
59	PAD2	KWAD2	AN2	—	V_{DDA}	PER1AD/PPS1AD	Disabled
60	PAD10	KWAD10	AN10	AMP1	V_{DDA}	PER0AD/PPS0AD	Disabled
61	PAD3	KWAD3	AN3	—	V_{DDA}	PER1AD/PPS1AD	Disabled
62	PAD11	KWAD11	AN11	AMP0	V_{DDA}	PER0AD/PPS0AD	Disabled
63	PAD4	KWAD4	AN4	—	V_{DDA}	PER1AD/PPS1AD	Disabled
64	PAD12	KWAD12	AN12	—	V_{DDA}	PER0AD/PPS0AD	Disabled
65	PAD5	KWAD5	AN5	—	V_{DDA}	PER1AD/PPS1AD	Disabled
66	PAD13	KWAD13	AN13	AMPM0	V_{DDA}	PER0AD/PPS0AD	Disabled
67	PAD6	KWAD6	AN6	—	V_{DDA}	PER1AD/PPS1AD	Disabled
68	PAD14	KWAD14	AN14	AMPP0	V_{DDA}	PER0AD/PPS0AD	Disabled
69	PAD7	KWAD7	AN7	—	V_{DDA}	PER1AD/PPS1AD	Disabled
70	PAD15	KWAD15	AN15	DACU0	V_{DDA}	PER0AD/PPS0AD	Disabled
71	PC4	—	—	—	V_{DDA}	PUCR/PUPCE	Disabled
72	PC5	AMPM1	—	—	V_{DDA}	PUCR/PUPCE	Disabled
73	PC6	AMPP1	—	—	V_{DDA}	PUCR/PUPCE	Disabled
74	PC7	DACU1	—	—	V_{DDA}	PUCR/PUPCE	Disabled
75	VRH	—	—	—	—	—	—
76	VDDA	—	—	—	—	—	—
77	VSSA	—	—	—	—	—	—
78	PD0	—	—	—	V_{DDX}	PUCR/PUPDE	Disabled
79	PD1	—	—	—	V_{DDX}	PUCR/PUPDE	Disabled
80	PD2	—	—	—	V_{DDX}	PUCR/PUPDE	Disabled
81	PD3	—	—	—	V_{DDX}	PUCR/PUPDE	Disabled
82	PS0	RXD0	—	—	V_{DDX}	PERS/PPSS	Up
83	PS1	TXD0	—	—	V_{DDX}	PERS/PPSS	Up
84	PS2	RXD1	—	—	V_{DDX}	PERS/PPSS	Up
85	PS3	TXD1	—	—	V_{DDX}	PERS/PPSS	Up

Table 2-4. Signals and Priorities

Legend	
?	Signal available on pin
?	Routing option on pin
?	Routing reset location
	Not available on pin

Port	Pin	Signal	Signals per Device and Package (signal priority on pin from top to bottom)																				I/O	Description
			GA240 / GA192	G240 / G192	G128 / GA128 / G96 / GA96	GA240 / GA192	G240 / G192	G128 / GA128 / G96 / GA96	G64 / GA64 / G48 / GA48	GN48	GA240 / GA192	G240 / G192	G128 / GA128 / G96 / GA96	G64 / GA64 / G48 / GA48	GN48	GN32 / GNA32	GN16 / GNA16	G64 / G48	GN48	GN32	GN16	GN32	GN16		
			100			64					48							32				20			
E	PE1	XTAL	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	-	CPMU OSC signal
		TXD0																				?	?	I/O	SCI transmit
		IOC3																				?	?	I/O	Timer channel
		PWM1																				?	?	O	PWM channel
		ETRIG1																				?	?	I	ADC external trigger
		[PE1]	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	I/O	GPIO
	PE0	EXTAL	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	-	CPMU OSC signal
		RXD0																				?	?	I	SCI receive
		IOC2																				?	?	I/O	Timer channel
		PWM0																				?	?	O	PWM channel
		ETRIG0																				?	?	I	ADC external trigger
		[PE0]	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	I/O	GPIO
T	PT7-PT6	IOC7-IOC6	?	?	?	?	?	?																I/O	Timer channel
		[PTT7:PTT6]	?	?	?	?	?	?	?	?														I/O	GPIO
	PT5-PT4	IOC5-IOC4	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?							I/O	Timer channel
		[PTT5:PTT4]	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?							I/O	GPIO
	PT3-PT2	IOC3-IOC2	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?			I/O	Timer channel
		[PTT3:PTT2]	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?			I/O	GPIO
	PT1	$\overline{\text{IRQ}}$				?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	I	Maskable level- or falling-edge sensitive interrupt
		IOC1	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	I/O	Timer channel
		[PTT1]	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	I/O	GPIO
	PT0	$\overline{\text{XIRQ}}$				?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	I	Non-maskable level-sensitive interrupt
		IOC0	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	I/O	Timer channel
		[PTT0]	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	I/O	GPIO

Table 2-36. PTIT Register Field Descriptions

Field	Description
7-0 PTIT	**Port T input data—** A read always returns the buffered input state of the associated pin. It can be used to detect overload or short circuit conditions on output pins.

2.4.3.17 Port T Data Direction Register (DDRT)

Address 0x0242 (G1, G2) Access: User read/write[1]

	7	6	5	4	3	2	1	0
R W	DDRT7	DDRT6	DDRT5	DDRT4	DDRT3	DDRT2	DDRT1	DDRT0
Reset	0	0	0	0	0	0	0	0

Address 0x0242 (G3) Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	0	0	DDRT5	DDRT4	DDRT3	DDRT2	DDRT1	DDRT0
W								
Reset	0	0	0	0	0	0	0	0

Figure 2-18. Port T Data Direction Register (DDRT)

[1] Read: Anytime
Write: Anytime

Table 2-37. DDRT Register Field Descriptions

Field	Description
7-0 DDRT	**Port T data direction—** This bit determines whether the pin is a general-purpose input or output. 1 Associated pin configured as output 0 Associated pin configured as input

Chapter 7
Background Debug Module (S12SBDMV1)

Table 7-1. Revision History

Revision Number	Date	Sections Affected	Summary of Changes
1.03	14.May.2009		Internal Conditional text only
1.04	30.Nov.2009		Internal Conditional text only
1.05	07.Dec.2010		Standardized format of revision history table header.
1.06	02.Mar.2011	7.3.2.2/7-287 7.2/7-283	Corrected BPAE bit description. Removed references to fixed VCO frequencies

7.1 Introduction

This section describes the functionality of the background debug module (BDM) sub-block of the HCS12S core platform.

The background debug module (BDM) sub-block is a single-wire, background debug system implemented in on-chip hardware for minimal CPU intervention. All interfacing with the BDM is done via the BKGD pin.

The BDM has enhanced capability for maintaining synchronization between the target and host while allowing more flexibility in clock rates. This includes a sync signal to determine the communication rate and a handshake signal to indicate when an operation is complete. The system is backwards compatible to the BDM of the S12 family with the following exceptions:

- TAGGO command not supported by S12SBDM
- External instruction tagging feature is part of the DBG module
- S12SBDM register map and register content modified
- Family ID readable from BDM ROM at global address 0x3_FF0F in active BDM (value for devices with HCS12S core is 0xC2)
- Clock switch removed from BDM (CLKSW bit removed from BDMSTS register)

7.1.1 Features

The BDM includes these distinctive features:

- Single-wire communication with host development system
- Enhanced capability for allowing more flexibility in clock rates
- SYNC command to determine communication rate

NOTE

The ACK pulse does not provide a time out. This means for the GO_UNTIL command that it can not be distinguished if a stop or wait has been executed (command discarded and ACK not issued) or if the “UNTIL” condition (BDM active) is just not reached yet. Hence in any case where the ACK pulse of a command is not issued the possible pending command should be aborted before issuing a new command. See the handshake abort procedure described in Section 7.4.8, “Hardware Handshake Abort Procedure”.

7.4.8 Hardware Handshake Abort Procedure

The abort procedure is based on the SYNC command. In order to abort a command, which had not issued the corresponding ACK pulse, the host controller should generate a low pulse in the BKGD pin by driving it low for at least 128 serial clock cycles and then driving it high for one serial clock cycle, providing a speedup pulse. By detecting this long low pulse in the BKGD pin, the target executes the SYNC protocol, see Section 7.4.9, “SYNC — Request Timed Reference Pulse”, and assumes that the pending command and therefore the related ACK pulse, are being aborted. Therefore, after the SYNC protocol has been completed the host is free to issue new BDM commands. For BDM firmware READ or WRITE commands it can not be guaranteed that the pending command is aborted when issuing a SYNC before the corresponding ACK pulse. There is a short latency time from the time the READ or WRITE access begins until it is finished and the corresponding ACK pulse is issued. The latency time depends on the firmware READ or WRITE command that is issued and on the selected bus clock rate. When the SYNC command starts during this latency time the READ or WRITE command will not be aborted, but the corresponding ACK pulse will be aborted. A pending GO, TRACE1 or GO_UNTIL command can not be aborted. Only the corresponding ACK pulse can be aborted by the SYNC command.

Although it is not recommended, the host could abort a pending BDM command by issuing a low pulse in the BKGD pin shorter than 128 serial clock cycles, which will not be interpreted as the SYNC command. The ACK is actually aborted when a negative edge is perceived by the target in the BKGD pin. The short abort pulse should have at least 4 clock cycles keeping the BKGD pin low, in order to allow the negative edge to be detected by the target. In this case, the target will not execute the SYNC protocol but the pending command will be aborted along with the ACK pulse. The potential problem with this abort procedure is when there is a conflict between the ACK pulse and the short abort pulse. In this case, the target may not perceive the abort pulse. The worst case is when the pending command is a read command (i.e., READ_BYTE). If the abort pulse is not perceived by the target the host will attempt to send a new command after the abort pulse was issued, while the target expects the host to retrieve the accessed memory byte. In this case, host and target will run out of synchronism. However, if the command to be aborted is not a read command the short abort pulse could be used. After a command is aborted the target assumes the next negative edge, after the abort pulse, is the first bit of a new BDM command.

NOTE

The details about the short abort pulse are being provided only as a reference for the reader to better understand the BDM internal behavior. It is not recommended that this procedure be used in a real application.

14.4 Functional Description

The ADC12B12C consists of an analog sub-block and a digital sub-block.

14.4.1 Analog Sub-Block

The analog sub-block contains all analog electronics required to perform a single conversion. Separate power supplies VDDA and VSSA allow to isolate noise of other MCU circuitry from the analog sub-block.

14.4.1.1 Sample and Hold Machine

The Sample and Hold Machine controls the storage and charge of the sample capacitor to the voltage level of the analog signal at the selected ADC input channel.

During the sample process the analog input connects directly to the storage node.

The input analog signals are unipolar and must be within the potential range of VSSA to VDDA.

During the hold process the analog input is disconnected from the storage node.

14.4.1.2 Analog Input Multiplexer

The analog input multiplexer connects one of the 12 external analog input channels to the sample and hold machine.

14.4.1.3 Analog-to-Digital (A/D) Machine

The A/D Machine performs analog to digital conversions. The resolution is program selectable to be either 8 or 10 or 12 bits. The A/D machine uses a successive approximation architecture. It functions by comparing the sampled and stored analog voltage with a series of binary coded discrete voltages. By following a binary search algorithm, the A/D machine identifies the discrete voltage that is nearest to the sampled and stored voltage.

When not converting the A/D machine is automatically powered down.

Only analog input signals within the potential range of VRL to VRH (A/D reference potentials) will result in a non-railed digital output code.

14.4.2 Digital Sub-Block

This subsection describes some of the digital features in more detail. See Section 14.3.2, “Register Descriptions” for all details.

14.4.2.1 External Trigger Input

The external trigger feature allows the user to synchronize ATD conversions to an external event rather than relying only on software to trigger the ATD module when a conversions is about to take place. The external trigger signal (out of reset ATD channel 11, configurable in ATDCTL1) is programmable to be

15.3.2 Register Descriptions

This section describes in address order all the ADC10B16C registers and their individual bits.

15.3.2.1 ATD Control Register 0 (ATDCTL0)

Writes to this register will abort current conversion sequence.

Module Base + 0x0000

	7	6	5	4	3	2	1	0
R	Reserved	0	0	0	WRAP3	WRAP2	WRAP1	WRAP0
W								
Reset	0	0	0	0	1	1	1	1

= Unimplemented or Reserved

Figure 15-3. ATD Control Register 0 (ATDCTL0)

Read: Anytime

Write: Anytime, in special modes always write 0 to Reserved Bit 7.

Table 15-1. ATDCTL0 Field Descriptions

Field	Description
3-0 WRAP[3-0]	**Wrap Around Channel Select Bits** — These bits determine the channel for wrap around when doing multi-channel conversions. The coding is summarized in Table 15-2.

Table 15-2. Multi-Channel Wrap Around Coding

WRAP3	WRAP2	WRAP1	WRAP0	Multiple Channel Conversions (MULT = 1) Wraparound to AN0 after Converting
0	0	0	0	Reserved[1]
0	0	0	1	AN1
0	0	1	0	AN2
0	0	1	1	AN3
0	1	0	0	AN4
0	1	0	1	AN5
0	1	1	0	AN6
0	1	1	1	AN7
1	0	0	0	AN8
1	0	0	1	AN9
1	0	1	0	AN10
1	0	1	1	AN11
1	1	0	0	AN12
1	1	0	1	AN13
1	1	1	0	AN14
1	1	1	1	AN15

edge or level sensitive with polarity control. Table 16-23 gives a brief description of the different combinations of control bits and their effect on the external trigger function.

In order to avoid maybe false trigger events please enable the external digital input via ATDDIEN register first and in the following enable the external trigger mode by bit ETRIGE.

Table 16-23. External Trigger Control Bits

ETRIGLE	ETRIGP	ETRIGE	SCAN	Description
X	X	0	0	Ignores external trigger. Performs one conversion sequence and stops.
X	X	0	1	Ignores external trigger. Performs continuous conversion sequences.
0	0	1	X	Trigger falling edge sensitive. Performs one conversion sequence per trigger.
0	1	1	X	Trigger rising edge sensitive. Performs one conversion sequence per trigger.
1	0	1	X	Trigger low level sensitive. Performs continuous conversions while trigger level is active.
1	1	1	X	Trigger high level sensitive. Performs continuous conversions while trigger level is active.

In either level or edge sensitive mode, the first conversion begins when the trigger is received.

Once ETRIGE is enabled a conversion must be triggered externally after writing to ATDCTL5 register.

During a conversion in edge sensitive mode, if additional trigger events are detected the overrun error flag ETORF is set.

If level sensitive mode is active and the external trigger de-asserts and later asserts again during a conversion sequence, this does not constitute an overrun. Therefore, the flag is not set. If the trigger is left active in level sensitive mode when a sequence is about to complete, another sequence will be triggered immediately.

16.4.2.2 General-Purpose Digital Port Operation

Each ATD input pin can be switched between analog or digital input functionality. An analog multiplexer makes each ATD input pin selected as analog input available to the A/D converter.

The pad of the ATD input pin is always connected to the analog input channel of the analog mulitplexer.

Each pad input signal is buffered to the digital port register.

This buffer can be turned on or off with the ATDDIEN register for each ATD input pin.
This is important so that the buffer does not draw excess current when an ATD input pin is selected as analog input to the ADC12B16C.

17.3.4 AMPM Input Pin

This analog pin is used as input for the operational amplifier negative input pin, if the according mode is selected, see register bit DACM[2:0].

17.4 Memory Map and Register Definition

This sections provides the detailed information of all registers for the DAC_8B5V module.

17.4.1 Register Summary

Figure 17-2 shows the summary of all implemented registers inside the DAC_8B5V module.

NOTE

Register Address = Module Base Address + Address Offset, where the Module Base Address is defined at the MCU level and the Address Offset is defined at the module level.

Address Offset / Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0000 DACCTL	R	FVR	DRIVE	0	0	0	DACM[2:0]		
	W								
0x0001 Reserved	R	0	0	0	0	0	0	0	0
	W								
0x0002 DACVOL	R	VOLTAGE[7:0]							
	W								
0x0003 - 0x0006 Reserved	R	0	0	0	0	0	0	0	0
	W								
0x0007 Reserved	R	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	W								
0x0007 DACDEBUG	R	0	BUF_EN	DAC_EN	S3	S2n	S2p	S1n	S1p
	W								

= Unimplemented

Figure 17-2. DAC_8B5V Register Summaryfv_dac_8b5v_RESERVED

Module Base + 0x00X2

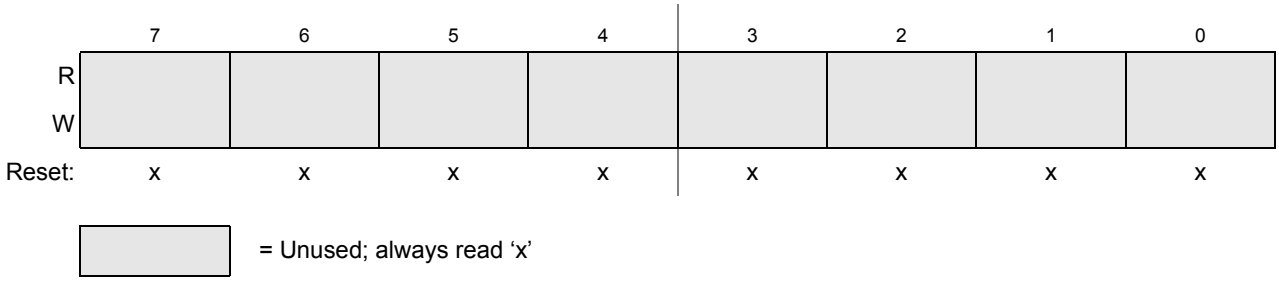

Figure 18-32. Identifier Register 2 — Standard Mapping

Module Base + 0x00X3

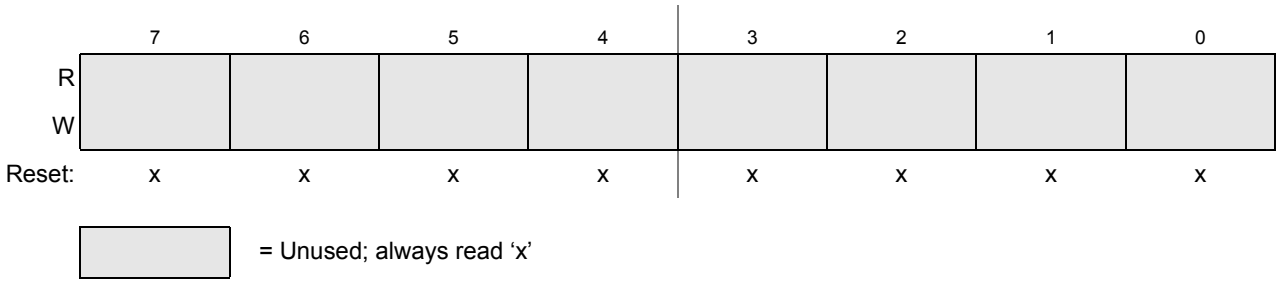

Figure 18-33. Identifier Register 3 — Standard Mapping

18.3.3.2 Data Segment Registers (DSR0-7)

The eight data segment registers, each with bits DB[7:0], contain the data to be transmitted or received. The number of bytes to be transmitted or received is determined by the data length code in the corresponding DLR register.

Module Base + 0x00X4 to Module Base + 0x00XB

	7	6	5	4	3	2	1	0
R W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Reset:	x	x	x	x	x	x	x	x

Figure 18-34. Data Segment Registers (DSR0–DSR7) — Extended Identifier Mapping

Table 18-33. DSR0–DSR7 Register Field Descriptions

Field	Description
7-0 DB[7:0]	**Data bits 7-0**

- Clock prescaling.
- 16-bit counter.
- 16-bit pulse accumulator on channel 7 .

23.1.2 Modes of Operation

Stop: Timer is off because clocks are stopped.

Freeze: Timer counter keeps on running, unless TSFRZ in TSCR1 is set to 1.

Wait: Counters keeps on running, unless TSWAI in TSCR1 is set to 1.

Normal: Timer counter keep on running, unless TEN in TSCR1 is cleared to 0.

23.1.3 Block Diagrams

The user code stored in the P-Flash memory must have a method of receiving the backdoor keys from an external stimulus. This external stimulus would typically be through one of the on-chip serial ports.

If the KEYEN[1:0] bits are in the enabled state (see Section 26.3.2.2), the MCU can be unsecured by the backdoor key access sequence described below:

1. Follow the command sequence for the Verify Backdoor Access Key command as explained in Section 26.4.6.11
2. If the Verify Backdoor Access Key command is successful, the MCU is unsecured and the SEC[1:0] bits in the FSEC register are forced to the unsecure state of 10

The Verify Backdoor Access Key command is monitored by the Memory Controller and an illegal key will prohibit future use of the Verify Backdoor Access Key command. A reset of the MCU is the only method to re-enable the Verify Backdoor Access Key command. The security as defined in the Flash security byte (0x3_FF0F) is not changed by using the Verify Backdoor Access Key command sequence. The backdoor keys stored in addresses 0x3_FF00-0x3_FF07 are unaffected by the Verify Backdoor Access Key command sequence. The Verify Backdoor Access Key command sequence has no effect on the program and erase protections defined in the Flash protection register, FPROT.

After the backdoor keys have been correctly matched, the MCU will be unsecured. After the MCU is unsecured, the sector containing the Flash security byte can be erased and the Flash security byte can be reprogrammed to the unsecure state, if desired. In the unsecure state, the user has full control of the contents of the backdoor keys by programming addresses 0x3_FF00-0x3_FF07 in the Flash configuration field.

26.5.2 Unsecuring the MCU in Special Single Chip Mode using BDM

A secured MCU can be unsecured in special single chip mode by using the following method to erase the P-Flash and EEPROM memory:

1. Reset the MCU into special single chip mode
2. Delay while the BDM executes the Erase Verify All Blocks command write sequence to check if the P-Flash and EEPROM memories are erased
3. Send BDM commands to disable protection in the P-Flash and EEPROM memory
4. Execute the Erase All Blocks command write sequence to erase the P-Flash and EEPROM memory. Alternatively the Unsecure Flash command can be executed, if so the steps 5 and 6 below are skeeped.
5. After the CCIF flag sets to indicate that the Erase All Blocks operation has completed, reset the MCU into special single chip mode
6. Delay while the BDM executes the Erase Verify All Blocks command write sequence to verify that the P-Flash and EEPROM memory are erased

If the P-Flash and EEPROM memory are verified as erased, the MCU will be unsecured. All BDM commands will now be enabled and the Flash security byte may be programmed to the unsecure state by continuing with the following steps:

7. Send BDM commands to execute the Program P-Flash command write sequence to program the Flash security byte to the unsecured state

Upon clearing CCIF to launch the Set User Margin Level command, the Memory Controller will set the user margin level for the targeted block and then set the CCIF flag.

NOTE

When the EEPROM block is targeted, the EEPROM user margin levels are applied only to the EEPROM reads. However, when the P-Flash block is targeted, the P-Flash user margin levels are applied to both P-Flash and EEPROM reads. It is not possible to apply user margin levels to the P-Flash block only.

Valid margin level settings for the Set User Margin Level command are defined in Table 27-55.

Table 27-55. Valid Set User Margin Level Settings

CCOB (CCOBIX=001)	Level Description
0x0000	Return to Normal Level
0x0001	User Margin-1 Level[1]
0x0002	User Margin-0 Level[2]

[1] Read margin to the erased state

[2] Read margin to the programmed state

Table 27-56. Set User Margin Level Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 001 at command launch
		Set if command not available in current mode (see Table 27-27)
		Set if an invalid FlashBlockSelectionCode[1:0] is supplied (See Table 27-34)
		Set if an invalid margin level setting is supplied
	FPVIOL	None
	MGSTAT1	None
	MGSTAT0	None

NOTE

User margin levels can be used to check that Flash memory contents have adequate margin for normal level read operations. If unexpected results are encountered when checking Flash memory contents at user margin levels, a potential loss of information has been detected.

Offset Module Base + 0x0013

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 28-25. Flash Reserved7 Register (FRSV7)

All bits in the FRSV7 register read 0 and are not writable.

28.4 Functional Description

28.4.1 Modes of Operation

The FTMRG96K1 module provides the modes of operation normal and special . The operating mode is determined by module-level inputs and affects the FCLKDIV, FCNFG, and EEPROT registers (see Table 28-27).

28.4.2 IFR Version ID Word

The version ID word is stored in the IFR at address 0x0_40B6. The contents of the word are defined in Table 28-26.

Table 28-26. IFR Version ID Fields

[15:4]	[3:0]
Reserved	VERNUM

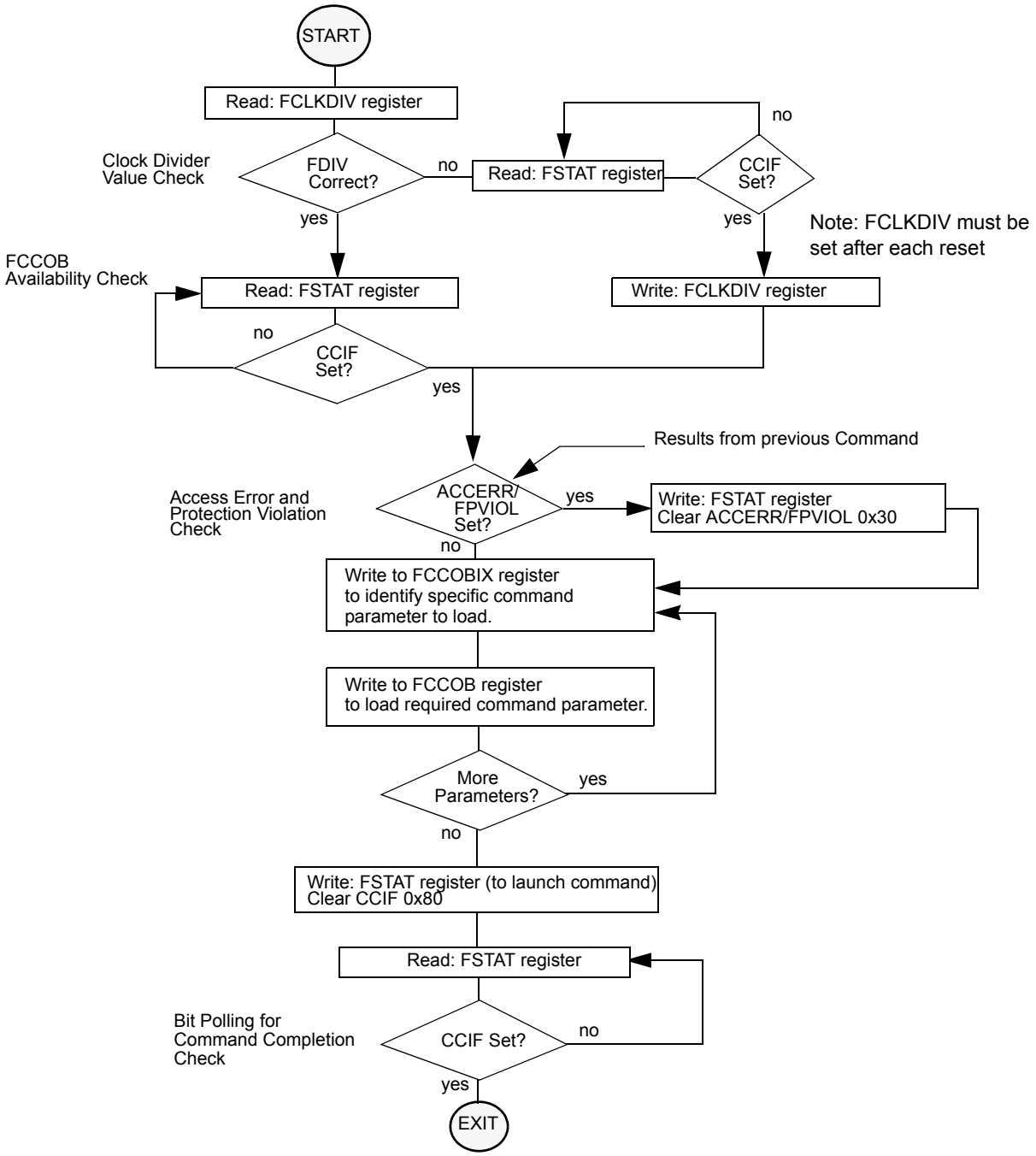

Figure 28-26. Generic Flash Command Write Sequence Flowchart

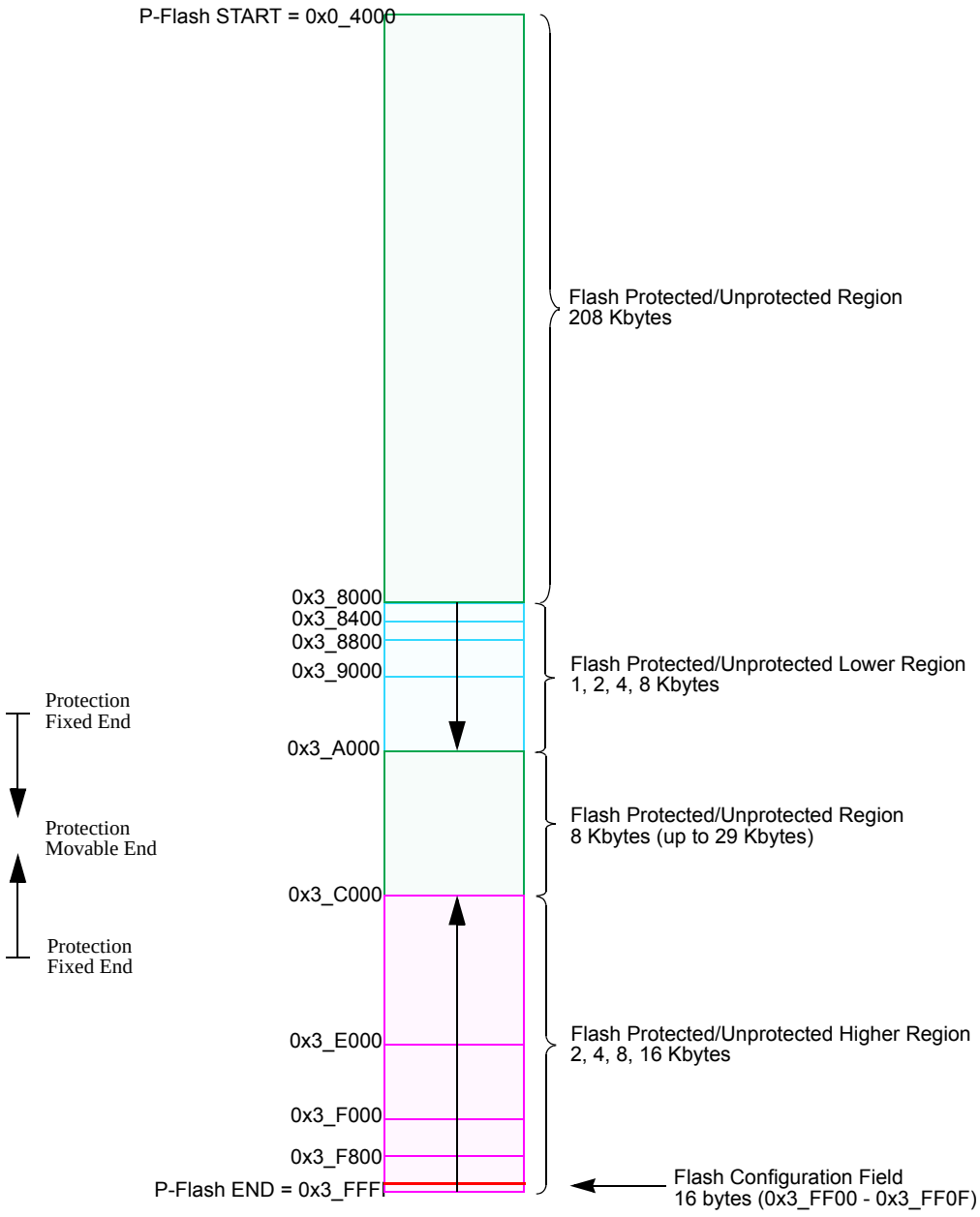

Figure 31-2. P-Flash Memory Map

Table 31-5. Program IFR Fields

Global Address	Size (Bytes)	Field Description
0x0_4000 – 0x0_4007	8	Reserved
0x0_4008 – 0x0_40B5	174	Reserved
0x0_40B6 – 0x0_40B7	2	Version ID[1]

Table A-5. Thermal Package Characteristics[1]

Num	C	Rating	Symbol	S12GN32, S12GNA32, S12GN16, S12GNA16	S12G64, S12GA64, S12G48, S12GN48, S12GA64	S12G128, S12GA128, S12G96, S12GA96	S12G240, S12GA240, S12G192, S12GA192	Unit
48-pin QFN								
22	D	Thermal resistance single sided PCB, natural convection[2]	θ_{JA}	82				°C/W
23	D	Thermal resistance single sided PCB @ 200 ft/min[3]	θ_{JMA}	67				°C/W
24	D	Thermal resistance double sided PCB with 2 internal planes, natural convection[3]	θ_{JA}	28				°C/W
25	D	Thermal resistance double sided PCB with 2 internal planes @ 200 ft/min[3]	θ_{JMA}	23				°C/W
26	D	Junction to Board[4]	θ_{JB}	11				°C/W
27	D	Junction to Case[5]	θ_{JC}	N/A				°C/W
28	D	Junction to Package Top[6]	Ψ_{JT}	4				°C/W
64-pin LQFP								
29	D	Thermal resistance single sided PCB, natural convection[2]	θ_{JA}		70	70	70	°C/W
30	D	Thermal resistance single sided PCB @ 200 ft/min[3]	θ_{JMA}		59	58	58	°C/W
31	D	Thermal resistance double sided PCB with 2 internal planes, natural convection[3]	θ_{JA}		52	52	52	°C/W
32	D	Thermal resistance double sided PCB with 2 internal planes @ 200 ft/min[3]	θ_{JMA}		46	46	45	°C/W
33	D	Junction to Board[4]	θ_{JB}		34	34	35	°C/W
34	D	Junction to Case[5]	θ_{JC}		20	18	17	°C/W
35	D	Junction to Package Top[6]	Ψ_{JT}		5	4	N/A	°C/W
100-pin LQFP								
36	D	Thermal resistance single sided PCB, natural convection[2]	θ_{JA}			61	62	°C/W
37	D	Thermal resistance single sided PCB @ 200 ft/min[3]	θ_{JMA}			51	55	°C/W
38	D	Thermal resistance double sided PCB with 2 internal planes, natural convection[3]	θ_{JA}			49	51	°C/W
39	D	Thermal resistance double sided PCB with 2 internal planes @ 200 ft/min[3]	θ_{JMA}			43	47	°C/W
40	D	Junction to Board[4]	θ_{JB}			34	37	°C/W
41	D	Junction to Case[5]	θ_{JC}			16	17	°C/W
42	D	Junction to Package Top[6]	Ψ_{JT}			3	N/A	°C/W

0x00A0–0x0C7 Pulse-Width-Modulator (PWM)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x00A0	PWME	R	PWME7	PWME6	PWME5	PWME4	PWME3	PWME2	PWME1	PWME0
		W								
0x00A1	PWMPOL	R	PPOL7	PPOL6	PPOL5	PPOL4	PPOL3	PPOL2	PPOL1	PPOL0
		W								
0x00A2	PWMCLK	R	PCLK7	PCLKL6	PCLK5	PCLK4	PCLK3	PCLK2	PCLK1	PCLK0
		W								
0x00A3	PWMPRCLK	R	0	PCKB2	PCKB1	PCKB0	0	PCKA2	PCKA1	PCKA0
		W								
0x00A4	PWMCAE	R	CAE7	CAE6	CAE5	CAE4	CAE3	CAE2	CAE1	CAE0
		W								
0x00A5	PWMCTL	R	CON67	CON45	CON23	CON01	PSWAI	PFRZ	0	0
		W								
0x00A6	PWMCLKAB	R	PCLKAB7	PCLKAB6	PCLKAB5	PCLKAB4	PCLKAB3	PCLKAB2	PCLKAB1	PCLKAB0
		W								
0x00A7	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x00A8	PWMSCLA	R	Bit 7	6	5	4	3	2	1	Bit 0
		W								
0x00A9	PWMSCLB	R	Bit 7	6	5	4	3	2	1	Bit 0
		W								
0x00AA - 0x00AB	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x00AC	PWMCNT0	R	Bit 7	6	5	4	3	2	1	Bit 0
		W	0	0	0	0	0	0	0	0
0x00AD	PWMCNT1	R	Bit 7	6	5	4	3	2	1	Bit 0
		W	0	0	0	0	0	0	0	0
0x00AE	PWMCNT2	R	Bit 7	6	5	4	3	2	1	Bit 0
		W	0	0	0	0	0	0	0	0
0x00AF	PWMCNT3	R	Bit 7	6	5	4	3	2	1	Bit 0
		W	0	0	0	0	0	0	0	0
0x0B0	PWMCNT4	R	Bit 7	6	5	4	3	2	1	Bit 0
		W	0	0	0	0	0	0	0	0
0x00B1	PWMCNT5	R	Bit 7	6	5	4	3	2	1	Bit 0
		W	0	0	0	0	0	0	0	0
0x00B2	PWMCNT6	R	Bit 7	6	5	4	3	2	1	Bit 0
		W	0	0	0	0	0	0	0	0
0x00B3	PWMCNT7	R	Bit 7	6	5	4	3	2	1	Bit 0
		W	0	0	0	0	0	0	0	0
0x00B4	PWMPER0	R	Bit 7	6	5	4	3	2	1	Bit 0
		W								
0x00B5	PWMPER1	R	Bit 7	6	5	4	3	2	1	Bit 0
		W								
0x00B6	PWMPER2	R	Bit 7	6	5	4	3	2	1	Bit 0
		W								

Table D-1. Bondpad Coordinates

Die Pad	Bond Post	Die Pad X Coordinate	Die Pad Y Coordinate	Function
88	87	128.5	-1472.06	PS[5]
89	88	14.5	-1472.06	PS[6]
90	89	-99.5	-1472.06	PS[7]
91	90	-213.5	-1472.06	VSSX2
92	91	-318.5	-1472.06	VDDX2
93	92	-428.5	-1472.06	PM[0]
94	93	-548.5	-1472.06	PM[1]
95	94	-688.5	-1472.06	PD[4]
96	95	-828.5	-1472.06	PD[5]
97	96	-998.5	-1472.06	PD[6]
98	97	-1168.5	-1472.06	PD[7]
99	98	-1338.5	-1472.06	PM[2]
100	99	-1518.5	-1472.06	PM[3]
101	100	-1707.5	-1472.06	PJ[7]