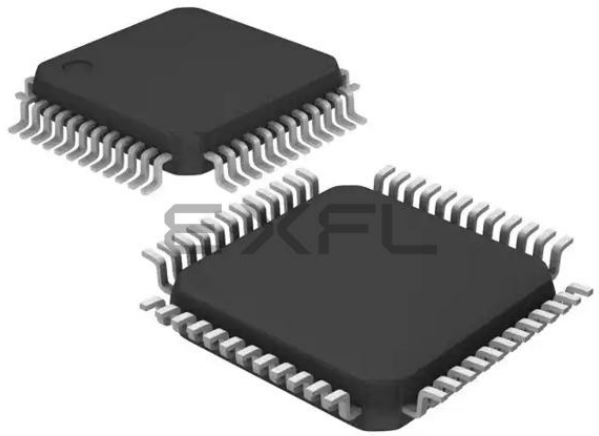

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Program Memory Type	FLASH
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Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s9s12g240f0mlfr

Table 2-36. PTIT Register Field Descriptions

Field	Description
7-0 PTIT	**Port T input data—** A read always returns the buffered input state of the associated pin. It can be used to detect overload or short circuit conditions on output pins.

2.4.3.17 Port T Data Direction Register (DDRT)

Address 0x0242 (G1, G2) Access: User read/write[1]

	7	6	5	4	3	2	1	0
R W	DDRT7	DDRT6	DDRT5	DDRT4	DDRT3	DDRT2	DDRT1	DDRT0
Reset	0	0	0	0	0	0	0	0

Address 0x0242 (G3) Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	0	0	DDRT5	DDRT4	DDRT3	DDRT2	DDRT1	DDRT0
W								
Reset	0	0	0	0	0	0	0	0

Figure 2-18. Port T Data Direction Register (DDRT)

[1] Read: Anytime
Write: Anytime

Table 2-37. DDRT Register Field Descriptions

Field	Description
7-0 DDRT	**Port T data direction—** This bit determines whether the pin is a general-purpose input or output. 1 Associated pin configured as output 0 Associated pin configured as input

2.4.3.31 Port M Polarity Select Register (PPSM)

Address 0x0255 (G1, G2) Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	0	0	0	0	PPSM3	PPSM2	PPSM1	PPSM0
W								
Reset	0	0	0	0	0	0	0	0

Address 0x0255 (G3) Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	PPSM1	PPSM0
W								
Reset	0	0	0	0	0	0	0	0

Figure 2-32. Port M Polarity Select Register (PPSM)

[1] Read: Anytime
Write: Anytime

Table 2-56. PPSM Register Field Descriptions

Field	Description
3-0 PPSM	**Port M pull device select**—Configure pull device polarity on input pin This bit selects a pullup or a pulldown device if enabled on the associated port input pin. 1 Pulldown device selected 0 Pullup device selected

2.4.3.32 Port M Wired-Or Mode Register (WOMM)

Address 0x0256 (G1, G2) Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	0	0	0	0	WOMM3	WOMM2	WOMM1	WOMM0
W								
Reset	0	0	0	0	0	0	0	0

Address 0x0256 (G3) Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	WOMM1	WOMM0
W								
Reset	0	0	0	0	0	0	0	0

Figure 2-33. Port M Wired-Or Mode Register (WOMM)

[1] Read: Anytime
Write: Anytime

2.4.3.43 Port J Input Register (PTIJ)

Address 0x0269 (G1, G2) Access: User read only[1]

	7	6	5	4	3	2	1	0
R	PTIJ7	PTIJ6	PTIJ5	PTIJ4	PTIJ3	PTIJ2	PTIJ1	PTIJ0
W								
Reset	0	0	0	0	0	0	0	0

Address 0x0269 (G3) Access: User read only[1]

	7	6	5	4	3	2	1	0
R	0	0	0	0	PTIJ3	PTIJ2	PTIJ1	PTIJ0
W								
Reset	0	0	0	0	0	0	0	0

Figure 2-43. Port J Input Register (PTIJ)

[1] Read: Anytime
Write:Never

Table 2-69. PTIJ Register Field Descriptions

Field	Description
7-0 PTIJ	**Port J input data—** A read always returns the buffered input state of the associated pin. It can be used to detect overload or short circuit conditions on output pins.

2.4.3.44 Port J Data Direction Register (DDRJ)

Address 0x026A (G1, G2) Access: User read/write[1]

	7	6	5	4	3	2	1	0
R W	DDRJ7	DDRJ6	DDRJ5	DDRJ4	DDRJ3	DDRJ2	DDRJ1	DDRJ0
Reset	0	0	0	0	0	0	0	0

Address 0x026A (G3) Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	0	0	0	0	DDRJ3	DDRJ2	DDRJ1	DDRJ0
W								
Reset	0	0	0	0	0	0	0	0

Figure 2-44. Port J Data Direction Register (DDRJ)

[1] Read: Anytime
Write: Anytime

16.1.2 Modes of Operation

16.1.2.1 Conversion Modes

There is software programmable selection between performing **single** or **continuous conversion** on a **single channel** or **multiple channels**.

16.1.2.2 MCU Operating Modes

- **Stop Mode**
  Entering Stop Mode aborts any conversion sequence in progress and if a sequence was aborted restarts it after exiting stop mode. This has the same effect/consequences as starting a conversion sequence with write to ATDCTL5. So after exiting from stop mode with a previously aborted sequence all flags are cleared etc.
- **Wait Mode**
  ADC12B16C behaves same in Run and Wait Mode. For reduced power consumption continuous conversions should be aborted before entering Wait mode.
- **Freeze Mode**
  In Freeze Mode the ADC12B16C will either continue or finish or stop converting according to the FRZ1 and FRZ0 bits. This is useful for debugging and emulation.

Module Base + 0x0001 Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	CANE	CLKSRC	LOOPB	LISTEN	BORM	WUPM	SLPAK	INITAK
W								
Reset:	0	0	0	1	0	0	0	1

= Unimplemented

Figure 18-5. MSCAN Control Register 1 (CANCTL1)

[1] Read: Anytime
Write: Anytime in initialization mode (INITRQ = 1 and INITAK = 1), except CANE which is write once in normal and anytime in special system operation modes when the MSCAN is in initialization mode (INITRQ = 1 and INITAK = 1)

Table 18-4. CANCTL1 Register Field Descriptions

Field	Description
7 CANE	**MSCAN Enable** 0 MSCAN module is disabled 1 MSCAN module is enabled
6 CLKSRC	**MSCAN Clock Source** — This bit defines the clock source for the MSCAN module (only for systems with a clock generation module; Section 18.4.3.2, “Clock System,” and Section Figure 18-43., “MSCAN Clocking Scheme,”). 0 MSCAN clock source is the oscillator clock 1 MSCAN clock source is the bus clock
5 LOOPB	**Loopback Self Test Mode** — When this bit is set, the MSCAN performs an internal loopback which can be used for self test operation. The bit stream output of the transmitter is fed back to the receiver internally. The RXCAN input is ignored and the TXCAN output goes to the recessive state (logic 1). The MSCAN behaves as it does normally when transmitting and treats its own transmitted message as a message received from a remote node. In this state, the MSCAN ignores the bit sent during the ACK slot in the CAN frame acknowledge field to ensure proper reception of its own message. Both transmit and receive interrupts are generated. 0 Loopback self test disabled 1 Loopback self test enabled
4 LISTEN	**Listen Only Mode** — This bit configures the MSCAN as a CAN bus monitor. When LISTEN is set, all valid CAN messages with matching ID are received, but no acknowledgement or error frames are sent out (see Section 18.4.4.4, “Listen-Only Mode”). In addition, the error counters are frozen. Listen only mode supports applications which require “hot plugging” or throughput analysis. The MSCAN is unable to transmit any messages when listen only mode is active. 0 Normal operation 1 Listen only mode activated
3 BORM	**Bus-Off Recovery Mode** — This bit configures the bus-off state recovery mode of the MSCAN. Refer to Section 18.5.2, “Bus-Off Recovery,” for details. 0 Automatic bus-off recovery (see Bosch CAN 2.0A/B protocol specification) 1 Bus-off recovery upon user request
2 WUPM	**Wake-Up Mode** — If WUPE in CANCTL0 is enabled, this bit defines whether the integrated low-pass filter is applied to protect the MSCAN from spurious wake-up (see Section 18.4.5.5, “MSCAN Sleep Mode”). 0 MSCAN wakes up on any dominant level on the CAN bus 1 MSCAN wakes up only in case of a dominant pulse on the CAN bus that has a length of T_{wup}

Table 18-7. Baud Rate Prescaler

BRP5	BRP4	BRP3	BRP2	BRP1	BRP0	Prescaler value (P)
0	0	0	0	0	0	1
0	0	0	0	0	1	2
0	0	0	0	1	0	3
0	0	0	0	1	1	4
:	:	:	:	:	:	:
1	1	1	1	1	1	64

18.3.2.4 MSCAN Bus Timing Register 1 (CANBTR1)

The CANBTR1 register configures various CAN bus timing parameters of the MSCAN module.

Module Base + 0x0003 Access: User read/write[1]

	7	6	5	4	3	2	1	0
R W	SAMP	TSEG22	TSEG21	TSEG20	TSEG13	TSEG12	TSEG11	TSEG10
Reset:	0	0	0	0	0	0	0	0

Figure 18-7. MSCAN Bus Timing Register 1 (CANBTR1)

1 Read: Anytime
Write: Anytime in initialization mode (INITRQ = 1 and INITAK = 1)

Table 18-8. CANBTR1 Register Field Descriptions

Field	Description
7 SAMP	**Sampling** — This bit determines the number of CAN bus samples taken per bit time. 0 One sample per bit. 1 Three samples per bit[1]. If SAMP = 0, the resulting bit value is equal to the value of the single bit positioned at the sample point. If SAMP = 1, the resulting bit value is determined by using majority rule on the three total samples. For higher bit rates, it is recommended that only one sample is taken per bit time (SAMP = 0).
6-4 TSEG2[2:0]	**Time Segment 2** — Time segments within the bit time fix the number of clock cycles per bit time and the location of the sample point (see Figure 18-44). Time segment 2 (TSEG2) values are programmable as shown in Table 18-9.
3-0 TSEG1[3:0]	**Time Segment 1** — Time segments within the bit time fix the number of clock cycles per bit time and the location of the sample point (see Figure 18-44). Time segment 1 (TSEG1) values are programmable as shown in Table 18-10.

1 In this case, PHASE_SEG1 must be at least 2 time quanta (Tq).

The clock source of each PWM channel is determined by PCLKx bits in PWMCLK (see Section 19.3.2.3, “PWM Clock Select Register (PWMCLK)) and PCLKABx bits in PWMCLKAB as shown in Table 19-5 and Table 19-6.

19.3.2.8 PWM Scale A Register (PWMSCLA)

PWMSCLA is the programmable scale value used in scaling clock A to generate clock SA. Clock SA is generated by taking clock A, dividing it by the value in the PWMSCLA register and dividing that by two.

Clock SA = Clock A / (2 * PWMSCLA)

NOTE

When PWMSCLA = $00, PWMSCLA value is considered a full scale value of 256. Clock A is thus divided by 512.

Any value written to this register will cause the scale counter to load the new scale value (PWMSCLA).

Module Base + 0x0008

	7	6	5	4	3	2	1	0
R W	Bit 7	6	5	4	3	2	1	Bit 0
Reset	0	0	0	0	0	0	0	0

Figure 19-10. PWM Scale A Register (PWMSCLA)

Read: Anytime

Write: Anytime (causes the scale counter to load the PWMSCLA value)

19.3.2.9 PWM Scale B Register (PWMSCLB)

PWMSCLB is the programmable scale value used in scaling clock B to generate clock SB. Clock SB is generated by taking clock B, dividing it by the value in the PWMSCLB register and dividing that by two.

Clock SB = Clock B / (2 * PWMSCLB)

NOTE

When PWMSCLB = $00, PWMSCLB value is considered a full scale value of 256. Clock B is thus divided by 512.

Any value written to this register will cause the scale counter to load the new scale value (PWMSCLB).

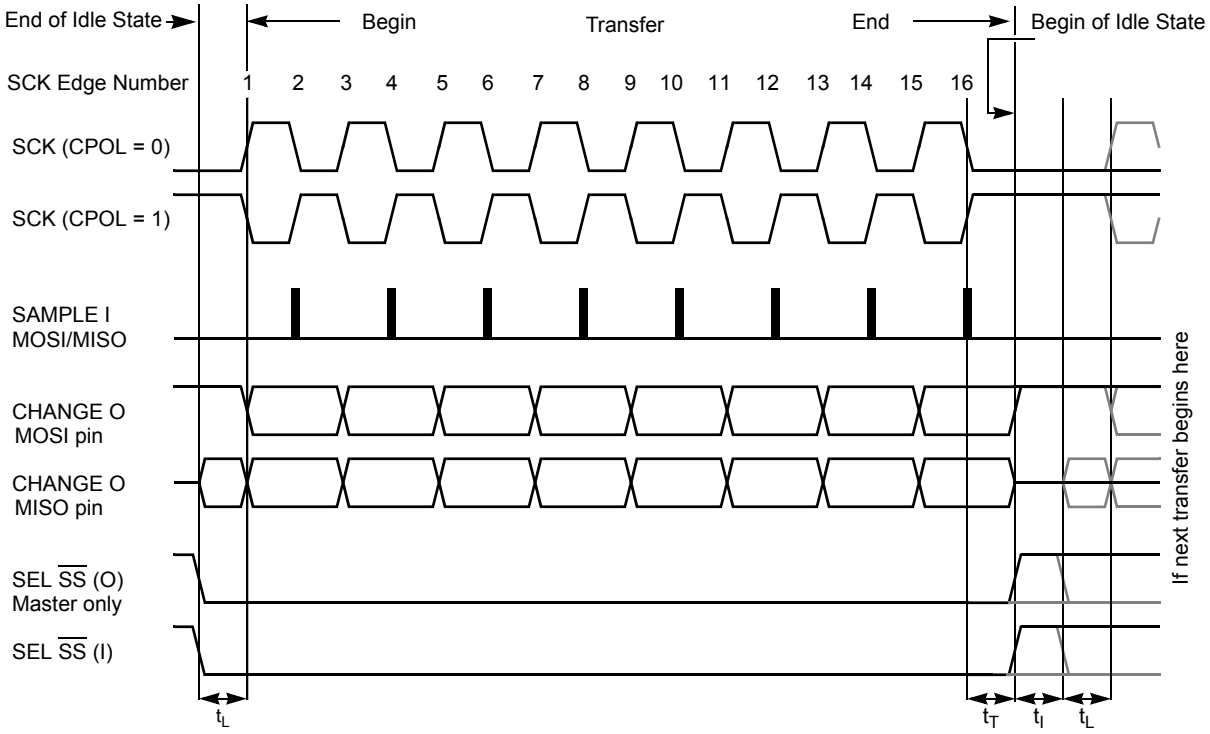
Module Base + 0x0009

	7	6	5	4	3	2	1	0
R W	Bit 7	6	5	4	3	2	1	Bit 0
Reset	0	0	0	0	0	0	0	0

Figure 19-11. PWM Scale B Register (PWMSCLB)

Read: Anytime

Write: Anytime (causes the scale counter to load the PWMSCLB value).



t_L = Minimum leading time before the first SCK edge, not required for back-to-back transfers

t_T = Minimum trailing time after the last SCK edge

t_I = Minimum idling time between transfers (minimum $\overline{SS}$ high time), not required for back-to-back transfers

Figure 21-14. SPI Clock Format 1 (CPHA = 1), with 8-Bit Transfer Width selected (XFRW = 0)

NOTE

Care must be taken when expecting data from a master while the slave is in wait or stop mode. Even though the shift register will continue to operate, the rest of the SPI is shut down (i.e., a SPIF interrupt will **not** be generated until exiting stop or wait mode). Also, the byte from the shift register will not be copied into the SPIDR register until after the slave SPI has exited wait or stop mode. In slave mode, a received byte pending in the receive shift register will be lost when entering wait or stop mode. An SPIF flag and SPIDR copy is generated only if wait mode is entered or exited during a tranmission. If the slave enters wait mode in idle mode and exits wait mode in idle mode, neither a SPIF nor a SPIDR copy will occur.

21.4.7.3 SPI in Stop Mode

Stop mode is dependent on the system. The SPI enters stop mode when the module clock is disabled (held high or low). If the SPI is in master mode and exchanging data when the CPU enters stop mode, the transmission is frozen until the CPU exits stop mode. After stop, data to and from the external SPI is exchanged correctly. In slave mode, the SPI will stay synchronized with the master.

The stop mode is not dependent on the SPISWAI bit.

21.4.7.4 Reset

The reset values of registers and signals are described in Section 21.3, “Memory Map and Register Definition”, which details the registers and their bit fields.

- If a data transmission occurs in slave mode after reset without a write to SPIDR, it will transmit garbage, or the data last received from the master before the reset.
- Reading from the SPIDR after reset will always read zeros.

21.4.7.5 Interrupts

The SPI only originates interrupt requests when SPI is enabled (SPE bit in SPICR1 set). The following is a description of how the SPI makes a request and how the MCU should acknowledge that request. The interrupt vector offset and interrupt priority are chip dependent.

The interrupt flags MODF, SPIF, and SPTEF are logically ORed to generate an interrupt request.

21.4.7.5.1 MODF

MODF occurs when the master detects an error on the $\overline{SS}$ pin. The master SPI must be configured for the MODF feature (see Table 21-2). After MODF is set, the current transfer is aborted and the following bit is changed:

- MSTR = 0, The master bit in SPICR1 resets.

The MODF interrupt is reflected in the status register MODF flag. Clearing the flag will also clear the interrupt. This interrupt will stay active while the MODF flag is set. MODF has an automatic clearing process which is described in Section 21.3.2.4, “SPI Status Register (SPISR)”.

24.4.6 Flash Command Description

This section provides details of all available Flash commands launched by a command write sequence. The ACCERR bit in the FSTAT register will be set during the command write sequence if any of the following illegal steps are performed, causing the command not to be processed by the Memory Controller:

- Starting any command write sequence that programs or erases Flash memory before initializing the FCLKDIV register
- Writing an invalid command as part of the command write sequence
- For additional possible errors, refer to the error handling table provided for each command

If a Flash block is read during execution of an algorithm (CCIF = 0) on that same block, the read operation will return invalid data if both flags SFDIF and DFDIF are set. If the SFDIF or DFDIF flags were not previously set when the invalid read operation occurred, both the SFDIF and DFDIF flags will be set.

If the ACCERR or FPVIOL bits are set in the FSTAT register, the user must clear these bits before starting any command write sequence (see Section 24.3.2.7).

CAUTION

A Flash word or phrase must be in the erased state before being programmed. Cumulative programming of bits within a Flash word or phrase is not allowed.

24.4.6.1 Erase Verify All Blocks Command

The Erase Verify All Blocks command will verify that all P-Flash and EEPROM blocks have been erased.

Table 24-29. Erase Verify All Blocks Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x01	Not required

Upon clearing CCIF to launch the Erase Verify All Blocks command, the Memory Controller will verify that the entire Flash memory space is erased. The CCIF flag will set after the Erase Verify All Blocks operation has completed. If all blocks are not erased, it means blank check failed, both MGSTAT bits will be set.

Table 24-30. Erase Verify All Blocks Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 000 at command launch
	FPVIOL	None
	MGSTAT1	Set if any errors have been encountered during the read[1] or if blank check failed .
	MGSTAT0	Set if any non-correctable errors have been encountered during the read or if blank check failed.

[1] As found in the memory map for FTMRG32K1.

Table 25-24. FCCOB - NVM Command Mode (Typical Usage)

CCOBIX[2:0]	Byte	FCCOB Parameter Fields (NVM Command Mode)
010	HI	Data 0 [15:8]
	LO	Data 0 [7:0]
011	HI	Data 1 [15:8]
	LO	Data 1 [7:0]
100	HI	Data 2 [15:8]
	LO	Data 2 [7:0]
101	HI	Data 3 [15:8]
	LO	Data 3 [7:0]

25.3.2.12 Flash Reserved1 Register (FRSV1)

This Flash register is reserved for factory testing.

Offset Module Base + 0x000C

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 25-18. Flash Reserved1 Register (FRSV1)

All bits in the FRSV1 register read 0 and are not writable.

25.3.2.13 Flash Reserved2 Register (FRSV2)

This Flash register is reserved for factory testing.

Offset Module Base + 0x000D

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 25-19. Flash Reserved2 Register (FRSV2)

All bits in the FRSV2 register read 0 and are not writable.

25.3.2.14 Flash Reserved3 Register (FRSV3)

This Flash register is reserved for factory testing.

27.4.6.13 Set Field Margin Level Command

The Set Field Margin Level command, valid in special modes only, causes the Memory Controller to set the margin level specified for future read operations of the P-Flash or EEPROM block.

Upon clearing CCIF to launch the Set Field Margin Level command, the Memory Controller will set the

Table 27-57. Set Field Margin Level Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x0E	Flash block selection code [1:0]. See Table 27-34
001	Margin level setting.	

field margin level for the targeted block and then set the CCIF flag.

NOTE

When the EEPROM block is targeted, the EEPROM field margin levels are applied only to the EEPROM reads. However, when the P-Flash block is targeted, the P-Flash field margin levels are applied to both P-Flash and EEPROM reads. It is not possible to apply field margin levels to the P-Flash block only.

Valid margin level settings for the Set Field Margin Level command are defined in Table 27-58.

Table 27-58. Valid Set Field Margin Level Settings

CCOB (CCOBIX=001)	Level Description
0x0000	Return to Normal Level
0x0001	User Margin-1 Level[1]
0x0002	User Margin-0 Level[2]
0x0003	Field Margin-1 Level[1]
0x0004	Field Margin-0 Level[2]

1 Read margin to the erased state

2 Read margin to the programmed state

Offset Module Base + 0x0013

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 28-25. Flash Reserved7 Register (FRSV7)

All bits in the FRSV7 register read 0 and are not writable.

28.4 Functional Description

28.4.1 Modes of Operation

The FTMRG96K1 module provides the modes of operation normal and special . The operating mode is determined by module-level inputs and affects the FCLKDIV, FCNFG, and EEPROT registers (see Table 28-27).

28.4.2 IFR Version ID Word

The version ID word is stored in the IFR at address 0x0_40B6. The contents of the word are defined in Table 28-26.

Table 28-26. IFR Version ID Fields

[15:4]	[3:0]
Reserved	VERNUM

28.4.6.3 Erase Verify P-Flash Section Command

The Erase Verify P-Flash Section command will verify that a section of code in the P-Flash memory is erased. The Erase Verify P-Flash Section command defines the starting point of the code to be verified and the number of phrases.

Table 28-36. Erase Verify P-Flash Section Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x03	Global address [17:16] of a P-Flash block
001	Global address [15:0] of the first phrase to be verified	
010	Number of phrases to be verified	

Upon clearing CCIF to launch the Erase Verify P-Flash Section command, the Memory Controller will verify the selected section of Flash memory is erased. The CCIF flag will set after the Erase Verify P-Flash Section operation has completed. If the section is not erased, it means blank check failed, both MGSTAT bits will be set.

Table 28-37. Erase Verify P-Flash Section Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 010 at command launch
		Set if command not available in current mode (see Table 28-27)
		Set if an invalid global address [17:0] is supplied see Table 28-3)[1]
		Set if a misaligned phrase address is supplied (global address [2:0] != 000)
		Set if the requested section crosses a the P-Flash address boundary
	FPVIOL	None
	MGSTAT1	Set if any errors have been encountered during the read[2] or if blank check failed.
	MGSTAT0	Set if any non-correctable errors have been encountered during the read[2] or if blank check failed.

1 As defined by the memory map for FTMRG96K1.

2 As found in the memory map for FTMRG96K1.

28.4.6.4 Read Once Command

The Read Once command provides read access to a reserved 64 byte field (8 phrases) located in the nonvolatile information register of P-Flash. The Read Once field is programmed using the Program Once command described in Section 28.4.6.6. The Read Once command must not be executed from the Flash block containing the Program Once reserved field to avoid code runaway.

Table 28-38. Read Once Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x04	Not Required

Address & Name		7	6	5	4	3	2	1	0
0x000A FCCOBHI	R	CCOB15	CCOB14	CCOB13	CCOB12	CCOB11	CCOB10	CCOB9	CCOB8
	W								
0x000B FCCOBLO	R	CCOB7	CCOB6	CCOB5	CCOB4	CCOB3	CCOB2	CCOB1	CCOB0
	W								
0x000C FRSV1	R	0	0	0	0	0	0	0	0
	W								
0x000D FRSV2	R	0	0	0	0	0	0	0	0
	W								
0x000E FRSV3	R	0	0	0	0	0	0	0	0
	W								
0x000F FRSV4	R	0	0	0	0	0	0	0	0
	W								
0x0010 FOPT	R	NV7	NV6	NV5	NV4	NV3	NV2	NV1	NV0
	W								
0x0011 FRSV5	R	0	0	0	0	0	0	0	0
	W								
0x0012 FRSV6	R	0	0	0	0	0	0	0	0
	W								
0x0013 FRSV7	R	0	0	0	0	0	0	0	0
	W								

= Unimplemented or Reserved

Figure 30-4. FTMRG192K2 Register Summary (continued)

30.3.2.1 Flash Clock Divider Register (FCLKDIV)

The FCLKDIV register is used to control timed events in program and erase algorithms.

Table 30-25. FOPT Field Descriptions

Field	Description
7–0 NV[7:0]	**Nonvolatile Bits** — The NV[7:0] bits are available as nonvolatile bits. Refer to the device user guide for proper use of the NV bits.

30.3.2.17 Flash Reserved5 Register (FRSV5)

This Flash register is reserved for factory testing.

Offset Module Base + 0x0011

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 30-23. Flash Reserved5 Register (FRSV5)

All bits in the FRSV5 register read 0 and are not writable.

30.3.2.18 Flash Reserved6 Register (FRSV6)

This Flash register is reserved for factory testing.

Offset Module Base + 0x0012

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 30-24. Flash Reserved6 Register (FRSV6)

All bits in the FRSV6 register read 0 and are not writable.

30.3.2.19 Flash Reserved7 Register (FRSV7)

This Flash register is reserved for factory testing.

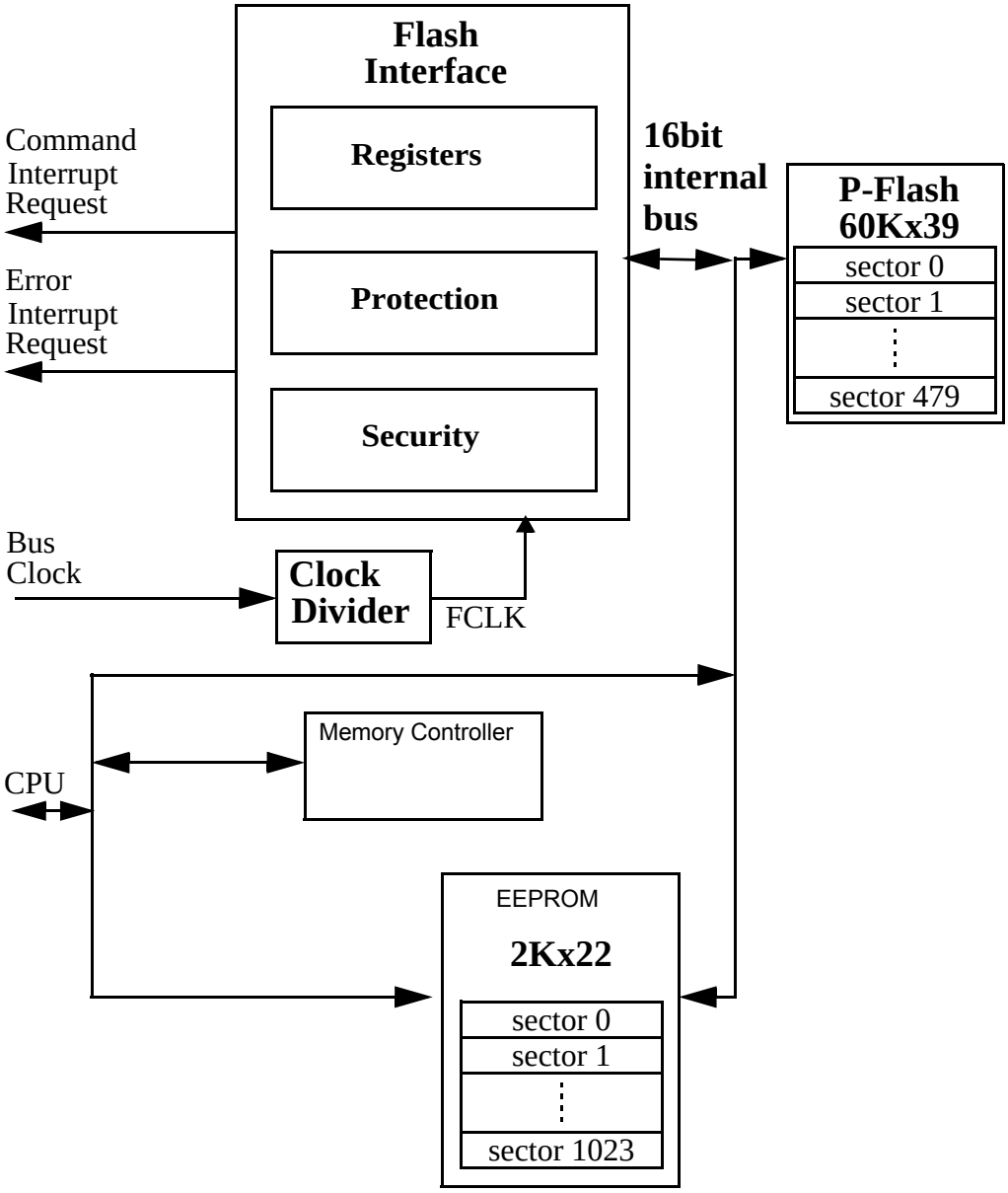


Figure 31-1. FTMRG240K2 Block Diagram

31.2 External Signal Description

The Flash module contains no signals that connect off-chip.

Table 31-57. Set Field Margin Level Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x0E	Flash block selection code [1:0]. See Table 31-34
001	Margin level setting.	

Upon clearing CCIF to launch the Set Field Margin Level command, the Memory Controller will set the field margin level for the targeted block and then set the CCIF flag.

NOTE

When the EEPROM block is targeted, the EEPROM field margin levels are applied only to the EEPROM reads. However, when the P-Flash block is targeted, the P-Flash field margin levels are applied to both P-Flash and EEPROM reads. It is not possible to apply field margin levels to the P-Flash block only.

Valid margin level settings for the Set Field Margin Level command are defined in Table 31-58.

Table 31-58. Valid Set Field Margin Level Settings

CCOB (CCOBIX=001)	Level Description
0x0000	Return to Normal Level
0x0001	User Margin-1 Level[1]
0x0002	User Margin-0 Level[2]
0x0003	Field Margin-1 Level[1]
0x0004	Field Margin-0 Level[2]

1 Read margin to the erased state

2 Read margin to the programmed state

Table 31-59. Set Field Margin Level Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 001 at command launch.
		Set if command not available in current mode (see Table 31-27).
		Set if an invalid margin level setting is supplied.
	FPVIOL	None
	MGSTAT1	None
	MGSTAT0	None

1 The values for thermal resistance are achieved by package simulations

2 Per JEDEC JESD51-2 with the single layer board (JESD51-3) horizontal.J

3 Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.

4 .Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured in simulation on the top surface of the board near the package.

5 Thermal resistance between the die and the case top surface as measured in simulation by the cold plate method (MIL SPEC-883 Method 1012.1).

6 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. Ψ_{JT} is a useful value to use to estimate junction temperature in a steady state customer enviroment.

A.2 I/O Characteristics

This section describes the characteristics of all I/O pins except EXTAL, XTAL, TEST, and supply pins.

Table A-6. 3.3-V I/O Characteristics (Junction Temperature From –40°C To +150°C)

Conditions are 3.15 V < V_{DD35} < 3.6 V junction temperature from –40°C to +150°C, unless otherwise noted I/O Characteristics for all I/O pins except EXTAL, XTAL,TEST and supply pins.							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	P	Input high voltage	V_{IH}	0.65*V_{DD35}	—	—	V
2	T	Input high voltage	V_{IH}	—	—	V_{DD35}+0.3	V
3	P	Input low voltage	V_{IL}	—	—	0.35*V_{DD35}	V
4	T	Input low voltage	V_{IL}	V_{SS35} – 0.3	—	—	V
5	C	Input hysteresis	V_{HYS}	0.06*V_{DD35}	—	0.3*V_{DD35}	mV
6	P	Input leakage current (pins in high impedance input mode)[1] V_{in} = V_{DD35} or V_{SS35} +125°C to < T_J < 150°C +105°C to < T_J < 125° –40°C to < T_J < 105°C	I_{in}	 -1 -0.5 -0.4	 — — —	 1 0.5 0.4	µA
7	P	Output high voltage (pins in output mode) I_{OH} = –1.75 mA	V_{OH}	V_{DD35}-0.4	—	—	V
8	C	Output low voltage (pins in output mode) I_{OL} = +1.75 mA	V_{OL}	—	—	0.4	V
9	P	Internal pull up device current V_{IH} min > input voltage > V_{IL} max	I_{PUL}	-1	—	–70	µA
10	P	Internal pull down device current V_{IH} min > input voltage > V_{IL} max	I_{PDH}	1	—	70	µA
11	D	Input capacitance	C_{in}	—	7	—	pF
12	T	Injection current[2] Single pin limit Total device limit, sum of all injected currents	 I_{ICS} I_{ICP}	 –2.5 –25	—	 2.5 25	mA

1 Maximum leakage current occurs at maximum operating temperature. Current decreases by approximately one-half for each 8°°C to 12°C° in the temperature range from 50°C to 125°C.

2 Refer to Section A.1.4, “Current Injection” for more details

0x0020–0x002F Debug Module (DBG)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0029	DBGXAH	R	0	0	0	0	0	0	Bit 17	Bit 16
		W								
0x002A	DBGXAM	R	Bit 15	14	13	12	11	10	9	Bit 8
		W								
0x002B	DBGXAL	R	Bit 7	6	5	4	3	2	1	Bit 0
		W								
0x002C	DBGADH	R	Bit 15	14	13	12	11	10	9	Bit 8
		W								
0x002D	DBGADL	R	Bit 7	6	5	4	3	2	1	Bit 0
		W								
0x002E	DBGADHM	R	Bit 15	14	13	12	11	10	9	Bit 8
		W								
0x002F	DBGADLM	R	Bit 7	6	5	4	3	2	1	Bit 0
		W								

0x0030–0x033 Reserved

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0030-0x0033	Reserved	R	0	0	0	0	0	0	0	0
		W								

0x0034–0x003F Clock and Power Management (CPMU) Map 1 of 2

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0034	CPMU SYNR	R	VCOFRQ[1:0]		SYNDIV[5:0]					
		W								
0x0035	CPMU REFDIV	R	REFFRQ[1:0]		0	0	REFDIV[3:0]			
		W								
0x0036	CPMU POSTDIV	R	0	0	0	POSTDIV[4:0]				
		W								
0x0037	CPMUFLG	R	RTIF	PORF	LVRF	LOCKIF	LOCK	ILAF	OSCIF	UPOSC
		W								
0x0038	CPMUINT	R	RTIE	0	0	LOCKIE	0	0	OSCIE	0
		W								
0x0039	CPMUCLKS	R	PLLSEL	PSTP	0	0	PRE	PCE	RTI OSCSEL	COP OSCSEL
		W								
0x003A	CPMUPLL	R	0	0	FM1	FM0	0	0	0	0
		W								
0x003B	CPMURTI	R	RTDEC	RTR6	RTR5	RTR4	RTR3	RTR2	RTR1	RTR0
		W								
0x003C	CPMUCOP	R	WCOP	RSBCK	0	0	0	CR2	CR1	CR0
		W			WRTMASK					