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Details

Product Status	Active
Core Processor	12V1
Core Size	16-Bit
Speed	25MHz
Connectivity	CANbus, IrDA, LINbus, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	40
Program Memory Size	240KB (240K × 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	11K x 8
Voltage - Supply (Vcc/Vdd)	3.13V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
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2.4.3.1 Port A Data Register (PORTA)



¹ Read: Anytime. The data source is depending on the data direction value. Write: Anytime

Table 2-22. PORTA Register Field Descriptions

Field	Description
7-0 PA	Port A general-purpose input/output data —Data Register The associated pin can be used as general-purpose I/O. In general-purpose output mode the port data register bit value is driven to the pin
	If the associated data direction bit is set to 1, a read returns the value of the port data register bit, otherwise the buffered pin input state is read.

2.4.3.2 Port B Data Register (PORTB)



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2.4.3.43 Port J Input Register (PTIJ)



Write:Never

Table 2-69. PTIJ Register Field Descriptions

Field	Description
7-0	Port J input data —
PTIJ	A read always returns the buffered input state of the associated pin. It can be used to detect overload or short circuit conditions on output pins.

2.4.3.44 Port J Data Direction Register (DDRJ)

Address ()x026A (<mark>G1</mark> , (G2)			1		Access: Us	ser read/write ¹
_	7	6	5	4	3	2	1	0
R W	DDRJ7	DDRJ6	DDRJ5	DDRJ4	DDRJ3	DDRJ2	DDRJ1	DDRJ0
Reset	0	0	0	0	0	0	0	0
Address (0x026A (<mark>G3</mark>)						Access: Us	ser read/write ¹
	7	6	5	4	3	2	1	0
R	0	0	0	0	DDRJ3	DDRJ2	DDRJ1	DDRJ0
W								
Reset	0	0	0	0	0	0	0	0
4		Figu	re 2-44. Port	J Data Direc	tion Registe	r (DDRJ)		

¹ Read: Anytime Write: Anytime handshake protocol is enabled, the time out between a read command and the data retrieval is disabled. Therefore, the host could wait for more then 512 serial clock cycles and still be able to retrieve the data from an issued read command. However, once the handshake pulse (ACK pulse) is issued, the time-out feature is re-activated, meaning that the target will time out after 512 clock cycles. Therefore, the host needs to retrieve the data within a 512 serial clock cycles time frame after the ACK pulse had been issued. After that period, the read command is discarded and the data is no longer available for retrieval. Any negative edge in the BKGD pin after the time-out period is considered to be a new command or a SYNC request.

Note that whenever a partially issued command, or partially retrieved data, has occurred the time out in the serial communication is active. This means that if a time frame higher than 512 serial clock cycles is observed between two consecutive negative edges and the command being issued or data being retrieved is not complete, a soft-reset will occur causing the partially received command or data retrieved to be disregarded. The next negative edge in the BKGD pin, after a soft-reset has occurred, is considered by the target as the start of a new BDM command, or the start of a SYNC request pulse.

0	1	1	Start Trace Buffer at trigger A breakpoint request occurs when Trace Buffer is full
1	x	1	Terminate tracing and generate breakpoint immediately on trigger
1	x	0	Terminate tracing immediately on trigger

Table 8-42. Breakpoint Setup For CPU Breakpoints

8.4.7.2 Breakpoints Generated Via The TRIG Bit

If a TRIG triggers occur, the Final State is entered whereby tracing trigger alignment is defined by the TALIGN bit. If a tracing session is selected by the TSOURCE bit, breakpoints are requested when the tracing session has completed, thus if Begin aligned triggering is selected, the breakpoint is requested only on completion of the subsequent trace (see Table 8-42). If no tracing session is selected, breakpoints are requested immediately. TRIG breakpoints are possible with a single write to DBGC1, setting ARM and TRIG simultaneously.

8.4.7.3 Breakpoint Priorities

If a TRIG trigger occurs after Begin aligned tracing has already started, then the TRIG no longer has an effect. When the associated tracing session is complete, the breakpoint occurs. Similarly if a TRIG is followed by a subsequent comparator channel match, it has no effect, since tracing has already started.

If a forced SWI breakpoint coincides with a BGND in user code with BDM enabled, then the BDM is activated by the BGND and the breakpoint to SWI is suppressed.

8.4.7.3.1 DBG Breakpoint Priorities And BDM Interfacing

Breakpoint operation is dependent on the state of the BDM module. If the BDM module is active, the CPU is executing out of BDM firmware, thus comparator matches and associated breakpoints are disabled. In addition, while executing a BDM TRACE command, tagging into BDM is disabled. If BDM is not active, the breakpoint gives priority to BDM requests over SWI requests if the breakpoint happens to coincide with a SWI instruction in user code. On returning from BDM, the SWI from user code gets executed.

DBGBRK	BDM Bit (DBGC1[4])	BDM Enabled	BDM Active	Breakpoint Mapping
0	Х	Х	Х	No Breakpoint
1	0	Х	0	Breakpoint to SWI
Х	Х	1	1	No Breakpoint
1	1	0	Х	Breakpoint to SWI
1	1	1	0	Breakpoint to BDM

BDM cannot be entered from a breakpoint unless the ENABLE bit is set in the BDM. If entry to BDM via a BGND instruction is attempted and the ENABLE bit in the BDM is cleared, the CPU actually executes the BDM firmware code, checks the ENABLE and returns if ENABLE is not set. If not serviced by the monitor then the breakpoint is re-asserted when the BDM returns to normal CPU flow.

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to erase the EEPROM and Flash memory without giving access to their contents. After erasing both Flash memory and EEPROM, another reset into special single chip mode will cause the blank check to succeed and the options/security byte can be programmed to "unsecured" state via BDM.

While the BDM is executing the blank check, the BDM interface is completely blocked, which means that all BDM commands are temporarily blocked.

9.1.5 Unsecuring the Microcontroller

Unsecuring the microcontroller can be done by three different methods:

- 1. Backdoor key access
- 2. Reprogramming the security bits
- 3. Complete memory erase (special modes)

9.1.5.1 Unsecuring the MCU Using the Backdoor Key Access

In normal modes (single chip and expanded), security can be temporarily disabled using the backdoor key access method. This method requires that:

- The backdoor key at 0xFF00–0xFF07 (= global addresses 0x3_FF00–0x3_FF07) has been programmed to a valid value.
- The KEYEN[1:0] bits within the Flash options/security byte select 'enabled'.
- In single chip mode, the application program programmed into the microcontroller must be designed to have the capability to write to the backdoor key locations.

The backdoor key values themselves would not normally be stored within the application data, which means the application program would have to be designed to receive the backdoor key values from an external source (e.g. through a serial port).

The backdoor key access method allows debugging of a secured microcontroller without having to erase the Flash. This is particularly useful for failure analysis.

NOTE

No word of the backdoor key is allowed to have the value 0x0000 or 0xFFFF.

9.1.6 Reprogramming the Security Bits

In normal single chip mode (NS), security can also be disabled by erasing and reprogramming the security bits within Flash options/security byte to the unsecured value. Because the erase operation will erase the entire sector from 0xFE00–0xFFFF (0x7F_FE00–0x7F_FFFF), the backdoor key and the interrupt vectors will also be erased; this method is not recommended for normal single chip mode. The application software can only erase and program the Flash options/security byte if the Flash sector containing the Flash options/security byte is not protected (see Flash protection). Thus Flash protection is a useful means of preventing this method. The microcontroller will enter the unsecured state after the next reset following the programming of the security bits to the unsecured value.

SC	CD	сс	СВ	СА	Analog Input Channel
1	0	0	0	0	Internal_6,
	0	0	0	1	Internal_7
	0	0	1	0	Internal_0
	0	0	1	1	Internal_1
	0	1	0	0	VRH
	0	1	0	1	VRL
	0	1	1	0	(VRH+VRL) / 2
	0	1	1	1	Reserved
	1	0	0	0	Internal_2
	1	0	0	1	Internal_3
	1	0	1	0	Internal_4
	1	0	1	1	Internal_5
	1	1	Х	Х	Reserved

Table 14-15. Analog Inpu	Channel Select Coding
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15.3.2.12 ATD Conversion Result Registers (ATDDR*n*)

The A/D conversion results are stored in 16 result registers. Results are always in unsigned data representation. Left and right justification is selected using the DJM control bit in ATDCTL3.

If automatic compare of conversions results is enabled (CMPE[n]=1 in ATDCMPE), these registers must be written with the compare values in left or right justified format depending on the actual value of the DJM bit. In this case, as the ATDDRn register is used to hold the compare value, the result will not be stored there at the end of the conversion but is lost.

Attention, n is the conversion number, NOT the channel number!

Read: Anytime

Write: Anytime

NOTE

For conversions not using automatic compare, results are stored in the result registers after each conversion. In this case avoid writing to ATDDRn except for initial values, because an A/D result might be overwritten.

15.3.2.12.1 Left Justified Result Data (DJM=0)

```
Module Base +
```

```
0x0010 = ATDDR0, 0x0012 = ATDDR1, 0x0014 = ATDDR2, 0x0016 = ATDDR3
0x0018 = ATDDR4, 0x001A = ATDDR5, 0x001C = ATDDR6, 0x001E = ATDDR7
0x0020 = ATDDR8, 0x0022 = ATDDR9, 0x0024 = ATDDR10, 0x0026 = ATDDR11
0x0028 = ATDDR12, 0x002A = ATDDR13, 0x002C = ATDDR14, 0x002E = ATDDR15
```



Figure 15-14. Left justified ATD conversion result register (ATDDRn)

Table 15-21 shows how depending on the A/D resolution the conversion result is transferred to the ATD result registers for left justified data. Compare is always done using all 12 bits of both the conversion result and the compare value in ATDDRn.

A/D resolution	DJM	conversion result mapping to ATDDR <i>n</i>
8-bit data	0	Result-Bit[11:4] = conversion result, Result-Bit[3:0]=0000
10-bit data	0	Result-Bit[11:2] = conversion result, Result-Bit[1:0]=00



Figure 18-45. Initialization Request/Acknowledge Cycle

Due to independent clock domains within the MSCAN, INITRQ must be synchronized to all domains by using a special handshake mechanism. This handshake causes additional synchronization delay (see Figure 18-45).

If there is no message transfer ongoing on the CAN bus, the minimum delay will be two additional bus clocks and three additional CAN clocks. When all parts of the MSCAN are in initialization mode, the INITAK flag is set. The application software must use INITAK as a handshake indication for the request (INITRQ) to go into initialization mode.

NOTE

The CPU cannot clear INITRQ before initialization mode (INITRQ = 1 and INITAK = 1) is active.

18.4.5 Low-Power Options

If the MSCAN is disabled (CANE = 0), the MSCAN clocks are stopped for power saving.

If the MSCAN is enabled (CANE = 1), the MSCAN has two additional modes with reduced power consumption, compared to normal mode: sleep and power down mode. In sleep mode, power consumption is reduced by stopping all clocks except those to access the registers from the CPU side. In power down mode, all clocks are stopped and no power is consumed.

Table 18-38 summarizes the combinations of MSCAN and CPU modes. A particular combination of modes is entered by the given settings on the CSWAI and SLPRQ/SLPAK bits.

Table 20-4	. SCICR1	Field	Descriptions
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Field	Description
7 LOOPS	 Loop Select Bit — LOOPS enables loop operation. In loop operation, the RXD pin is disconnected from the SCI and the transmitter output is internally connected to the receiver input. Both the transmitter and the receiver must be enabled to use the loop function. 0 Normal operation enabled 1 Loop operation enabled The receiver input is determined by the RSRC bit.
6 SCISWAI	 SCI Stop in Wait Mode Bit — SCISWAI disables the SCI in wait mode. SCI enabled in wait mode SCI disabled in wait mode
5 RSRC	 Receiver Source Bit — When LOOPS = 1, the RSRC bit determines the source for the receiver shift register input. See Table 20-5. 0 Receiver input internally connected to transmitter output 1 Receiver input connected externally to transmitter
4 M	 Data Format Mode Bit — MODE determines whether data characters are eight or nine bits long. 0 One start bit, eight data bits, one stop bit 1 One start bit, nine data bits, one stop bit
3 WAKE	 Wakeup Condition Bit — WAKE determines which condition wakes up the SCI: a logic 1 (address mark) in the most significant bit position of a received data character or an idle condition on the RXD pin. Idle line wakeup Address mark wakeup
2 ILT	 Idle Line Type Bit — ILT determines when the receiver starts counting logic 1s as idle character bits. The counting begins either after the start bit or after the stop bit. If the count begins after the start bit, then a string of logic 1s preceding the stop bit may cause false recognition of an idle character. Beginning the count after the stop bit avoids false idle character recognition, but requires properly synchronized transmissions. Idle character bit count begins after stop bit
1 PE	 Parity Enable Bit — PE enables the parity function. When enabled, the parity function inserts a parity bit in the most significant bit position. 0 Parity function disabled 1 Parity function enabled
0 PT	 Parity Type Bit — PT determines whether the SCI generates and checks for even parity or odd parity. With even parity, an even number of 1s clears the parity bit and an odd number of 1s sets the parity bit. With odd parity, an odd number of 1s clears the parity bit and an even number of 1s sets the parity bit. 0 Even parity 1 Odd parity

Table 20-5. Loop Functions

LOOPS	RSRC	Function
0	х	Normal operation
1	0	Loop mode with transmitter output internally connected to receiver input
1	1	Single-wire mode with TXD pin connected to receiver input

23.3.2.18 Output Compare Pin Disconnect Register(OCPD)

Module Base + 0x002C



Figure 23-28. Output Compare Pin Disconnect Register (OCPD)

Read: Anytime

Write: Anytime

All bits reset to zero.

Table 23-22. OCPD Field Description

Note: Writing to unavailable bits has no effect. Reading from unavailable bits return a zero.

Field	Description
7:0 OCPD[7:0]	 Output Compare Pin Disconnect Bits Enables the timer channel port. Output Compare action will occur on the channel pin. These bits do not affect the input capture or pulse accumulator functions. Disables the timer channel port. Output Compare action will not occur on the channel pin, but the output compare flag still become set.

23.3.2.19 Precision Timer Prescaler Select Register (PTPSR)

Module Base + 0x002E

	7	6	5	4	3	2	1	0
R W	PTPS7	PTPS6	PTPS5	PTPS4	PTPS3	PTPS2	PTPS1	PTPS0
Reset	0	0	0	0	0	0	0	0

Figure 23-29. Precision Timer Prescaler Select Register (PTPSR)

Read: Anytime

Write: Anytime

All bits reset to zero.

24.3 Memory Map and Registers

This section describes the memory map and registers for the Flash module. Read data from unimplemented memory space in the Flash module is undefined. Write access to unimplemented or reserved memory space in the Flash module will be ignored by the Flash module.

CAUTION

Writing to the Flash registers while a Flash command is executing (that is indicated when the value of flag CCIF reads as '0') is not allowed. If such action is attempted the write operation will not change the register value.

Writing to the Flash registers is allowed when the Flash is not busy executing commands (CCIF = 1) and during initialization right after reset, despite the value of flag CCIF in that case (refer to Section 24.6 for a complete description of the reset sequence).

Global Address (in Bytes)	Size (Bytes)	Description
0x0_0000 - 0x0_03FF	1,024	Register Space
0x0_0400 – 0x0_05FF	512	EEPROM Memory
0x0_0600 – 0x0_07FF	512	FTMRG reserved area
0x0_4000 – 0x0_7FFF	16,284	NVMRES ¹ =1 : NVM Resource area (see Figure 24-3)
0x3_8000 – 0x3_BFFF	16,384	FTMRG reserved area
0x3_C000 - 0x3_FFFF	16,384	P-Flash Memory

Table 24-2. FTMRG Memory Map

¹ See NVMRES description in Section 24.4.3

24.3.1 Module Memory Map

The S12 architecture places the P-Flash memory between global addresses 0x3_C000 and 0x3_FFFF as shown in Table 24-3. The P-Flash memory map is shown in Figure 24-2.

Table 24-3. P-Flash	Memory	Addressing
---------------------	--------	------------

Global Address	Size (Bytes)	Description
0x3_C000 – 0x3_FFFF	16 K	P-Flash Block Contains Flash Configuration Field (see Table 24-4)

NOTE

Programming or erasing the Flash memory cannot be performed if the bus clock runs at less than 0.8 MHz. Setting FDIV too high can destroy the Flash memory due to overstress. Setting FDIV too low can result in incomplete programming or erasure of the Flash memory cells.

When the FCLKDIV register is written, the FDIVLD bit is set automatically. If the FDIVLD bit is 0, the FCLKDIV register has not been written since the last reset. If the FCLKDIV register has not been written, any Flash program or erase command loaded during a command write sequence will not execute and the ACCERR bit in the FSTAT register will set.

24.4.4.2 Command Write Sequence

The Memory Controller will launch all valid Flash commands entered using a command write sequence.

Before launching a command, the ACCERR and FPVIOL bits in the FSTAT register must be clear (see Section 24.3.2.7) and the CCIF flag should be tested to determine the status of the current command write sequence. If CCIF is 0, the previous command write sequence is still active, a new command write sequence cannot be started, and all writes to the FCCOB register are ignored.

24.4.4.2.1 Define FCCOB Contents

The FCCOB parameter fields must be loaded with all required parameters for the Flash command being executed. Access to the FCCOB parameter fields is controlled via the CCOBIX bits in the FCCOBIX register (see Section 24.3.2.3).

The contents of the FCCOB parameter fields are transferred to the Memory Controller when the user clears the CCIF command completion flag in the FSTAT register (writing 1 clears the CCIF to 0). The CCIF flag will remain clear until the Flash command has completed. Upon completion, the Memory Controller will return CCIF to 1 and the FCCOB register will be used to communicate any results. The flow for a generic command write sequence is shown in Figure 24-25.

Register	Error Bit	Error Condition		
		Set if CCOBIX[2:0] < 010 at command launch		
		Set if CCOBIX[2:0] > 101 at command launch		
	ACCERR	Set if command not available in current mode (see Table 24-25)		
	ACCERR	Set if an invalid global address [17:0] is supplied		
FSTAT		Set if a misaligned word address is supplied (global address [0] != 0)		
_		Set if the requested group of words breaches the end of the EEPROM block		
	FPVIOL	Set if the selected area of the EEPROM memory is protected		
	MGSTAT1	Set if any errors have been encountered during the verify operation		
	MGSTAT0	Set if any non-correctable errors have been encountered during the verify operation		

Table 24-61. Program EEPROM Command Error Handling

24.4.6.16 Erase EEPROM Sector Command

The Erase EEPROM Sector operation will erase all addresses in a sector of the EEPROM block.

Table 24-62	. Erase EEP	ROM Sector	Command	FCCOB	Requirements
-------------	-------------	------------	---------	-------	--------------

CCOBIX[2:0]	FCCOB	Parameters
000	0x12	Global address [17:16] to identify EEPROM block
001	Global address [15:0] anywhere within the sector to be erased. See Section 24.1.2.2 for EEPROM sector size.	

Upon clearing CCIF to launch the Erase EEPROM Sector command, the Memory Controller will erase the selected Flash sector and verify that it is erased. The CCIF flag will set after the Erase EEPROM Sector operation has completed.

Register	Error Bit	Error Condition
		Set if CCOBIX[2:0] != 001 at command launch
	ACCERR	Set if command not available in current mode (see Table 24-25)
	ACCERR	Set if an invalid global address [17:0] is suppliedsee Table 24-3)
FSTAT		Set if a misaligned word address is supplied (global address [0] != 0)
	FPVIOL	Set if the selected area of the EEPROM memory is protected
	MGSTAT1	Set if any errors have been encountered during the verify operation
	MGSTAT0	Set if any non-correctable errors have been encountered during the verify operation

Table 24-63. Erase EEPROM Sector Command Error Handling

SEC[1:0]	Status of Security
00	SECURED
01	SECURED ¹
10	UNSECURED
11	SECURED

Table 25-11. Flash Security States

¹ Preferred SEC state to set MCU to secured state.

The security function in the Flash module is described in Section 25.5.

25.3.2.3 Flash CCOB Index Register (FCCOBIX)

The FCCOBIX register is used to index the FCCOB register for Flash memory operations.



CCOBIX bits are readable and writable while remaining bits read 0 and are not writable.

Table 25-12. FCCOBIX Field Descriptions

Field	Description
2–0 CCOBIX[1:0]	Common Command Register Index — The CCOBIX bits are used to select which word of the FCCOB register array is being read or written to. See 25.3.2.11 Flash Common Command Object Register (FCCOB)," for more
	details.

25.3.2.4 Flash Reserved0 Register (FRSV0)

This Flash register is reserved for factory testing.



Figure 25-8. Flash Reserved0 Register (FRSV0)

All bits in the FRSV0 register read 0 and are not writable.

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All assigned bits in the FERCNFG register are readable and writable.

Table 26-14. FERCNFG Field Descriptions

Field	Description
1 DFDIE	 Double Bit Fault Detect Interrupt Enable — The DFDIE bit controls interrupt generation when a double bit fault is detected during a Flash block read operation. 0 DFDIF interrupt disabled 1 An interrupt will be requested whenever the DFDIF flag is set (see Section 26.3.2.8)
0 SFDIE	 Single Bit Fault Detect Interrupt Enable — The SFDIE bit controls interrupt generation when a single bit fault is detected during a Flash block read operation. 0 SFDIF interrupt disabled whenever the SFDIF flag is set (see Section 26.3.2.8) 1 An interrupt will be requested whenever the SFDIF flag is set (see Section 26.3.2.8)

26.3.2.7 Flash Status Register (FSTAT)

The FSTAT register reports the operational status of the Flash module.

Offset Module Base + 0x0006



Figure 26-11. Flash Status Register (FSTAT)

¹ Reset value can deviate from the value shown if a double bit fault is detected during the reset sequence (see Section 26.6).

CCIF, ACCERR, and FPVIOL bits are readable and writable, MGBUSY and MGSTAT bits are readable but not writable, while remaining bits read 0 and are not writable.

27.4.6 Flash Command Description

This section provides details of all available Flash commands launched by a command write sequence. The ACCERR bit in the FSTAT register will be set during the command write sequence if any of the following illegal steps are performed, causing the command not to be processed by the Memory Controller:

- Starting any command write sequence that programs or erases Flash memory before initializing the FCLKDIV register
- Writing an invalid command as part of the command write sequence
- For additional possible errors, refer to the error handling table provided for each command

If a Flash block is read during execution of an algorithm (CCIF = 0) on that same block, the read operation will return invalid data if both flags SFDIF and DFDIF are set. If the SFDIF or DFDIF flags were not previously set when the invalid read operation occurred, both the SFDIF and DFDIF flags will be set.

If the ACCERR or FPVIOL bits are set in the FSTAT register, the user must clear these bits before starting any command write sequence (see Section 27.3.2.7).

CAUTION

A Flash word or phrase must be in the erased state before being programmed. Cumulative programming of bits within a Flash word or phrase is not allowed.

27.4.6.1 Erase Verify All Blocks Command

The Erase Verify All Blocks command will verify that all P-Flash and EEPROM blocks have been erased.

Table 27-31. Erase Verify All Blocks Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters		
000	0x01	Not required	

Upon clearing CCIF to launch the Erase Verify All Blocks command, the Memory Controller will verify that the entire Flash memory space is erased. The CCIF flag will set after the Erase Verify All Blocks operation has completed. If all blocks are not erased, it means blank check failed, both MGSTAT bits will be set.

 Table 27-32. Erase Verify All Blocks Command Error Handling

Register	Error Bit	Error Condition
	ACCERR	Set if CCOBIX[2:0] != 000 at command launch
	FPVIOL	None
FSTAT	MGSTAT1	Set if any errors have been encountered during the reador if blank check failed .
	MGSTAT0	Set if any non-correctable errors have been encountered during the read or if blank check failed.

28.3.2.11 Flash Common Command Object Register (FCCOB)

The FCCOB is an array of six words addressed via the CCOBIX index found in the FCCOBIX register. Byte wide reads and writes are allowed to the FCCOB register.



28.3.2.11.1 FCCOB - NVM Command Mode

NVM command mode uses the indexed FCCOB register to provide a command code and its relevant parameters to the Memory Controller. The user first sets up all required FCCOB fields and then initiates the command's execution by writing a 1 to the CCIF bit in the FSTAT register (a 1 written by the user clears the CCIF command completion flag to 0). When the user clears the CCIF bit in the FSTAT register all FCCOB parameter fields are locked and cannot be changed by the user until the command completes (as evidenced by the Memory Controller returning CCIF to 1). Some commands return information to the FCCOB register array.

The generic format for the FCCOB parameter fields in NVM command mode is shown in Table 28-24. The return values are available for reading after the CCIF flag in the FSTAT register has been returned to 1 by the Memory Controller. Writes to the unimplemented parameter fields (CCOBIX = 110 and CCOBIX = 111) are ignored with reads from these fields returning 0x0000.

Table 28-24 shows the generic Flash command format. The high byte of the first word in the CCOB array contains the command code, followed by the parameters for this specific Flash command. For details on the FCCOB settings required by each command, see the Flash command descriptions in Section 28.4.6.

CCOBIX[2:0]	Byte	FCCOB Parameter Fields (NVM Command Mode)	
000	HI	FCMD[7:0] defining Flash command	
000	LO	6'h0, Global address [17:16]	
001	HI	Global address [15:8]	
	LO	Global address [7:0]	

Table 28-24. FCCOB - NVM Command Mode (Typical Usage)

Register	Error Bit	Error Condition	
	ACCERR	Set if CCOBIX[2:0] != 001 at command launch	
		Set if command not available in current mode (see Table 28-27)	
		Set if an invalid FlashBlockSelectionCode[1:0] is supplied (See Table 28-34) ¹	
FSTAT		Set if an invalid margin level setting is supplied	
	FPVIOL	None	
	MGSTAT1	None	
	MGSTAT0	None	

Table 28-59. Set Field Margin Level Command Error Handling

¹ As defined by the memory map for FTMRG96K1.

CAUTION

Field margin levels must only be used during verify of the initial factory programming.

NOTE

Field margin levels can be used to check that Flash memory contents have adequate margin for data retention at the normal level setting. If unexpected results are encountered when checking Flash memory contents at field margin levels, the Flash memory contents should be erased and reprogrammed.

28.4.6.14 Erase Verify EEPROM Section Command

The Erase Verify EEPROM Section command will verify that a section of code in the EEPROM is erased. The Erase Verify EEPROM Section command defines the starting point of the data to be verified and the number of words.

CCOBIX[2:0]	FCCOB Parameters		
000	0x10	Global address [17:16] to identify the EEPROM block	
001	Global address [15:0] of the first word to be verified		
010	Number of words to be verified		

Table 28-60. Erase Verify EEPROM Section Command FCCOB Requirements

Upon clearing CCIF to launch the Erase Verify EEPROM Section command, the Memory Controller will verify the selected section of EEPROM memory is erased. The CCIF flag will set after the Erase Verify EEPROM Section operation has completed. If the section is not erased, it means blank check failed, both MGSTAT bits will be set.

28.4.8 Wait Mode

The Flash module is not affected if the MCU enters wait mode. The Flash module can recover the MCU from wait via the CCIF interrupt (see Section 28.4.7, "Interrupts").

28.4.9 Stop Mode

If a Flash command is active (CCIF = 0) when the MCU requests stop mode, the current Flash operation will be completed before the MCU is allowed to enter stop mode.

28.5 Security

The Flash module provides security information to the MCU. The Flash security state is defined by the SEC bits of the FSEC register (see Table 28-11). During reset, the Flash module initializes the FSEC register using data read from the security byte of the Flash configuration field at global address 0x3_FF0F. The security state out of reset can be permanently changed by programming the security byte assuming that the MCU is starting from a mode where the necessary P-Flash erase and program commands are available and that the upper region of the P-Flash is unprotected. If the Flash security byte is successfully programmed, its new value will take affect after the next MCU reset.

The following subsections describe these security-related subjects:

- Unsecuring the MCU using Backdoor Key Access
- Unsecuring the MCU in Special Single Chip Mode using BDM
- Mode and Security Effects on Flash Command Availability

28.5.1 Unsecuring the MCU using Backdoor Key Access

The MCU may be unsecured by using the backdoor key access feature which requires knowledge of the contents of the backdoor keys (four 16-bit words programmed at addresses 0x3_FF00-0x3_FF07). If the KEYEN[1:0] bits are in the enabled state (see Section 28.3.2.2), the Verify Backdoor Access Key command (see Section 28.4.6.11) allows the user to present four prospective keys for comparison to the keys stored in the Flash memory via the Memory Controller. If the keys presented in the Verify Backdoor Access Key command match the backdoor keys stored in the Flash memory, the SEC bits in the FSEC register (see Table 28-11) will be changed to unsecure the MCU. Key values of 0x0000 and 0xFFFF are not permitted as backdoor keys. While the Verify Backdoor Access Key command is active, P-Flash memory and EEPROM memory will not be available for read access and will return invalid data.

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Upon clearing CCIF to launch the Read Once command, a Read Once phrase is fetched and stored in the FCCOB indexed register. The CCIF flag will set after the Read Once operation has completed. Valid phrase index values for the Read Once command range from 0x0000 to 0x0007. During execution of the Read Once command, any attempt to read addresses within P-Flash block will return invalid data.

Register	Error Bit	Error Condition	
	ACCERR	Set if CCOBIX[2:0] != 001 at command launch	
		Set if command not available in current mode (see Table 30-27)	
ESTAT		Set if an invalid phrase index is supplied	
FSTAI	FPVIOL	None	
	MGSTAT1	Set if any errors have been encountered during the read	
	MGSTAT0	Set if any non-correctable errors have been encountered during the read	

Table 30-39	. Read	Once	Command	Error	Handling
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30.4.6.5 Program P-Flash Command

The Program P-Flash operation will program a previously erased phrase in the P-Flash memory using an embedded algorithm.

CAUTION

A P-Flash phrase must be in the erased state before being programmed. Cumulative programming of bits within a Flash phrase is not allowed.

 Table 30-40. Program P-Flash Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters		
000	0x06	Global address [17:16] to identify P-Flash block	
001	Global address [15:0] of phrase location to be programmed ¹		
010	Word 0 program value		
011	Word 1 program value		
100	Word 2 program value		
101	Word 3 program value		

Global address [2:0] must be 000

Upon clearing CCIF to launch the Program P-Flash command, the Memory Controller will program the data words to the supplied global address and will then proceed to verify the data words read back as expected. The CCIF flag will set after the Program P-Flash operation has completed.