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Details

Product Status	Active
Core Processor	12V1
Core Size	16-Bit
Speed	25MHz
Connectivity	CANbus, IrDA, LINbus, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	26
Program Memory Size	48KB (48K x 8)
Program Memory Type	FLASH
EEPROM Size	1.5K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3.13V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s9s12g48f1clc

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Table 1-21. 64-Pin LQFP Pinout for S12G96 and S12G128

Package Pin	Function <----lowest----PRIORITY----highest---->					Power Supply	Internal Pull Resistor	
	Pin	2nd Func.	3rd Func.	4th Func	5th Func		CTRL	Reset State
57	PS5	MOSI0	—	—	—	V _{DDX}	PERS/PPSS	Up
58	PS6	SCK0	—	—	—	V _{DDX}	PERS/PPSS	Up
59	PS7	API_EXTC LK	ECLK	$\overline{SS0}$	—	V _{DDX}	PERS/PPSS	Up
60	PM0	RXCAN	—	—	—	V _{DDX}	PERM/PPSM	Disabled
61	PM1	TXCAN	—	—	—	V _{DDX}	PERM/PPSM	Disabled
62	PM2	RXD2	—	—	—	V _{DDX}	PERM/PPSM	Disabled
63	PM3	TXD2	—	—	—	V _{DDX}	PERM/PPSM	Disabled
64	PJ7	KWJ7	$\overline{SS2}$	—	—	V _{DDX}	PERJ/PPSJ	Up

¹ The regular I/O characteristics (see [Section A.2, “I/O Characteristics”](#)) apply if the EXTAL/XTAL function is disabled

1.8.9.3 Pinout 100-Pin LQFP

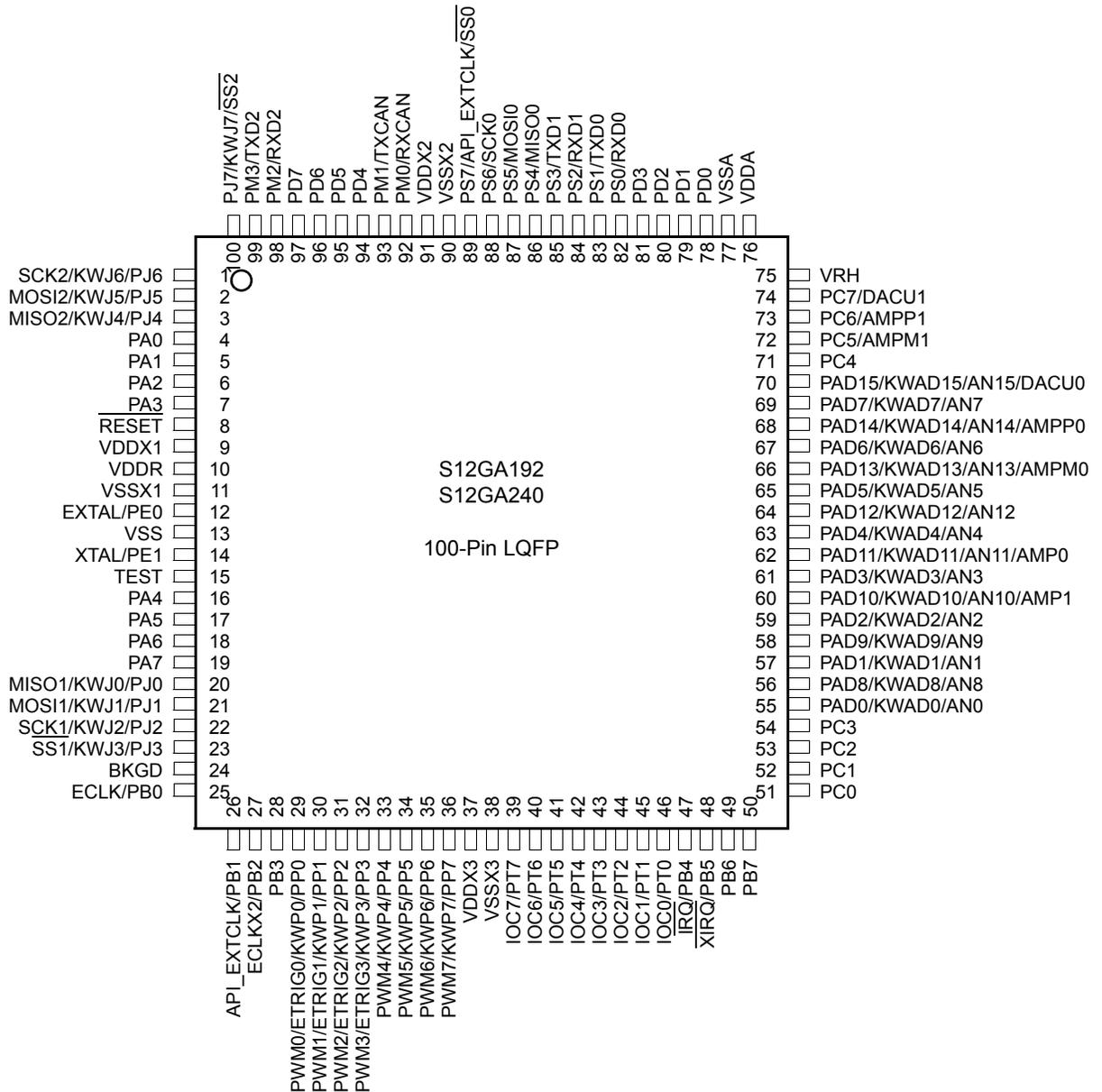


Figure 1-26. 100-Pin LQFP Pinout for S12GA192 and S12GA240

Table 2-76. PT1AD Register Field Descriptions

Field	Description
7-0 PT1AD	Port AD general-purpose input/output data—Data Register When not used with an alternative signal, the associated pin can be used as general-purpose I/O. In general-purpose output mode the port data register bit value is driven to the pin. If the associated data direction bit is set to 1, a read returns the value of the port data register bit, otherwise the buffered pin input state is read if the digital input buffers are enabled (Section 2.3.12, “Pins AD15-0”).

2.4.3.51 Port AD Input Register (PTI0AD)

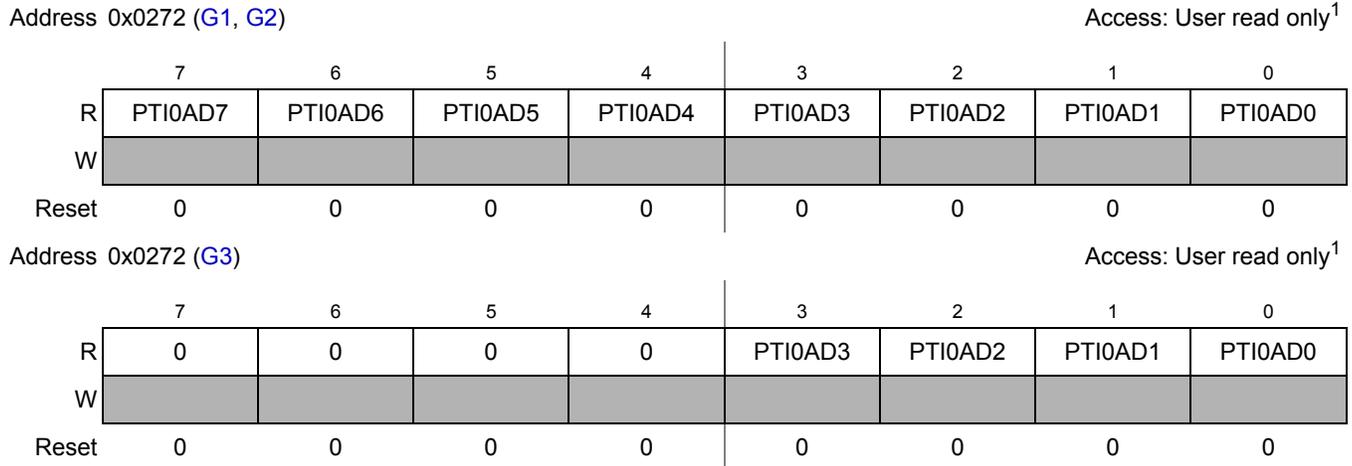


Figure 2-51. Port AD Input Register (PTI0AD)

¹ Read: Anytime
Write: Never

Table 2-77. PTI0AD Register Field Descriptions

Field	Description
7-0 PTI0AD	Port AD input data— A read always returns the buffered input state of the associated pin. It can be used to detect overload or short circuit conditions on output pins.

2.4.3.52 Port AD Input Register (PTI1AD)

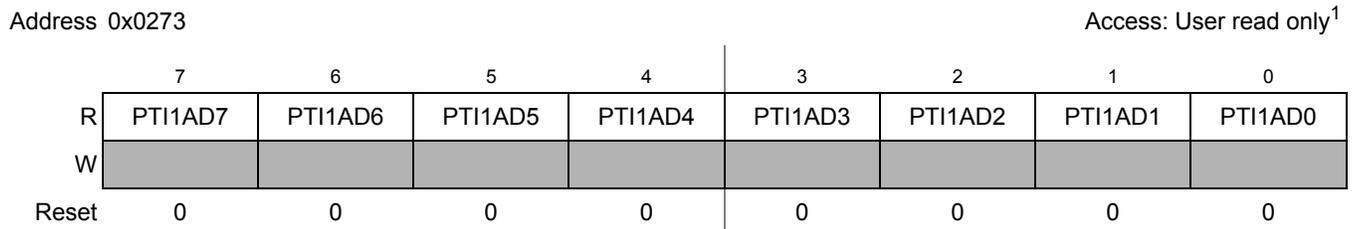


Figure 2-52. Port AD Input Register (PTI1AD)

¹ Read: Anytime
Write: Never

Table 2-80. DDR1AD Register Field Descriptions

Field	Description
7-0 DDR1AD	<p>Port AD data direction— This bit determines whether the associated pin is an input or output.</p> <p>1 Associated pin configured as output 0 Associated pin configured as input</p>

2.4.3.55 Reserved Register

NOTE

Address 0x0276 is reserved for RVA on G(A)240 and G(A)192 only. Refer to RVA section “RVA Control Register (RVACTL)”.

2.4.3.56 Pin Routing Register 1 (PRR1)

NOTE

Routing takes only effect if PKGCR is set to select the 100 LQFP package.

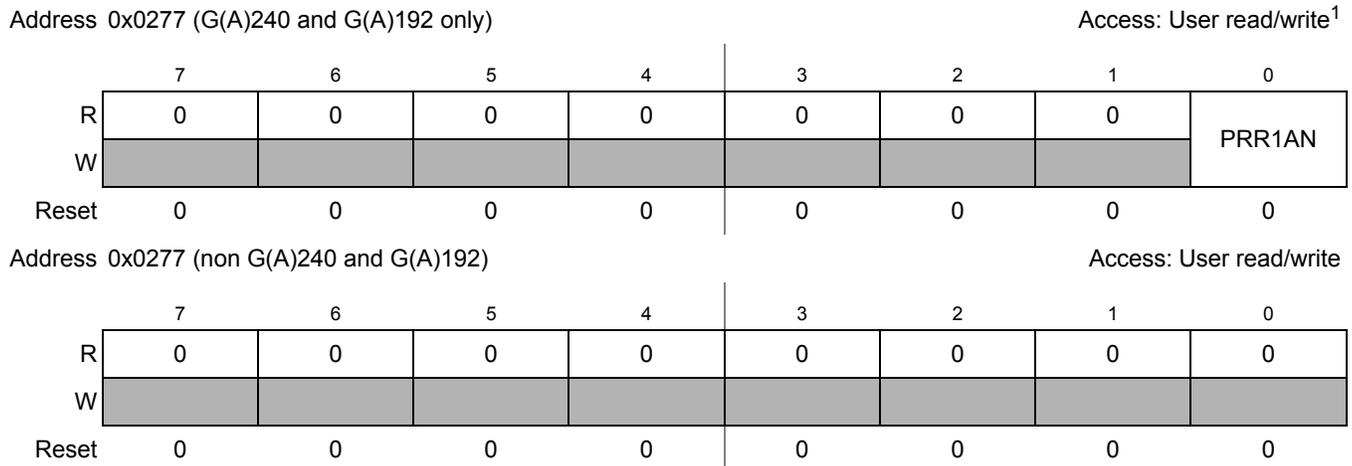


Figure 2-55. Pin Routing Register (PRR1)

¹ Read: Anytime
Write: Anytime

Table 2-81. PRR1 Register Field Descriptions

Field	Description
0 PRR1AN	<p>Pin Routing Register ADC channels — Select alternative routing for AN15/14/13/11/10 pins to port C This bit programs the routing of the specific ADC channels to alternative external pins in 100 LQFP. See Table 2-82. The routing affects the analog signals and digital input trigger paths to the ADC. Refer to the related pin descriptions in Section 2.3.4, “Pins PC7-0” and Section 2.3.12, “Pins AD15-0”.</p> <p>1 AN inputs on port C 0 AN inputs on port AD</p>

Chapter 5

S12G Memory Map Controller (S12GMMCV1)

Table 5-1. Revision History Table

Rev. No. (Item No.)	Date (Submitted By)	Sections Affected	Substantial Change(s)
01.02	20-May 2010		Updates for S12VR48 and S12VR64

5.1 Introduction

The S12GMMC module controls the access to all internal memories and peripherals for the CPU12 and S12SBDM module. It regulates access priorities and determines the address mapping of the on-chip resources. [Figure 5-1](#) shows a block diagram of the S12GMMC module.

5.1.1 Glossary

Table 5-2. Glossary Of Terms

Term	Definition
Local Addresses	Address within the CPU12's Local Address Map (Figure 5-11)
Global Address	Address within the Global Address Map (Figure 5-11)
Aligned Bus Access	Bus access to an even address.
Misaligned Bus Access	Bus access to an odd address.
NS	Normal Single-Chip Mode
SS	Special Single-Chip Mode
Unimplemented Address Ranges	Address ranges which are not mapped to any on-chip resource.
NVM	Non-volatile Memory; Flash or EEPROM
IFR	NVM Information Row. Refer to FTMRG Block Guide

5.1.2 Overview

The S12GMMC connects the CPU12's and the S12SBDM's bus interfaces to the MCU's on-chip resources (memories and peripherals). It arbitrates the bus accesses and determines all of the MCU's memory maps. Furthermore, the S12GMMC is responsible for constraining memory accesses on secured devices and for selecting the MCU's functional mode.

Table 7-3. BDMSTS Field Descriptions

Field	Description
7 ENBDM	<p>Enable BDM — This bit controls whether the BDM is enabled or disabled. When enabled, BDM can be made active to allow firmware commands to be executed. When disabled, BDM cannot be made active but BDM hardware commands are still allowed.</p> <p>0 BDM disabled 1 BDM enabled</p> <p>Note: ENBDM is set out of reset in special single chip mode. In special single chip mode with the device secured, this bit will not be set until after the Flash erase verify tests are complete.</p>
6 BDMACT	<p>BDM Active Status — This bit becomes set upon entering BDM. The standard BDM firmware lookup table is then enabled and put into the memory map. BDMACT is cleared by a carefully timed store instruction in the standard BDM firmware as part of the exit sequence to return to user code and remove the BDM memory from the map.</p> <p>0 BDM not active 1 BDM active</p>
4 SDV	<p>Shift Data Valid — This bit is set and cleared by the BDM hardware. It is set after data has been transmitted as part of a BDM firmware or hardware read command or after data has been received as part of a BDM firmware or hardware write command. It is cleared when the next BDM command has been received or BDM is exited. SDV is used by the standard BDM firmware to control program flow execution.</p> <p>0 Data phase of command not complete 1 Data phase of command is complete</p>
3 TRACE	<p>TRACE1 BDM Firmware Command is Being Executed — This bit gets set when a BDM TRACE1 firmware command is first recognized. It will stay set until BDM firmware is exited by one of the following BDM commands: GO or GO_UNTIL.</p> <p>0 TRACE1 command is not being executed 1 TRACE1 command is being executed</p>
1 UNSEC	<p>Unsecure — If the device is secured this bit is only writable in special single chip mode from the BDM secure firmware. It is in a zero state as secure mode is entered so that the secure BDM firmware lookup table is enabled and put into the memory map overlapping the standard BDM firmware lookup table. The secure BDM firmware lookup table verifies that the on-chip Flash is erased. This being the case, the UNSEC bit is set and the BDM program jumps to the start of the standard BDM firmware lookup table and the secure BDM firmware lookup table is turned off. If the erase test fails, the UNSEC bit will not be asserted.</p> <p>0 System is in a secured mode. 1 System is in a unsecured mode.</p> <p>Note: When UNSEC is set, security is off and the user can change the state of the secure bits in the on-chip Flash EEPROM. Note that if the user does not change the state of the bits to “unsecured” mode, the system will be secured again when it is next taken out of reset. After reset this bit has no meaning or effect when the security byte in the Flash EEPROM is configured for unsecure mode.</p>

Register Global Address 0x3_FF06

	7	6	5	4	3	2	1	0
R	CCR7	CCR6	CCR5	CCR4	CCR3	CCR2	CCR1	CCR0
W								
Reset								
Special Single-Chip Mode	1	1	0	0	1	0	0	0
All Other Modes	0	0	0	0	0	0	0	0

Figure 7-4. BDM CCR Holding Register (BDMCCR)

Read: All modes through BDM operation when not secured

Table 8-39. PCH Field Descriptions (continued)

Bit	Description
0 PC16	Program Counter bit 16 — In Normal and Loop1 mode this bit corresponds to program counter bit 16.

8.4.5.4 Trace Buffer Organization (Compressed Pure PC mode)

Table 8-40. Trace Buffer Organization Example (Compressed PurePC mode)

Mode	Line Number	2-bits	6-bits	6-bits	6-bits
		Field 3	Field 2	Field 1	Field 0
Compressed Pure PC Mode	Line 1	00	PC1 (Initial 18-bit PC Base Address)		
	Line 2	11	PC4	PC3	PC2
	Line 3	01	0	0	PC5
	Line 4	00	PC6 (New 18-bit PC Base Address)		
	Line 5	10	0	PC8	PC7
	Line 6	00	PC9 (New 18-bit PC Base Address)		

NOTE

Configured for end aligned triggering in compressed PurePC mode, then after rollover it is possible that the oldest base address is overwritten. In this case all entries between the pointer and the next base address have lost their base address following rollover. For example in [Table 8-40](#) if one line of rollover has occurred, Line 1, PC1, is overwritten with a new entry. Thus the entries on Lines 2 and 3 have lost their base address. For reconstruction of program flow the first base address following the pointer must be used, in the example, Line 4. The pointer points to the oldest entry, Line 2.

Field3 Bits in Compressed Pure PC Modes

Table 8-41. Compressed Pure PC Mode Field 3 Information Bit Encoding

INF1	INF0	TRACE BUFFER ROW CONTENT
0	0	Base PC address TB[17:0] contains a full PC[17:0] value
0	1	Trace Buffer[5:0] contain incremental PC relative to base address zero value
1	0	Trace Buffer[11:0] contain next 2 incremental PCs relative to base address zero value
1	1	Trace Buffer[17:0] contain next 3 incremental PCs relative to base address zero value

Each time that PC[17:6] differs from the previous base PC[17:6], then a new base address is stored. The base address zero value is the lowest address in the 64 address range

The first line of the trace buffer always gets a base PC address, this applies also on rollover.

Table 16-14. ATDCTL5 Field Descriptions (continued)

Field	Description
4 MULT	<p>Multi-Channel Sample Mode — When MULT is 0, the ATD sequence controller samples only from the specified analog input channel for an entire conversion sequence. The analog channel is selected by channel selection code (control bits CD/CC/CB/CA located in ATDCTL5). When MULT is 1, the ATD sequence controller samples across channels. The number of channels sampled is determined by the sequence length value (S8C, S4C, S2C, S1C). The first analog channel examined is determined by channel selection code (CD, CC, CB, CA control bits); subsequent channels sampled in the sequence are determined by incrementing the channel selection code or wrapping around to AN0 (channel 0).</p> <p>0 Sample only one channel 1 Sample across several channels</p>
3–0 CD, CC, CB, CA	<p>Analog Input Channel Select Code — These bits select the analog input channel(s). Table 16-15 lists the coding used to select the various analog input channels.</p> <p>In the case of single channel conversions (MULT=0), this selection code specifies the channel to be examined.</p> <p>In the case of multiple channel conversions (MULT=1), this selection code specifies the first channel to be examined in the conversion sequence. Subsequent channels are determined by incrementing the channel selection code or wrapping around to AN0 (after converting the channel defined by the Wrap Around Channel Select Bits WRAP3-0 in ATDCTL0). When starting with a channel number higher than the one defined by WRAP3-0 the first wrap around will be AN16 to AN0.</p>

Table 16-15. Analog Input Channel Select Coding

SC	CD	CC	CB	CA	Analog Input Channel
0	0	0	0	0	AN0
	0	0	0	1	AN1
	0	0	1	0	AN2
	0	0	1	1	AN3
	0	1	0	0	AN4
	0	1	0	1	AN5
	0	1	1	0	AN6
	0	1	1	1	AN7
	1	0	0	0	AN8
	1	0	0	1	AN9
	1	0	1	0	AN10
	1	0	1	1	AN11
	1	1	0	0	AN12
	1	1	0	1	AN13
	1	1	1	0	AN14
1	1	1	1	AN15	

¹ Read: Anytime
Write: Anytime in initialization mode (INITRQ = 1 and INITAK = 1)

Table 18-25. CANIDMR4–CANIDMR7 Register Field Descriptions

Field	Description
7-0 AM[7:0]	<p>Acceptance Mask Bits — If a particular bit in this register is cleared, this indicates that the corresponding bit in the identifier acceptance register must be the same as its identifier bit before a match is detected. The message is accepted if all such bits match. If a bit is set, it indicates that the state of the corresponding bit in the identifier acceptance register does not affect whether or not the message is accepted.</p> <p>0 Match corresponding acceptance code register and identifier bits 1 Ignore corresponding acceptance code register bit</p>

18.3.3 Programmer’s Model of Message Storage

The following section details the organization of the receive and transmit message buffers and the associated control registers.

To simplify the programmer interface, the receive and transmit message buffers have the same outline. Each message buffer allocates 16 bytes in the memory map containing a 13 byte data structure.

An additional transmit buffer priority register (TBPR) is defined for the transmit buffers. Within the last two bytes of this memory map, the MSCAN stores a special 16-bit time stamp, which is sampled from an internal timer after successful transmission or reception of a message. This feature is only available for transmit and receiver buffers, if the TIME bit is set (see [Section 18.3.2.1, “MSCAN Control Register 0 \(CANCTL0\)”](#)).

The time stamp register is written by the MSCAN. The CPU can only read these registers.

20.1.2 Features

The SCI includes these distinctive features:

- Full-duplex or single-wire operation
- Standard mark/space non-return-to-zero (NRZ) format
- Selectable IrDA 1.4 return-to-zero-inverted (RZI) format with programmable pulse widths
- 13-bit baud rate selection
- Programmable 8-bit or 9-bit data format
- Separately enabled transmitter and receiver
- Programmable polarity for transmitter and receiver
- Programmable transmitter output parity
- Two receiver wakeup methods:
 - Idle line wakeup
 - Address mark wakeup
- Interrupt-driven operation with eight flags:
 - Transmitter empty
 - Transmission complete
 - Receiver full
 - Idle receiver input
 - Receiver overrun
 - Noise error
 - Framing error
 - Parity error
 - Receive wakeup on active edge
 - Transmit collision detect supporting LIN
 - Break Detect supporting LIN
- Receiver framing error detection
- Hardware parity checking
- 1/16 bit-time noise detection

20.1.3 Modes of Operation

The SCI functions the same in normal, special, and emulation modes. It has two low power modes, wait and stop modes.

- Run mode
- Wait mode
- Stop mode

23.4.5 Event Counter Mode

Clearing the PAMOD bit configures the PACNT for event counter operation. An active edge on the IOC7 pin increments the pulse accumulator counter. The PEDGE bit selects falling edges or rising edges to increment the count.

NOTE

The PACNT input and timer channel 7 use the same pin IOC7. To use the IOC7, disconnect it from the output logic by clearing the channel 7 output mode and output level bits, OM7 and OL7. Also clear the channel 7 output compare 7 mask bit, OC7M7.

The Pulse Accumulator counter register reflect the number of active input edges on the PACNT input pin since the last reset.

The PAOVF bit is set when the accumulator rolls over from 0xFFFF to 0x0000. The pulse accumulator overflow interrupt enable bit, PAOVI, enables the PAOVF flag to generate interrupt requests.

NOTE

The pulse accumulator counter can operate in event counter mode even when the timer enable bit, TEN, is clear.

23.4.6 Gated Time Accumulation Mode

Setting the PAMOD bit configures the pulse accumulator for gated time accumulation operation. An active level on the PACNT input pin enables a divided-by-64 clock to drive the pulse accumulator. The PEDGE bit selects low levels or high levels to enable the divided-by-64 clock.

The trailing edge of the active level at the IOC7 pin sets the PAIF. The PAI bit enables the PAIF flag to generate interrupt requests.

The pulse accumulator counter register reflect the number of pulses from the divided-by-64 clock since the last reset.

NOTE

The timer prescaler generates the divided-by-64 clock. If the timer is not active, there is no divided-by-64 clock.

23.5 Resets

The reset state of each individual bit is listed within [Section 23.3, “Memory Map and Register Definition”](#) which details the registers and their bit fields

23.6 Interrupts

This section describes interrupts originated by the TIM16B8CV3 block. [Table 23-25](#) lists the interrupts generated by the TIM16B8CV3 to communicate with the MCU.

25.4.4.3 Valid Flash Module Commands

Table 25-27 present the valid Flash commands, as enabled by the combination of the functional MCU mode (Normal SingleChip NS, Special Singlechip SS) with the MCU security state (Unsecured, Secured).

Special Singlechip mode is selected by input `mmc_ss_mode_ts2` asserted. MCU Secured state is selected by input `mmc_secure` input asserted.

Table 25-27. Flash Commands by Mode and Security State

FCMD	Command	Unsecured		Secured	
		NS ¹	SS ²	NS ³	SS ⁴
0x01	Erase Verify All Blocks	*	*	*	*
0x02	Erase Verify Block	*	*	*	*
0x03	Erase Verify P-Flash Section	*	*	*	
0x04	Read Once	*	*	*	
0x06	Program P-Flash	*	*	*	
0x07	Program Once	*	*	*	
0x08	Erase All Blocks		*		*
0x09	Erase Flash Block	*	*	*	
0x0A	Erase P-Flash Sector	*	*	*	
0x0B	Unsecure Flash		*		*
0x0C	Verify Backdoor Access Key	*		*	
0x0D	Set User Margin Level	*	*	*	
0x0E	Set Field Margin Level		*		
0x10	Erase Verify EEPROM Section	*	*	*	
0x11	Program EEPROM	*	*	*	
0x12	Erase EEPROM Sector	*	*	*	

¹ Unsecured Normal Single Chip mode

² Unsecured Special Single Chip mode.

³ Secured Normal Single Chip mode.

⁴ Secured Special Single Chip mode.

25.4.4.4 P-Flash Commands

Table 25-28 summarizes the valid P-Flash commands along with the effects of the commands on the P-Flash block and other resources within the Flash module.

Table 25-28. P-Flash Commands

FCMD	Command	Function on P-Flash Memory
0x01	Erase Verify All Blocks	Verify that all P-Flash (and EEPROM) blocks are erased.

26.4.7 Interrupts

The Flash module can generate an interrupt when a Flash command operation has completed or when a Flash command operation has detected an ECC fault.

Table 26-66. Flash Interrupt Sources

Interrupt Source	Interrupt Flag	Local Enable	Global (CCR) Mask
Flash Command Complete	CCIF (FSTAT register)	CCIE (FCNFG register)	I Bit
ECC Double Bit Fault on Flash Read	DFDIF (FERSTAT register)	DFDIE (FERCNFG register)	I Bit
ECC Single Bit Fault on Flash Read	SFDIF (FERSTAT register)	SFDIE (FERCNFG register)	I Bit

NOTE

Vector addresses and their relative interrupt priority are determined at the MCU level.

26.4.7.1 Description of Flash Interrupt Operation

The Flash module uses the CCIF flag in combination with the CCIE interrupt enable bit to generate the Flash command interrupt request. The Flash module uses the DFDIF and SFDIF flags in combination with the DFDIE and SFDIE interrupt enable bits to generate the Flash error interrupt request. For a detailed description of the register bits involved, refer to [Section 26.3.2.5, “Flash Configuration Register \(FCNFG\)”](#), [Section 26.3.2.6, “Flash Error Configuration Register \(FERCNFG\)”](#), [Section 26.3.2.7, “Flash Status Register \(FSTAT\)”](#), and [Section 26.3.2.8, “Flash Error Status Register \(FERSTAT\)”](#).

The logic used for generating the Flash module interrupts is shown in [Figure 26-27](#).

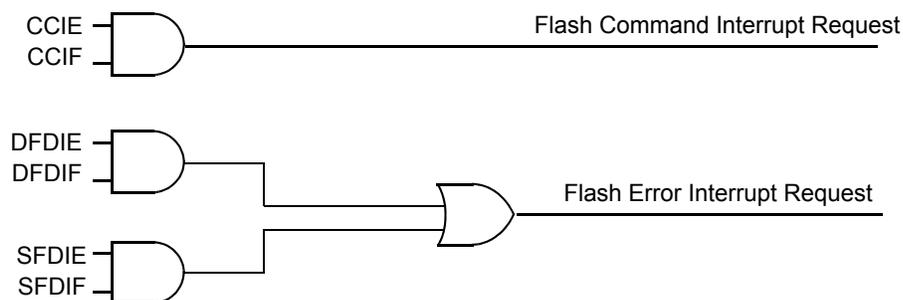


Figure 26-27. Flash Module Interrupts Implementation

The reserved nonvolatile information register accessed by the Program Once command cannot be erased and any attempt to program one of these phrases a second time will not be allowed. Valid phrase index values for the Program Once command range from 0x0000 to 0x0007. During execution of the Program Once command, any attempt to read addresses within P-Flash will return invalid data.

Table 28-43. Program Once Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 101 at command launch
		Set if command not available in current mode (see Table 28-27)
		Set if an invalid phrase index is supplied
		Set if the requested phrase has already been programmed ¹
	FPVIOL	None
	MGSTAT1	Set if any errors have been encountered during the verify operation
MGSTAT0	Set if any non-correctable errors have been encountered during the verify operation	

¹ If a Program Once phrase is initially programmed to 0xFFFF_FFFF_FFFF_FFFF, the Program Once command will be allowed to execute again on that same phrase.

28.4.6.7 Erase All Blocks Command

The Erase All Blocks operation will erase the entire P-Flash and EEPROM memory space.

Table 28-44. Erase All Blocks Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x08	Not required

Upon clearing CCIF to launch the Erase All Blocks command, the Memory Controller will erase the entire Flash memory space and verify that it is erased. If the Memory Controller verifies that the entire Flash memory space was properly erased, security will be released. During the execution of this command (CCIF=0) the user must not write to any Flash module register. The CCIF flag will set after the Erase All Blocks operation has completed.

Table 28-45. Erase All Blocks Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 000 at command launch
		Set if command not available in current mode (see Table 28-27)
	FPVIOL	Set if any area of the P-Flash or EEPROM memory is protected
	MGSTAT1	Set if any errors have been encountered during the verify operation ¹
	MGSTAT0	Set if any non-correctable errors have been encountered during the verify operation ¹

¹ As found in the memory map for FTMRG96K1.

Table 29-8. FDIV values for various BUSCLK Frequencies

BUSCLK Frequency (MHz)		FDIV[5:0]	BUSCLK Frequency (MHz)		FDIV[5:0]
MIN ¹	MAX ²		MIN ¹	MAX ²	
1.0	1.6	0x00	16.6	17.6	0x10
1.6	2.6	0x01	17.6	18.6	0x11
2.6	3.6	0x02	18.6	19.6	0x12
3.6	4.6	0x03	19.6	20.6	0x13
4.6	5.6	0x04	20.6	21.6	0x14
5.6	6.6	0x05	21.6	22.6	0x15
6.6	7.6	0x06	22.6	23.6	0x16
7.6	8.6	0x07	23.6	24.6	0x17
8.6	9.6	0x08	24.6	25.6	0x18
9.6	10.6	0x09			
10.6	11.6	0x0A			
11.6	12.6	0x0B			
12.6	13.6	0x0C			
13.6	14.6	0x0D			
14.6	15.6	0x0E			
15.6	16.6	0x0F			

¹ BUSCLK is Greater Than this value.
² BUSCLK is Less Than or Equal to this value.

29.3.2.2 Flash Security Register (FSEC)

The FSEC register holds all bits associated with the security of the MCU and Flash module.

Offset Module Base + 0x0001

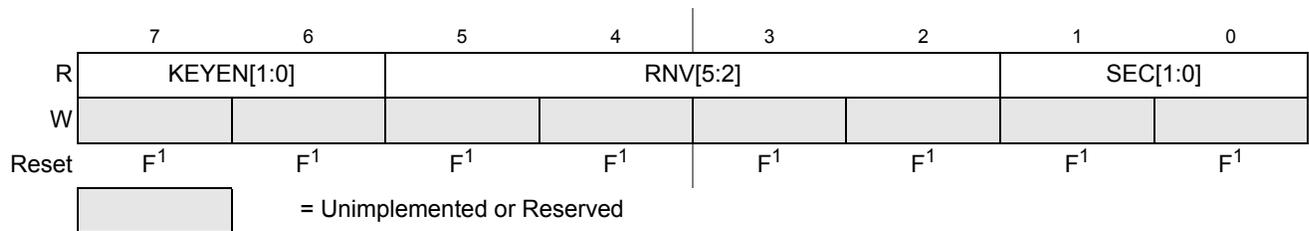


Figure 29-6. Flash Security Register (FSEC)

¹ Loaded from IFR Flash configuration field, during reset sequence.

All bits in the FSEC register are readable but not writable.

During the reset sequence, the FSEC register is loaded with the contents of the Flash security byte in the Flash configuration field at global address 0x3_FF0F located in P-Flash memory (see [Table 29-4](#)) as

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either V_{SS35} or V_{DD35}).

Table A-1. Absolute Maximum Ratings¹

Num	Rating	Symbol	Min	Max	Unit
1	I/O, regulator and analog supply voltage	V_{DD35}	-0.3	6.0	V
2	Voltage difference V_{DDX} to V_{DDA}	ΔV_{DDX}	-6.0	0.3	V
3	Voltage difference V_{SSX} to V_{SSA}	ΔV_{SSX}	-0.3	0.3	V
4	Digital I/O input voltage	V_{IN}	-0.3	6.0	V
5	Analog reference	V_{RH}	-0.3	6.0	V
6	EXTAL, XTAL	V_{ILV}	-0.3	2.16	V
7	Instantaneous maximum current Single pin limit for all digital I/O pins ²	I_D	-25	+25	mA
8	Instantaneous maximum current Single pin limit for EXTAL, XTAL	I_{DL}	-25	+25	mA
9	Maximum current Single pin limit for power supply pins	I_{DV}	-60	+60	mA
10	Storage temperature range	T_{stg}	-65	155	°C

¹ Beyond absolute maximum ratings device might be damaged.

² All digital I/O pins are internally clamped to V_{SSX} and V_{DDX} , or V_{SSA} and V_{DDA} .

A.1.6 ESD Protection and Latch-up Immunity

All ESD testing is in conformity with CDF-AEC-Q100 stress test qualification for automotive grade integrated circuits. During the device qualification ESD stresses were performed for the Human Body Model (HBM) and the Charge Device Model.

A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

0x0070–0x09F Analog to Digital Converter (ADC)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
0x007A	ATDSTAT2H	R	CCF[15:8]							
		W								
0x007B	ATDSTAT2L	R	CCF[7:0]							
		W								
0x007C	ATDDIENH	R	IEN[15:8]							
		W								
0x007D	ATDDIENL	R	IEN[7:0]							
		W								
0x007E	ATDCMPHTH	R	CMPHT[15:8]							
		W								
0x007F	ATDCMPHTL	R	CMPHT[7:0]							
		W								
0x0080- 0x0091	ATDDR0	R	See Section 16.3.2.12.1, “Left Justified Result Data (DJM=0)” and Section 16.3.2.12.2, “Right Justified Result Data (DJM=1)”							
		W								
0x0082- 0x0083	ATDDR1	R	See Section 16.3.2.12.1, “Left Justified Result Data (DJM=0)” and Section 16.3.2.12.2, “Right Justified Result Data (DJM=1)”							
		W								
0x0084- 0x0085	ATDDR2	R	See Section 16.3.2.12.1, “Left Justified Result Data (DJM=0)” and Section 16.3.2.12.2, “Right Justified Result Data (DJM=1)”							
		W								
0x0086- 0x0087	ATDDR3	R	See Section 16.3.2.12.1, “Left Justified Result Data (DJM=0)” and Section 16.3.2.12.2, “Right Justified Result Data (DJM=1)”							
		W								
0x0088- 0x0089	ATDDR4	R	See Section 16.3.2.12.1, “Left Justified Result Data (DJM=0)” and Section 16.3.2.12.2, “Right Justified Result Data (DJM=1)”							
		W								
0x008A- 0x008B	ATDDR5	R	See Section 16.3.2.12.1, “Left Justified Result Data (DJM=0)” and Section 16.3.2.12.2, “Right Justified Result Data (DJM=1)”							
		W								
0x008C- 0x008D	ATDDR6	R	See Section 16.3.2.12.1, “Left Justified Result Data (DJM=0)” and Section 16.3.2.12.2, “Right Justified Result Data (DJM=1)”							
		W								
0x008E- 0x008F	ATDDR7	R	See Section 16.3.2.12.1, “Left Justified Result Data (DJM=0)” and Section 16.3.2.12.2, “Right Justified Result Data (DJM=1)”							
		W								
0x0090- 0x0091	ATDDR8	R	See Section 16.3.2.12.1, “Left Justified Result Data (DJM=0)” and Section 16.3.2.12.2, “Right Justified Result Data (DJM=1)”							
		W								
0x0092- 0x0093	ATDDR9	R	See Section 16.3.2.12.1, “Left Justified Result Data (DJM=0)” and Section 16.3.2.12.2, “Right Justified Result Data (DJM=1)”							
		W								
0x0094- 0x0095	ATDDR10	R	See Section 16.3.2.12.1, “Left Justified Result Data (DJM=0)” and Section 16.3.2.12.2, “Right Justified Result Data (DJM=1)”							
		W								
0x0096- 0x0097	ATDDR11	R	See Section 16.3.2.12.1, “Left Justified Result Data (DJM=0)” and Section 16.3.2.12.2, “Right Justified Result Data (DJM=1)”							
		W								
0x0098- 0x0099	ATDDR12	R	See Section 16.3.2.12.1, “Left Justified Result Data (DJM=0)” and Section 16.3.2.12.2, “Right Justified Result Data (DJM=1)”							
		W								
0x009A- 0x009B	ATDDR13	R	See Section 16.3.2.12.1, “Left Justified Result Data (DJM=0)” and Section 16.3.2.12.2, “Right Justified Result Data (DJM=1)”							
		W								
0x009C- 0x009D	ATDDR14	R	See Section 16.3.2.12.1, “Left Justified Result Data (DJM=0)” and Section 16.3.2.12.2, “Right Justified Result Data (DJM=1)”							
		W								
0x009E- 0x009F	ATDDR15	R	See Section 16.3.2.12.1, “Left Justified Result Data (DJM=0)” and Section 16.3.2.12.2, “Right Justified Result Data (DJM=1)”							
		W								