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Product Status	Active
Core Processor	12V1
Core Size	16-Bit
Speed	25MHz
Connectivity	CANbus, IrDA, LINbus, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	26
Program Memory Size	48KB (48K x 8)
Program Memory Type	FLASH
EEPROM Size	1.5K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3.13V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
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Supplier Device Package	32-LQFP (7x7)
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Chapter 16

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Chapter 18

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Table 2-78. PTI1AD Register Field Descriptions

Field	Description
7-0 PTI1AD	Port AD input data— A read always returns the buffered input state of the associated pin. It can be used to detect overload or short circuit conditions on output pins.

2.4.3.53 Port AD Data Direction Register (DDR0AD)

Address 0x0274 (G1, G2)

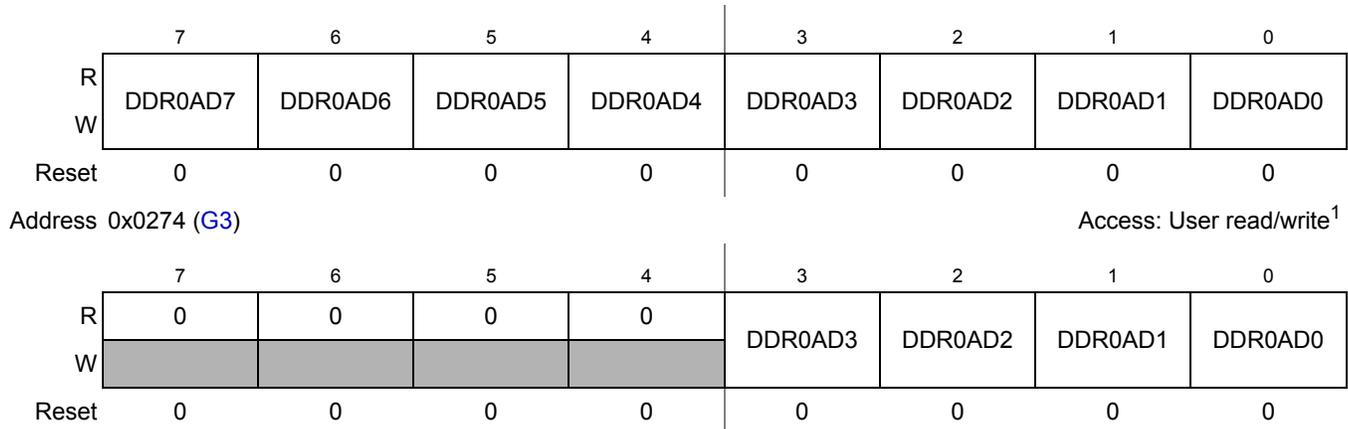
Access: User read/write¹

Figure 2-53. Port AD Data Direction Register (DDR0AD)

¹ Read: Anytime
Write: Anytime

Table 2-79. DDR0AD Register Field Descriptions

Field	Description
7-0 DDR0AD	Port AD data direction— This bit determines whether the associated pin is an input or output. 1 Associated pin configured as output 0 Associated pin configured as input

2.4.3.54 Port AD Data Direction Register (DDR1AD)

Address 0x0275

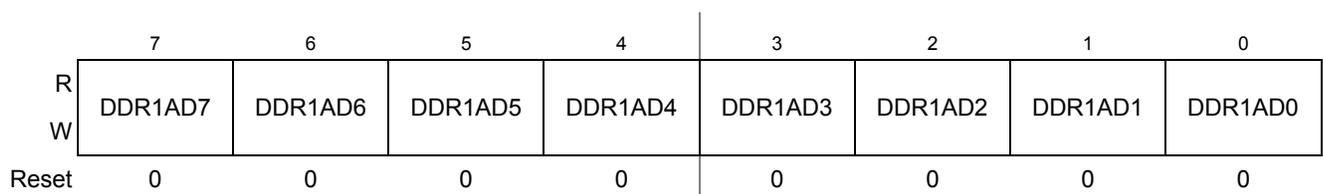
Access: User read/write¹

Figure 2-54. Port AD Data Direction Register (DDR1AD)

¹ Read: Anytime
Write: Anytime

Figure 7-11 shows the ACK handshake protocol in a command level timing diagram. The READ_BYTE instruction is used as an example. First, the 8-bit instruction opcode is sent by the host, followed by the address of the memory location to be read. The target BDM decodes the instruction. A bus cycle is grabbed (free or stolen) by the BDM and it executes the READ_BYTE operation. Having retrieved the data, the BDM issues an ACK pulse to the host controller, indicating that the addressed byte is ready to be retrieved. After detecting the ACK pulse, the host initiates the byte retrieval process. Note that data is sent in the form of a word and the host needs to determine which is the appropriate byte based on whether the address was odd or even.

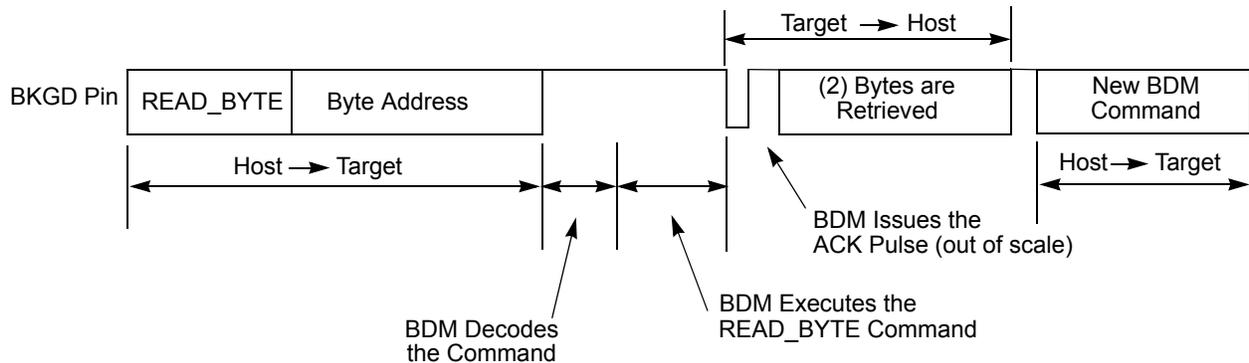


Figure 7-11. Handshake Protocol at Command Level

Differently from the normal bit transfer (where the host initiates the transmission), the serial interface ACK handshake pulse is initiated by the target MCU by issuing a negative edge in the BKGD pin. The hardware handshake protocol in Figure 7-10 specifies the timing when the BKGD pin is being driven, so the host should follow this timing constraint in order to avoid the risk of an electrical conflict in the BKGD pin.

NOTE

The only place the BKGD pin can have an electrical conflict is when one side is driving low and the other side is issuing a speedup pulse (high). Other “highs” are pulled rather than driven. However, at low rates the time of the speedup pulse can become lengthy and so the potential conflict time becomes longer as well.

The ACK handshake protocol does not support nested ACK pulses. If a BDM command is not acknowledge by an ACK pulse, the host needs to abort the pending command first in order to be able to issue a new BDM command. When the CPU enters wait or stop while the host issues a hardware command (e.g., WRITE_BYTE), the target discards the incoming command due to the wait or stop being detected. Therefore, the command is not acknowledged by the target, which means that the ACK pulse will not be issued in this case. After a certain time the host (not aware of stop or wait) should decide to abort any possible pending ACK pulse in order to be sure a new command can be issued. Therefore, the protocol provides a mechanism in which a command, and its corresponding ACK, can be aborted.

Table 12-11. ATD Behavior in Freeze Mode (Breakpoint)

FRZ1	FRZ0	Behavior in Freeze Mode
0	0	Continue conversion
0	1	Reserved
1	0	Finish current conversion, then freeze
1	1	Freeze Immediately

12.3.2.5 ATD Control Register 4 (ATDCTL4)

Writes to this register will abort current conversion sequence.

Module Base + 0x0004

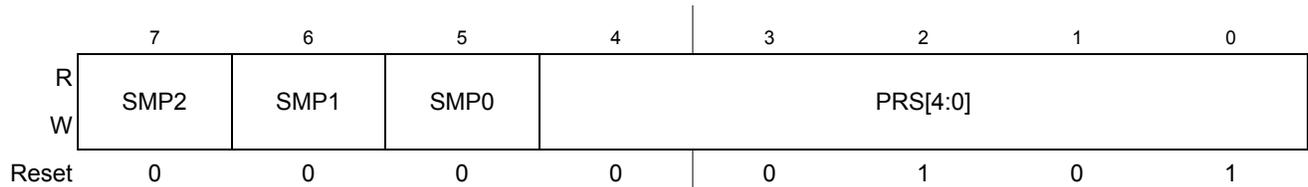


Figure 12-7. ATD Control Register 4 (ATDCTL4)

Read: Anytime

Write: Anytime

Table 12-12. ATDCTL4 Field Descriptions

Field	Description
7–5 SMP[2:0]	Sample Time Select — These three bits select the length of the sample time in units of ATD conversion clock cycles. Note that the ATD conversion clock period is itself a function of the prescaler value (bits PRS4-0). Table 12-13 lists the available sample time lengths.
4–0 PRS[4:0]	ATD Clock Prescaler — These 5 bits are the binary prescaler value PRS. The ATD conversion clock frequency is calculated as follows: $f_{\text{ATDCLK}} = \frac{f_{\text{BUS}}}{2 \times (\text{PRS} + 1)}$ Refer to Device Specification for allowed frequency range of f_{ATDCLK} .

Table 12-13. Sample Time Select

SMP2	SMP1	SMP0	Sample Time in Number of ATD Clock Cycles
0	0	0	4
0	0	1	6
0	1	0	8
0	1	1	10
1	0	0	12
1	0	1	16
1	1	0	20

Analog-to-Digital Converter (ADC10B12CV2)

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0	
0x0003	ATDCTL3	R W	DJM	S8C	S4C	S2C	S1C	FIFO	FRZ1	FRZ0	
0x0004	ATDCTL4	R W	SMP2	SMP1	SMP0	PRS[4:0]					
0x0005	ATDCTL5	R W	0	SC	SCAN	MULT	CD	CC	CB	CA	
0x0006	ATDSTAT0	R W	SCF	0	ETORF	FIFOR	CC3	CC2	CC1	CC0	
0x0007	Unimplemented	R W	0	0	0	0	0	0	0	0	
0x0008	ATDCMPEH	R W	0	0	0	0	CMPE[11:8]				
0x0009	ATDCMPEL	R W	CMPE[7:0]								
0x000A	ATDSTAT2H	R W	0	0	0	0	CCF[11:8]				
0x000B	ATDSTAT2L	R W	CCF[7:0]								
0x000C	ATDDIENH	R W	1	1	1	1	IEN[11:8]				
0x000D	ATDDIENL	R W	IEN[7:0]								
0x000E	ATDCMPHTH	R W	0	0	0	0	CMPHT[11:8]				
0x000F	ATDCMPHTL	R W	CMPHT[7:0]								
0x0010	ATDDR0	R W	See Section 13.3.2.12.1, "Left Justified Result Data (DJM=0)" and Section 13.3.2.12.2, "Right Justified Result Data (DJM=1)"								
0x0012	ATDDR1	R W	See Section 13.3.2.12.1, "Left Justified Result Data (DJM=0)" and Section 13.3.2.12.2, "Right Justified Result Data (DJM=1)"								
0x0014	ATDDR2	R W	See Section 13.3.2.12.1, "Left Justified Result Data (DJM=0)" and Section 13.3.2.12.2, "Right Justified Result Data (DJM=1)"								
0x0016	ATDDR3	R W	See Section 13.3.2.12.1, "Left Justified Result Data (DJM=0)" and Section 13.3.2.12.2, "Right Justified Result Data (DJM=1)"								
0x0018	ATDDR4	R W	See Section 13.3.2.12.1, "Left Justified Result Data (DJM=0)" and Section 13.3.2.12.2, "Right Justified Result Data (DJM=1)"								
0x001A	ATDDR5	R W	See Section 13.3.2.12.1, "Left Justified Result Data (DJM=0)" and Section 13.3.2.12.2, "Right Justified Result Data (DJM=1)"								
0x001C	ATDDR6	R W	See Section 13.3.2.12.1, "Left Justified Result Data (DJM=0)" and Section 13.3.2.12.2, "Right Justified Result Data (DJM=1)"								
0x001E	ATDDR7	R W	See Section 13.3.2.12.1, "Left Justified Result Data (DJM=0)" and Section 13.3.2.12.2, "Right Justified Result Data (DJM=1)"								
0x0020	ATDDR8	R W	See Section 13.3.2.12.1, "Left Justified Result Data (DJM=0)" and Section 13.3.2.12.2, "Right Justified Result Data (DJM=1)"								
0x0022	ATDDR9	R W	See Section 13.3.2.12.1, "Left Justified Result Data (DJM=0)" and Section 13.3.2.12.2, "Right Justified Result Data (DJM=1)"								

= Unimplemented or Reserved

Figure 13-2. ADC10B12C Register Summary (Sheet 2 of 3)

16.3.2.10 ATD Input Enable Register (ATDDIEN)

Module Base + 0x000C

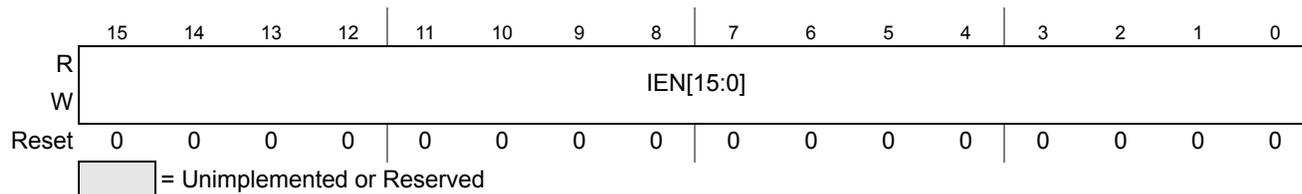


Figure 16-12. ATD Input Enable Register (ATDDIEN)

Read: Anytime

Write: Anytime

Table 16-19. ATDDIEN Field Descriptions

Field	Description
15–0 IEN[15:0]	<p>ATD Digital Input Enable on channel x ($x= 15, 14, 13, 12, 11, 10, 9, 8, 7, 6, 5, 4, 3, 2, 1, 0$) — This bit controls the digital input buffer from the analog input pin (ANx) to the digital data register.</p> <p>0 Disable digital input buffer to ANx pin 1 Enable digital input buffer on ANx pin.</p> <p>Note: Setting this bit will enable the corresponding digital input buffer continuously. If this bit is set while simultaneously using it as an analog port, there is potentially increased power consumption because the digital input buffer maybe in the linear region.</p>

16.3.2.11 ATD Compare Higher Than Register (ATDCMPHT)

Writes to this register will abort current conversion sequence.

Read: Anytime

Write: Anytime

Module Base + 0x000E

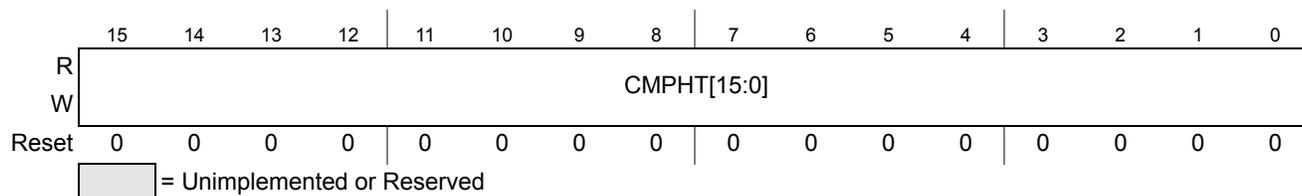


Figure 16-13. ATD Compare Higher Than Register (ATDCMPHT)

Table 16-20. ATDCMPHT Field Descriptions

Field	Description
15–0 CMPHT[15:0]	<p>Compare Operation Higher Than Enable for conversion number n ($n= 15, 14, 13, 12, 11, 10, 9, 8, 7, 6, 5, 4, 3, 2, 1, 0$) of a Sequence ($n$ conversion number, NOT channel number!) — This bit selects the operator for comparison of conversion results.</p> <p>0 If result of conversion n is lower or same than compare value in ATDDRn, this is flagged in ATDSTAT2 1 If result of conversion n is higher than compare value in ATDDRn, this is flagged in ATDSTAT2</p>

18.2.2 TXCAN — CAN Transmitter Output Pin

TXCAN is the MSCAN transmitter output pin. The TXCAN output pin represents the logic level on the CAN bus:

- 0 = Dominant state
- 1 = Recessive state

18.2.3 CAN System

A typical CAN system with MSCAN is shown in [Figure 18-2](#). Each CAN station is connected physically to the CAN bus lines through a transceiver device. The transceiver is capable of driving the large current needed for the CAN bus and has current protection against defective CAN or defective stations.

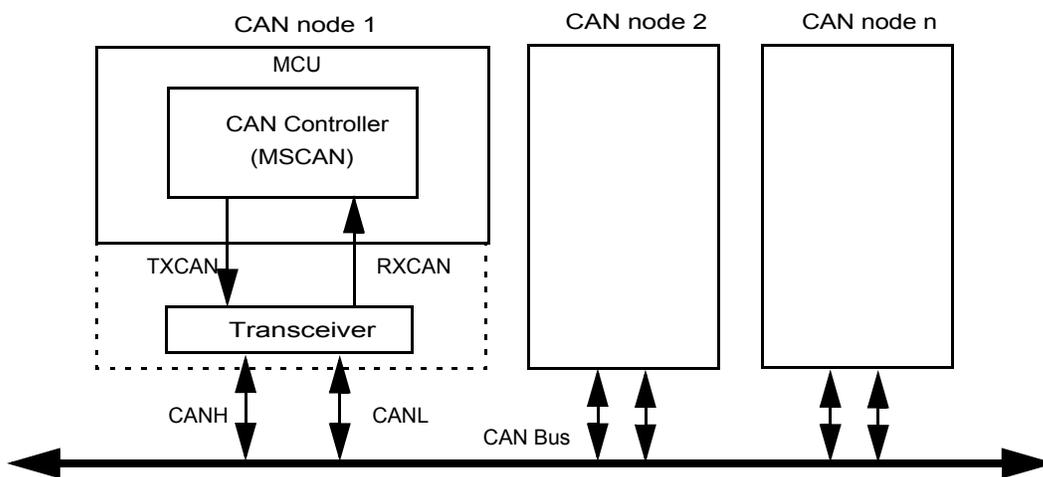


Figure 18-2. CAN System

18.3 Memory Map and Register Definition

This section provides a detailed description of all registers accessible in the MSCAN.

18.3.1 Module Memory Map

[Figure 18-3](#) gives an overview on all registers and their individual bits in the MSCAN memory map. The *register address* results from the addition of *base address* and *address offset*. The *base address* is determined at the MCU level and can be found in the MCU memory map description. The *address offset* is defined at the module level.

The MSCAN occupies 64 bytes in the memory space. The base address of the MSCAN module is determined at the MCU level when the MCU is defined. The register decode map is fixed and begins at the first address of the module address offset.

20.1.2 Features

The SCI includes these distinctive features:

- Full-duplex or single-wire operation
- Standard mark/space non-return-to-zero (NRZ) format
- Selectable IrDA 1.4 return-to-zero-inverted (RZI) format with programmable pulse widths
- 13-bit baud rate selection
- Programmable 8-bit or 9-bit data format
- Separately enabled transmitter and receiver
- Programmable polarity for transmitter and receiver
- Programmable transmitter output parity
- Two receiver wakeup methods:
 - Idle line wakeup
 - Address mark wakeup
- Interrupt-driven operation with eight flags:
 - Transmitter empty
 - Transmission complete
 - Receiver full
 - Idle receiver input
 - Receiver overrun
 - Noise error
 - Framing error
 - Parity error
 - Receive wakeup on active edge
 - Transmit collision detect supporting LIN
 - Break Detect supporting LIN
- Receiver framing error detection
- Hardware parity checking
- 1/16 bit-time noise detection

20.1.3 Modes of Operation

The SCI functions the same in normal, special, and emulation modes. It has two low power modes, wait and stop modes.

- Run mode
- Wait mode
- Stop mode

20.4.5.5 LIN Transmit Collision Detection

This module allows to check for collisions on the LIN bus.

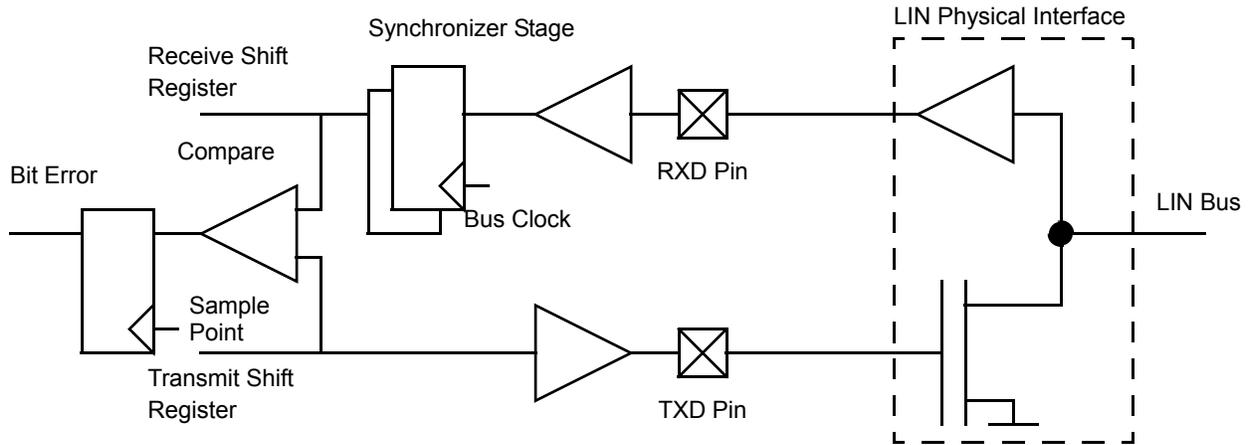


Figure 20-18. Collision Detect Principle

If the bit error circuit is enabled ($BERRM[1:0] = 0:1$ or $= 1:0$), the error detect circuit will compare the transmitted and the received data stream at a point in time and flag any mismatch. The timing checks run when transmitter is active (not idle). As soon as a mismatch between the transmitted data and the received data is detected the following happens:

- The next bit transmitted will have a high level ($TXPOL = 0$) or low level ($TXPOL = 1$)
- The transmission is aborted and the byte in transmit buffer is discarded.
- the transmit data register empty and the transmission complete flag will be set
- The bit error interrupt flag, $BERRIF$, will be set.
- No further transmissions will take place until the $BERRIF$ is cleared.

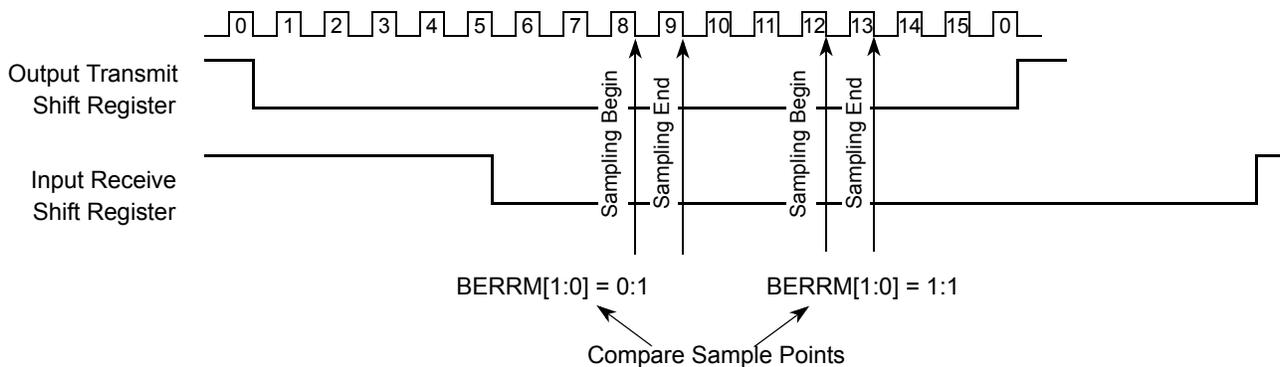


Figure 20-19. Timing Diagram Bit Error Detection

If the bit error detect feature is disabled, the bit error interrupt flag is cleared.

NOTE

The $RXPOL$ and $TXPOL$ bit should be set the same when transmission collision detect feature is enabled, otherwise the bit error interrupt flag may be set incorrectly.

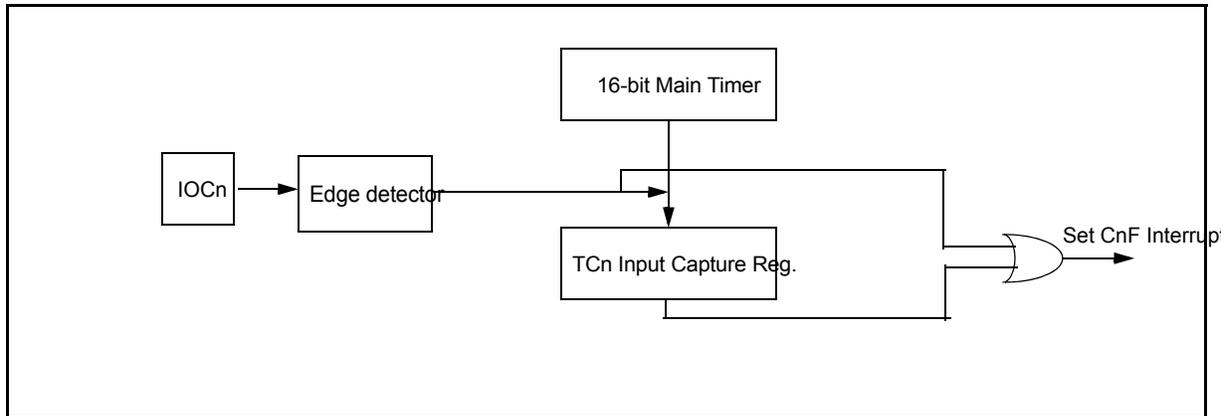


Figure 22-2. Interrupt Flag Setting

22.2 External Signal Description

The TIM16B6CV3 module has a selected number of external pins. Refer to device specification for exact number.

22.2.1 IOC5 - IOC0 — Input Capture and Output Compare Channel 5-0

Those pins serve as input capture or output compare for TIM16B6CV3 channel .

NOTE

For the description of interrupts see [Section 22.6, “Interrupts”](#).

22.3 Memory Map and Register Definition

This section provides a detailed description of all memory and registers.

22.3.1 Module Memory Map

The memory map for the TIM16B6CV3 module is given below in [Figure 22-3](#). The address listed for each register is the address offset. The total address for each register is the sum of the base address for the TIM16B6CV3 module and the address offset for each register.

22.3.2 Register Descriptions

This section consists of register descriptions in address order. Each description includes a standard register diagram with an associated figure number. Details of register bit and field function follow the register diagrams, in bit order.

Offset Module Base + 0x0001

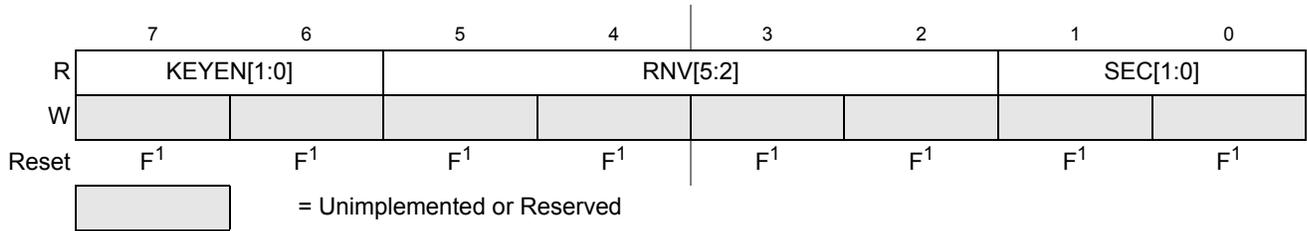


Figure 24-6. Flash Security Register (FSEC)

¹ Loaded from IFR Flash configuration field, during reset sequence.

All bits in the FSEC register are readable but not writable.

During the reset sequence, the FSEC register is loaded with the contents of the Flash security byte in the Flash configuration field at global address 0x3_FF0F located in P-Flash memory (see [Table 24-4](#)) as indicated by reset condition F in [Figure 24-6](#). If a double bit fault is detected while reading the P-Flash phrase containing the Flash security byte during the reset sequence, all bits in the FSEC register will be set to leave the Flash module in a secured state with backdoor key access disabled.

Table 24-9. FSEC Field Descriptions

Field	Description
7–6 KEYEN[1:0]	Backdoor Key Security Enable Bits — The KEYEN[1:0] bits define the enabling of backdoor key access to the Flash module as shown in Table 24-10 .
5–2 RNV[5:2]	Reserved Nonvolatile Bits — The RNV bits should remain in the erased state for future enhancements.
1–0 SEC[1:0]	Flash Security Bits — The SEC[1:0] bits define the security state of the MCU as shown in Table 24-11 . If the Flash module is unsecured using backdoor key access, the SEC bits are forced to 10.

Table 24-10. Flash KEYEN States

KEYEN[1:0]	Status of Backdoor Key Access
00	DISABLED
01	DISABLED ¹
10	ENABLED
11	DISABLED

¹ Preferred KEYEN state to disable backdoor key access.

Table 24-11. Flash Security States

SEC[1:0]	Status of Security
00	SECURED
01	SECURED ¹
10	UNSECURED
11	SECURED

¹ Preferred SEC state to set MCU to secured state.

Table 24-52. Set User Margin Level Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x0D	Flash block selection code [1:0]. See Table 24-32
001	Margin level setting.	

Upon clearing CCIF to launch the Set User Margin Level command, the Memory Controller will set the user margin level for the targeted block and then set the CCIF flag.

NOTE

When the EEPROM block is targeted, the EEPROM user margin levels are applied only to the EEPROM reads. However, when the P-Flash block is targeted, the P-Flash user margin levels are applied to both P-Flash and EEPROM reads. It is not possible to apply user margin levels to the P-Flash block only.

Valid margin level settings for the Set User Margin Level command are defined in [Table 24-53](#).

Table 24-53. Valid Set User Margin Level Settings

CCOB (CCOBIX=001)	Level Description
0x0000	Return to Normal Level
0x0001	User Margin-1 Level ¹
0x0002	User Margin-0 Level ²

¹ Read margin to the erased state

² Read margin to the programmed state

Table 24-54. Set User Margin Level Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 001 at command launch
		Set if command not available in current mode (see Table 24-25)
		Set if an invalid FlashBlockSelectionCode[1:0] is supplied (See Table 24-32)
		Set if an invalid margin level setting is supplied
	FPVIOL	None
	MGSTAT1	None
	MGSTAT0	None

Table 27-16. FERSTAT Field Descriptions

Field	Description
1 DFDIF	Double Bit Fault Detect Interrupt Flag — The setting of the DFDIF flag indicates that a double bit fault was detected in the stored parity and data bits during a Flash array read operation or that a Flash array read operation returning invalid data was attempted on a Flash block that was under a Flash command operation. ¹ The DFDIF flag is cleared by writing a 1 to DFDIF. Writing a 0 to DFDIF has no effect on DFDIF. ² 0 No double bit fault detected 1 Double bit fault detected or a Flash array read operation returning invalid data was attempted while command running
0 SFDIF	Single Bit Fault Detect Interrupt Flag — With the IGNSF bit in the FCNFG register clear, the SFDIF flag indicates that a single bit fault was detected in the stored parity and data bits during a Flash array read operation or that a Flash array read operation returning invalid data was attempted on a Flash block that was under a Flash command operation. ¹ The SFDIF flag is cleared by writing a 1 to SFDIF. Writing a 0 to SFDIF has no effect on SFDIF. 0 No single bit fault detected 1 Single bit fault detected and corrected or a Flash array read operation returning invalid data was attempted while command running

¹ The single bit fault and double bit fault flags are mutually exclusive for parity errors (an ECC fault occurrence can be either single fault or double fault but never both). A simultaneous access collision (Flash array read operation returning invalid data attempted while command running) is indicated when both SFDIF and DFDIF flags are high.

² There is a one cycle delay in storing the ECC DFDIF and SFDIF fault flags in this register. At least one NOP is required after a flash memory read before checking FERSTAT for the occurrence of ECC errors.

27.3.2.9 P-Flash Protection Register (FPROT)

The FPROT register defines which P-Flash sectors are protected against program and erase operations.

Offset Module Base + 0x0008

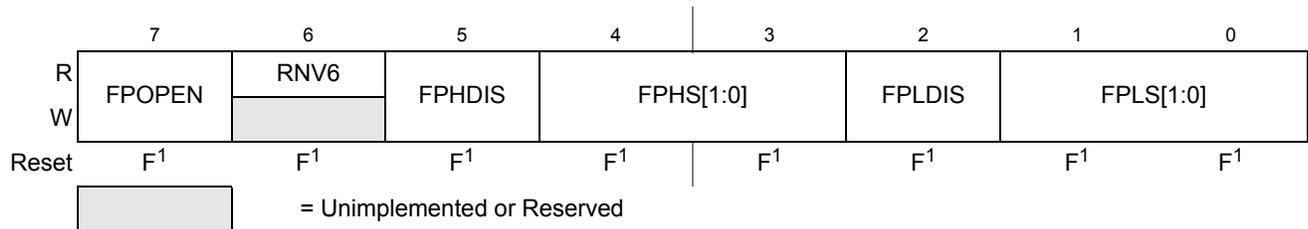


Figure 27-13. Flash Protection Register (FPROT)

¹ Loaded from IFR Flash configuration field, during reset sequence.

The (unreserved) bits of the FPROT register are writable with the restriction that the size of the protected region can only be increased (see [Section 27.3.2.9.1, “P-Flash Protection Restrictions,”](#) and [Table 27-21](#)).

During the reset sequence, the FPROT register is loaded with the contents of the P-Flash protection byte in the Flash configuration field at global address 0x3_FF0C located in P-Flash memory (see [Table 27-4](#)) as indicated by reset condition ‘F’ in [Figure 27-13](#). To change the P-Flash protection that will be loaded during the reset sequence, the upper sector of the P-Flash memory must be unprotected, then the P-Flash protection byte must be reprogrammed. If a double bit fault is detected while reading the P-Flash phrase containing the P-Flash protection byte during the reset sequence, the FPOPEN bit will be cleared and remaining bits in the FPROT register will be set to leave the P-Flash memory fully protected.

Offset Module Base + 0x0013

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 27-25. Flash Reserved7 Register (FRSV7)

All bits in the FRSV7 register read 0 and are not writable.

27.4 Functional Description

27.4.1 Modes of Operation

The FTMRG64K1 module provides the modes of operation normal and special . The operating mode is determined by module-level inputs and affects the FCLKDIV, FCNFG, and EEPROT registers (see [Table 27-27](#)).

27.4.2 IFR Version ID Word

The version ID word is stored in the IFR at address 0x0_40B6. The contents of the word are defined in [Table 27-26](#).

Table 27-26. IFR Version ID Fields

[15:4]	[3:0]
Reserved	VERNUM

28.3.2.2 Flash Security Register (FSEC)

The FSEC register holds all bits associated with the security of the MCU and Flash module.

Offset Module Base + 0x0001

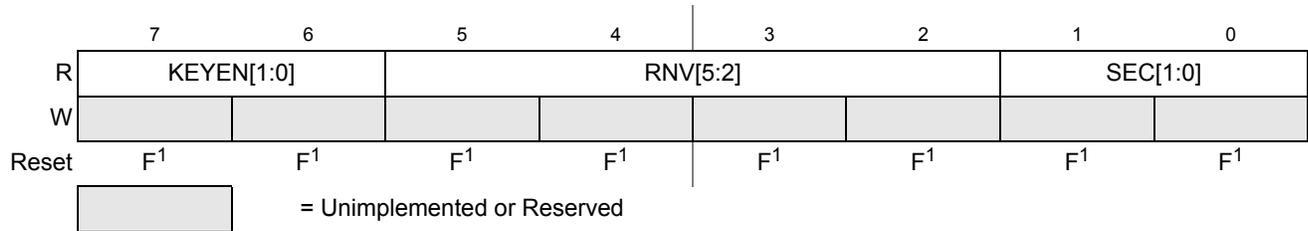


Figure 28-6. Flash Security Register (FSEC)

¹ Loaded from IFR Flash configuration field, during reset sequence.

All bits in the FSEC register are readable but not writable.

During the reset sequence, the FSEC register is loaded with the contents of the Flash security byte in the Flash configuration field at global address 0x3_FF0F located in P-Flash memory (see [Table 28-4](#)) as indicated by reset condition F in [Figure 28-6](#). If a double bit fault is detected while reading the P-Flash phrase containing the Flash security byte during the reset sequence, all bits in the FSEC register will be set to leave the Flash module in a secured state with backdoor key access disabled.

Table 28-9. FSEC Field Descriptions

Field	Description
7–6 KEYEN[1:0]	Backdoor Key Security Enable Bits — The KEYEN[1:0] bits define the enabling of backdoor key access to the Flash module as shown in Table 28-10 .
5–2 RNV[5:2]	Reserved Nonvolatile Bits — The RNV bits should remain in the erased state for future enhancements.
1–0 SEC[1:0]	Flash Security Bits — The SEC[1:0] bits define the security state of the MCU as shown in Table 28-11 . If the Flash module is unsecured using backdoor key access, the SEC bits are forced to 10.

Table 28-10. Flash KEYEN States

KEYEN[1:0]	Status of Backdoor Key Access
00	DISABLED
01	DISABLED ¹
10	ENABLED
11	DISABLED

¹ Preferred KEYEN state to disable backdoor key access.

- VERNUM: Version number. The first version is number 0b_0001 with both 0b_0000 and 0b_1111 meaning 'none'.

28.4.3 Internal NVM resource (NVMRES)

IFR is an internal NVM resource readable by CPU, when NVMRES is active. The IFR fields are shown in [Table 28-5](#).

The NVMRES global address map is shown in [Table 28-6](#).

28.4.4 Flash Command Operations

Flash command operations are used to modify Flash memory contents.

The next sections describe:

- How to write the FCLKDIV register that is used to generate a time base (FCLK) derived from BUSCLK for Flash program and erase command operations
- The command write sequence used to set Flash command parameters and launch execution
- Valid Flash commands available for execution, according to MCU functional mode and MCU security state.

28.4.4.1 Writing the FCLKDIV Register

Prior to issuing any Flash program or erase command after a reset, the user is required to write the FCLKDIV register to divide BUSCLK down to a target FCLK of 1 MHz. [Table 28-8](#) shows recommended values for the FDIV field based on BUSCLK frequency.

NOTE

Programming or erasing the Flash memory cannot be performed if the bus clock runs at less than 0.8 MHz. Setting FDIV too high can destroy the Flash memory due to overstress. Setting FDIV too low can result in incomplete programming or erasure of the Flash memory cells.

When the FCLKDIV register is written, the FDIVLD bit is set automatically. If the FDIVLD bit is 0, the FCLKDIV register has not been written since the last reset. If the FCLKDIV register has not been written, any Flash program or erase command loaded during a command write sequence will not execute and the ACCERR bit in the FSTAT register will set.

28.4.4.2 Command Write Sequence

The Memory Controller will launch all valid Flash commands entered using a command write sequence.

Before launching a command, the ACCERR and FPVIOL bits in the FSTAT register must be clear (see [Section 28.3.2.7](#)) and the CCIF flag should be tested to determine the status of the current command write sequence. If CCIF is 0, the previous command write sequence is still active, a new command write sequence cannot be started, and all writes to the FCCOB register are ignored.

Table 30-41. Program P-Flash Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 101 at command launch
		Set if command not available in current mode (see Table 30-27)
		Set if an invalid global address [17:0] is supplied see Table 30-3)
		Set if a misaligned phrase address is supplied (global address [2:0] != 000)
	FPVIOL	Set if the global address [17:0] points to a protected area
	MGSTAT1	Set if any errors have been encountered during the verify operation
MGSTAT0	Set if any non-correctable errors have been encountered during the verify operation	

30.4.6.6 Program Once Command

The Program Once command restricts programming to a reserved 64 byte field (8 phrases) in the nonvolatile information register located in P-Flash. The Program Once reserved field can be read using the Read Once command as described in [Section 30.4.6.4](#). The Program Once command must only be issued once since the nonvolatile information register in P-Flash cannot be erased. The Program Once command must not be executed from the Flash block containing the Program Once reserved field to avoid code runaway.

Table 30-42. Program Once Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x07	Not Required
001	Program Once phrase index (0x0000 - 0x0007)	
010	Program Once word 0 value	
011	Program Once word 1 value	
100	Program Once word 2 value	
101	Program Once word 3 value	

Upon clearing CCIF to launch the Program Once command, the Memory Controller first verifies that the selected phrase is erased. If erased, then the selected phrase will be programmed and then verified with read back. The CCIF flag will remain clear, setting only after the Program Once operation has completed.

The reserved nonvolatile information register accessed by the Program Once command cannot be erased and any attempt to program one of these phrases a second time will not be allowed. Valid phrase index values for the Program Once command range from 0x0000 to 0x0007. During execution of the Program Once command, any attempt to read addresses within P-Flash will return invalid data.

Table 31-49. Erase P-Flash Sector Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 001 at command launch
		Set if command not available in current mode (see Table 31-27)
		Set if an invalid global address [17:16] is supplied see Table 31-3)
		Set if a misaligned phrase address is supplied (global address [2:0] != 000)
	FPVIOL	Set if the selected P-Flash sector is protected
	MGSTAT1	Set if any errors have been encountered during the verify operation
MGSTAT0	Set if any non-correctable errors have been encountered during the verify operation	

31.4.6.10 Unsecure Flash Command

The Unsecure Flash command will erase the entire P-Flash and EEPROM memory space and, if the erase is successful, will release security.

Table 31-50. Unsecure Flash Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x0B	Not required

Upon clearing CCIF to launch the Unsecure Flash command, the Memory Controller will erase the entire P-Flash and EEPROM memory space and verify that it is erased. If the Memory Controller verifies that the entire Flash memory space was properly erased, security will be released. If the erase verify is not successful, the Unsecure Flash operation sets MGSTAT1 and terminates without changing the security state. During the execution of this command (CCIF=0) the user must not write to any Flash module register. The CCIF flag is set after the Unsecure Flash operation has completed.

Table 31-51. Unsecure Flash Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 000 at command launch
		Set if command not available in current mode (see Table 31-27)
	FPVIOL	Set if any area of the P-Flash or EEPROM memory is protected
	MGSTAT1	Set if any errors have been encountered during the verify operation
	MGSTAT0	Set if any non-correctable errors have been encountered during the verify operation

31.4.6.11 Verify Backdoor Access Key Command

The Verify Backdoor Access Key command will only execute if it is enabled by the KEYEN bits in the FSEC register (see [Table 31-10](#)). The Verify Backdoor Access Key command releases security if user-supplied keys match those stored in the Flash security bytes of the Flash configuration field (see

0x0240–0x025F Port Integration Module (PIM) Map 4 of 6

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0254	PERM	R	0	0	0	0	PERM3	PERM2	PERM1	PERM0
		W								
0x0255	PPSM	R	0	0	0	0	PPSM3	PPSM2	PPSM1	PPSM0
		W								
0x0256	WOMM	R	0	0	0	0	WOMM3	WOMM2	WOMM1	WOMM0
		W								
0x0257	PKGCR	R	APICLK7	0	0	0	0	PKGCR2	PKGCR1	PKGCR0
		W								
0x0258	PTP	R	PTP7	PTP6	PTP5	PTP4	PTP3	PTP2	PTP1	PTP0
		W								
0x0259	PTIP	R	PTIP7	PTIP6	PTIP5	PTIP4	PTIP3	PTIP2	PTIP1	PTIP0
		W								
0x025A	DDRP	R	DDRP7	DDRP6	DDRP5	DDRP4	DDRP3	DDRP2	DDRP1	DDRP0
		W								
0x025B	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x025C	PERP	R	PERP7	PERP6	PERP5	PERP4	PERP3	PERP2	PERP1	PERP0
		W								
0x025D	PPSP	R	PPSP7	PPSP6	PPSP5	PPSP4	PPSP3	PPSP2	PPSP1	PPSP0
		W								
0x025E	PIEP	R	PIEP7	PIEP6	PIEP5	PIEP4	PIEP3	PIEP2	PIEP1	PIEP0
		W								
0x025F	PIFP	R	PIFP7	PIFP6	PIFP5	PIFP4	PIFP3	PIFP2	PIFP1	PIFP0
		W								

0x0260–0x0261 Analog Comparator(ACMP)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0260	ACMPC	W								
		R	ACIE	ACOPE	ACICE	0	ACMOD1	ACMOD0	0	ACE
0x0261	ACMPS	R	ACIF	ACO	0	0	0	0	0	0
		W								

0x0262–0x0275 Port Integration Module (PIM) Map 5 of 6

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0262- 0x0267	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0267	Reserved	R	Reserved	Reserved	0	0	0	0	0	Reserved
		W								
0x0268	PTJ	R	PTJ7	PTJ6	PTJ5	PTJ4	PTJ3	PTJ2	PTJ1	PTJ0
		W								
0x0269	PTIJ	R	PTIJ7	PTIJ6	PTIJ5	PTIJ4	PTIJ3	PTIJ2	PTIJ1	PTIJ0
		W								