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Details

Product Status	Active
Core Processor	12V1
Core Size	16-Bit
Speed	25MHz
Connectivity	CANbus, IrDA, LINbus, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	40
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3.13V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s9s12g64f0vlfr

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Table 1-13. 48-Pin LQFP Pinout for S12GN48

Package Pin	Function <----lowest-----PRIORITY-----highest---->					Power Supply	Internal Pull Resistor	
	Pin	2nd Func.	3rd Func.	4th Func	5th Func		CTRL	Reset State
28	PAD9	KWAD9	AN9	ACMPO	—	V _{DDA}	PER0AD/PPS0AD	Disabled
29	PAD2	KWAD2	AN2	—	—	V _{DDA}	PER1AD/PPS1AD	Disabled
30	PAD10	KWAD10	AN10	ACMPPI		V _{DDA}	PER0AD/PPS0AD	Disabled
31	PAD3	KWAD3	AN3	—	—	V _{DDA}	PER1AD/PPS1AD	Disabled
32	PAD11	KWAD11	AN11	ACMPPI		V _{DDA}	PER0AD/PPS0AD	Disabled
33	PAD4	KWAD4	AN4	—	—	V _{DDA}	PER1AD/PPS1AD	Disabled
34	PAD5	KWAD5	AN5	—	—	V _{DDA}	PER1AD/PPS0AD	Disabled
35	PAD6	KWAD6	AN6	—	—	V _{DDA}	PER1AD/PPS1AD	Disabled
36	PAD7	KWAD7	AN7	—	—	V _{DDA}	PER1AD/PPS1AD	Disabled
37	VDDA	VRH	—	—	—	—	—	—
38	VSSA	—	—	—	—	—	—	—
39	PS0	RXD0	—	—	—	V _{DDX}	PERS/PPSS	Up
40	PS1	TXD0	—	—	—	V _{DDX}	PERS/PPSS	Up
41	PS2	RXD1	—	—	—	V _{DDX}	PERS/PPSS	Up
42	PS3	TXD1	—	—	—	V _{DDX}	PERS/PPSS	Up
43	PS4	MISO0	—	—	—	V _{DDX}	PERS/PPSS	Up
44	PS5	MOSI0	—	—	—	V _{DDX}	PERS/PPSS	Up
45	PS6	SCK0	—	—	—	V _{DDX}	PERS/PPSS	Up
46	PS7	API_EXTC LK	ECLK	$\overline{SS0}$	—	V _{DDX}	PERS/PPSS	Up
47	PM0	—	—	—	—	V _{DDX}	PERM/PPSM	Disabled
48	PM1	—	—	—	—	V _{DDX}	PERM/PPSM	Disabled

¹ The regular I/O characteristics (see [Section A.2, “I/O Characteristics”](#)) apply if the EXTAL/XTAL function is disabled

1.17 ADC Result Reference

MCUs of the S12G-Family are able to measure the internal reference voltage V_{DDF} (see [Table 1-38](#)). V_{DDF} is a constant voltage with a narrow distribution over temperature and external voltage supply (see [Table A-47](#)).

A 12-bit left justified¹ ADC conversion result of V_{DDF} is provided at address 0x0_4022/0x0_4023 in the NVM's IFR for reference. The measurement conditions of the reference conversion are listed in [Section A.16, "ADC Conversion Result Reference"](#). By measuring the voltage V_{DDF} (see [Table 1-38](#)) and comparing the result to the reference value in the IFR, it is possible to determine the ADC's reference voltage V_{RH} in the application environment:

$$V_{RH} = \frac{\text{StoredReference}}{\text{ConvertedReference}} \cdot 5V$$

The exact absolute value of an analog conversion can be determined as follows:

$$\text{Result} = \text{ConvertedADInput} \cdot \frac{\text{StoredReference} \cdot 5V}{\text{ConvertedReference} \cdot 2^n}$$

With:

ConvertedADInput:	Result of the analog to digital conversion of the desired pin
ConvertedReference:	Result of channel "Internal_0" conversion
StoredReference:	Value in IFR locatio 0x0_4022/0x0_4023
n:	ADC resolution (10 bit)

CAUTION

To assure high accuracy of the V_{DDF} reference conversion, the NVMs must not be programmed, erased, or read while the conversion takes place. This implies that code must be executed from RAM. The "ConvertedReference" value must be the average of eight consecutive conversions.

CAUTION

The ADC's reference voltage V_{RH} must remain at a constant level throughout the conversion process.

1.18 ADC VRH/VRL Signal Connection

On all S12G devices except for the S12GA192 and the S12GA240 the external VRH signal is directly connected to the ADC's VRH signal input. The ADC's VRL input is connected to VSSA. (see [Figure 1-27](#)).

1. The format of the stored V_{DDF} reference value is still subject to change.

Table 2-18. Block Memory Map (0x0000-0x027F) (continued)

Port	Global Address	Register	Access	Reset Value	Section/Page
T	0x0240	PTT—Port T Data Register	R/W	0x00	2.4.3.15/2-207
	0x0241	PTIT—Port T Input Register	R	³	2.4.3.16/2-207
	0x0242	DDRT—Port T Data Direction Register	R/W	0x00	2.4.3.17/2-208
	0x0243	Reserved	R	0x00	
	0x0244	PERT—Port T Pull Device Enable Register	R/W	0x00	2.4.3.18/2-209
	0x0245	PPST—Port T Polarity Select Register	R/W	0x00	2.4.3.19/2-210
	0x0246	Reserved	R	0x00	
	0x0247	Reserved	R	0x00	
S	0x0248	PTS—Port S Data Register	R/W	0x00	2.4.3.20/2-210
	0x0249	PTIS—Port S Input Register	R	³	2.4.3.21/2-211
	0x024A	DDRS—Port S Data Direction Register	R/W	0x00	2.4.3.22/2-211
	0x024B	Reserved	R	0x00	
	0x024C	PERS—Port S Pull Device Enable Register	R/W	0xFF	2.4.3.23/2-212
	0x024D	PPSS—Port S Polarity Select Register	R/W	0x00	2.4.3.24/2-212
	0x024E	WOMS—Port S Wired-Or Mode Register	R/W	0x00	2.4.3.25/2-213
	0x024F	PRR0—Pin Routing Register 0 ⁴	R/W	0x00	2.4.3.26/2-213
M	0x0250	PTM—Port M Data Register	R/W	0x00	2.4.3.27/2-215
	0x0251	PTIM—Port M Input Register	R	³	2.4.3.29/2-216
	0x0252	DDRM—Port M Data Direction Register	R/W	0x00	2.4.3.29/2-216
	0x0253	Reserved	R	0x00	
	0x0254	PERM—Port M Pull Device Enable Register	R/W	0x00	2.4.3.30/2-217
	0x0255	PPSM—Port M Polarity Select Register	R/W	0x00	2.4.3.31/2-218
	0x0256	WOMM—Port M Wired-Or Mode Register	R/W	0x00	2.4.3.32/2-218
	0x0257	PKGCR—Package Code Register	R/W	⁵	2.4.3.33/2-219
P	0x0258	PTP—Port P Data Register	R/W	0x00	2.4.3.34/2-220
	0x0259	PTIP—Port P Input Register	R	³	2.4.3.35/2-221
	0x025A	DDRP—Port P Data Direction Register	R/W	0x00	2.4.3.36/2-222
	0x025B	Reserved	R	0x00	
	0x025C	PERP—Port P Pull Device Enable Register	R/W	0x00	2.4.3.37/2-222
	0x025D	PPSP—Port P Polarity Select Register	R/W	0x00	2.4.3.38/2-223
	0x025E	PIEP—Port P Interrupt Enable Register	R/W	0x00	2.4.3.39/2-224
	0x025F	PIFP—Port P Interrupt Flag Register	R/W	0x00	2.4.3.40/2-224

2.4.3.4 Port B Data Direction Register (DDRB)

Address 0x0003 (G1)

Access: User read/write¹

	7	6	5	4	3	2	1	0
R	DDRB7	DDRB6	DDRB5	DDRB4	DDRB3	DDRB2	DDRB1	DDRB0
W								
Reset	0	0	0	0	0	0	0	0

Address 0x0003 (G2, G3)

Access: User read only

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

Figure 2-5. Port B Data Direction Register (DDRB)

¹ Read: Anytime
Write: Anytime

Table 2-25. DDRB Register Field Descriptions

Field	Description
7-0 DDRB	Port B Data Direction— This bit determines whether the associated pin is an input or output. 1 Associated pin configured as output 0 Associated pin configured as input

2.4.3.5 Port C Data Register (PORTC)

Address 0x0004 (G1)

Access: User read/write¹

	7	6	5	4	3	2	1	0
R	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
W								
Reset	0	0	0	0	0	0	0	0

Address 0x0004 (G2, G3)

Access: User read only

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

Figure 2-6. Port C Data Register (PORTC)

¹ Read: Anytime. The data source is depending on the data direction value.
Write: Anytime

2.4.3.43 Port J Input Register (PTIJ)

Address 0x0269 (G1, G2)

Access: User read only¹

	7	6	5	4	3	2	1	0
R	PTIJ7	PTIJ6	PTIJ5	PTIJ4	PTIJ3	PTIJ2	PTIJ1	PTIJ0
W								
Reset	0	0	0	0	0	0	0	0

Address 0x0269 (G3)

Access: User read only¹

	7	6	5	4	3	2	1	0
R	0	0	0	0	PTIJ3	PTIJ2	PTIJ1	PTIJ0
W								
Reset	0	0	0	0	0	0	0	0

Figure 2-43. Port J Input Register (PTIJ)

¹ Read: Anytime
Write: Never

Table 2-69. PTIJ Register Field Descriptions

Field	Description
7-0 PTIJ	Port J input data— A read always returns the buffered input state of the associated pin. It can be used to detect overload or short circuit conditions on output pins.

2.4.3.44 Port J Data Direction Register (DDRJ)

Address 0x026A (G1, G2)

Access: User read/write¹

	7	6	5	4	3	2	1	0
R	DDRJ7	DDRJ6	DDRJ5	DDRJ4	DDRJ3	DDRJ2	DDRJ1	DDRJ0
W								
Reset	0	0	0	0	0	0	0	0

Address 0x026A (G3)

Access: User read/write¹

	7	6	5	4	3	2	1	0
R	0	0	0	0	DDRJ3	DDRJ2	DDRJ1	DDRJ0
W								
Reset	0	0	0	0	0	0	0	0

Figure 2-44. Port J Data Direction Register (DDRJ)

¹ Read: Anytime
Write: Anytime

2.5 PIM Ports - Functional Description

2.5.1 General

Each pin except BKGD can act as general-purpose I/O. In addition most pins can act as an output or input of a peripheral module.

2.5.2 Registers

A set of configuration registers is common to all ports with exception of the ADC port (Table 2-91). All registers can be written at any time, however a specific configuration might not become active.

Example: Selecting a pullup device. This device does not become active while the port is used as a push-pull output.

Table 2-91. Register availability per port¹

Port	Data (Portx, PTx)	Input (PTIx)	Data Direction (DDRx)	Pull Enable (PERx)	Polarity Select (PPSx)	Wired-Or Mode (WOMx)	Interrupt Enable (PIEx)	Interrupt Flag (PIFx)
A	yes	-	yes	yes	-	-	-	-
B	yes	-	yes		-	-	-	-
C	yes	-	yes		-	-	-	-
D	yes	-	yes		-	-	-	-
E	yes	-	yes		-	-	-	-
T	yes	yes	yes	yes	yes	-	-	-
S	yes	yes	yes	yes	yes	yes	-	-
M	yes	yes	yes	yes	yes	yes	-	-
P	yes	yes	yes	yes	yes	-	yes	yes
J	yes	yes	yes	yes	yes	-	yes	yes
AD	yes	yes	yes	yes	yes	-	yes	yes

¹ Each cell represents one register with individual configuration bits

2.5.2.1 Data Register (PORTx, PTx)

This register holds the value driven out to the pin if the pin is used as a general-purpose I/O.

Writing to this register has only an effect on the pin if the pin is used as general-purpose output. When reading this address, the buffered state of the pin is returned if the associated data direction register bit is set to 0.

If the data direction register bits are set to 1, the contents of the data register is returned. This is independent of any other configuration (Figure 2-64).

2.5.2.2 Input Register (PTIx)

This register is read-only and always returns the buffered state of the pin (Figure 2-64).

Write: All modes through BDM operation when not secured

NOTE

When BDM is made active, the CPU stores the content of its CCR register in the BDMCCR register. However, out of special single-chip reset, the BDMCCR is set to 0xD8 and not 0xD0 which is the reset value of the CCR register in this CPU mode. Out of reset in all other modes the BDMCCR register is read zero.

When entering background debug mode, the BDM CCR holding register is used to save the condition code register of the user's program. It is also used for temporary storage in the standard BDM firmware mode. The BDM CCR holding register can be written to modify the CCR value.

7.3.2.2 BDM Program Page Index Register (BDMPPR)

Register Global Address 0x3_FF08

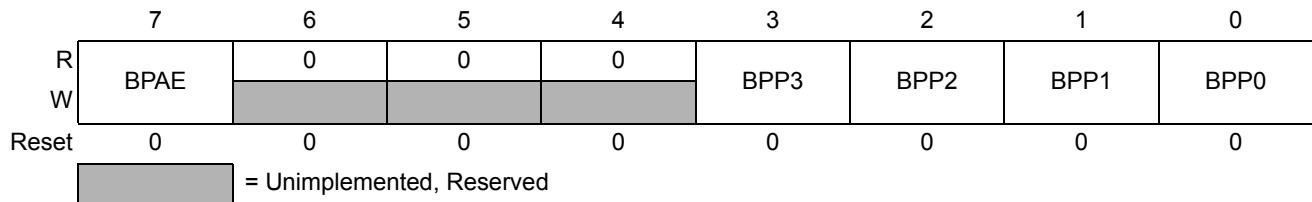


Figure 7-5. BDM Program Page Register (BDMPPR)

Read: All modes through BDM operation when not secured

Write: All modes through BDM operation when not secured

Table 7-4. BDMPPR Field Descriptions

Field	Description
7 BPAE	BDM Program Page Access Enable Bit — BPAE enables program page access for BDM hardware and firmware read/write instructions. The BDM hardware commands used to access the BDM registers (READ_BD and WRITE_BD) can not be used for program page accesses even if the BPAE bit is set. 0 BDM Program Paging disabled 1 BDM Program Paging enabled
3–0 BPP[3:0]	BDM Program Page Index Bits 3–0 — These bits define the selected program page. For more detailed information regarding the program page window scheme, please refer to the S12S_MMC Block Guide.

7.3.3 Family ID Assignment

The family ID is an 8-bit value located in the BDM ROM in active BDM (at global address: 0x3_FF0F). The read-only value is a unique family ID which is 0xC2 for devices with an HCS12S core.

7.4 Functional Description

The BDM receives and executes commands from a host via a single wire serial interface. There are two types of BDM commands: hardware and firmware commands.

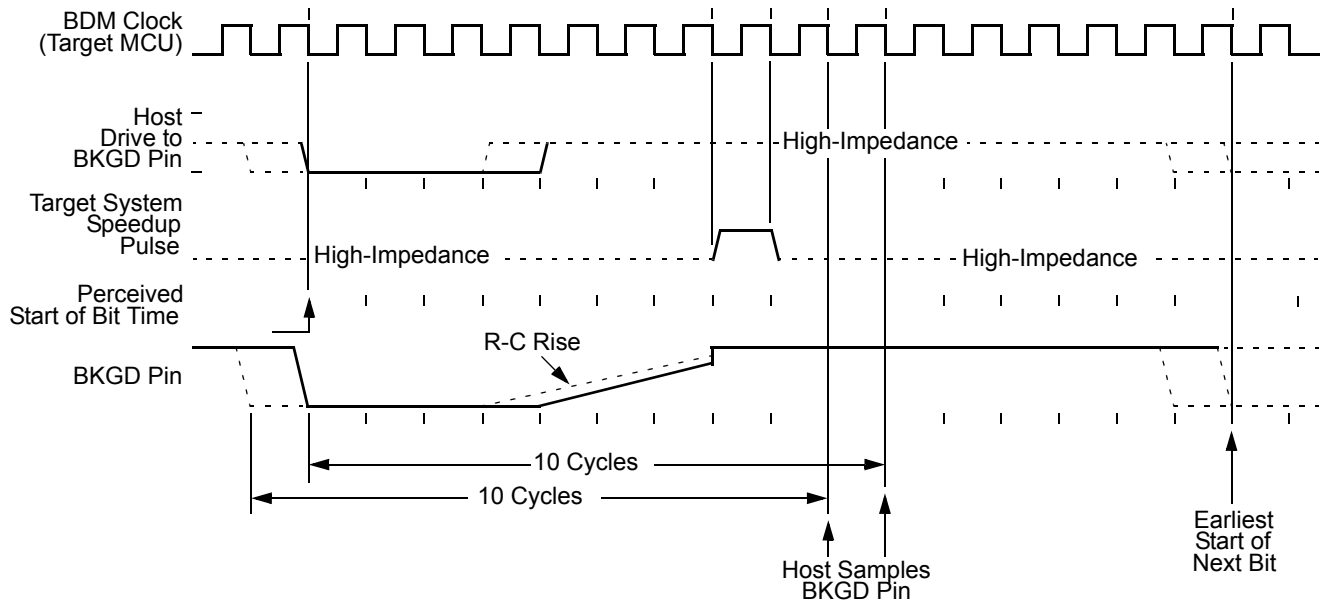


Figure 7-8. BDM Target-to-Host Serial Bit Timing (Logic 1)

Figure 7-9 shows the host receiving a logic 0 from the target. Since the host is asynchronous to the target, there is up to a one clock-cycle delay from the host-generated falling edge on BKGD to the start of the bit time as perceived by the target. The host initiates the bit time but the target finishes it. Since the target wants the host to receive a logic 0, it drives the BKGD pin low for 13 target clock cycles then briefly drives it high to speed up the rising edge. The host samples the bit level about 10 target clock cycles after starting the bit time.

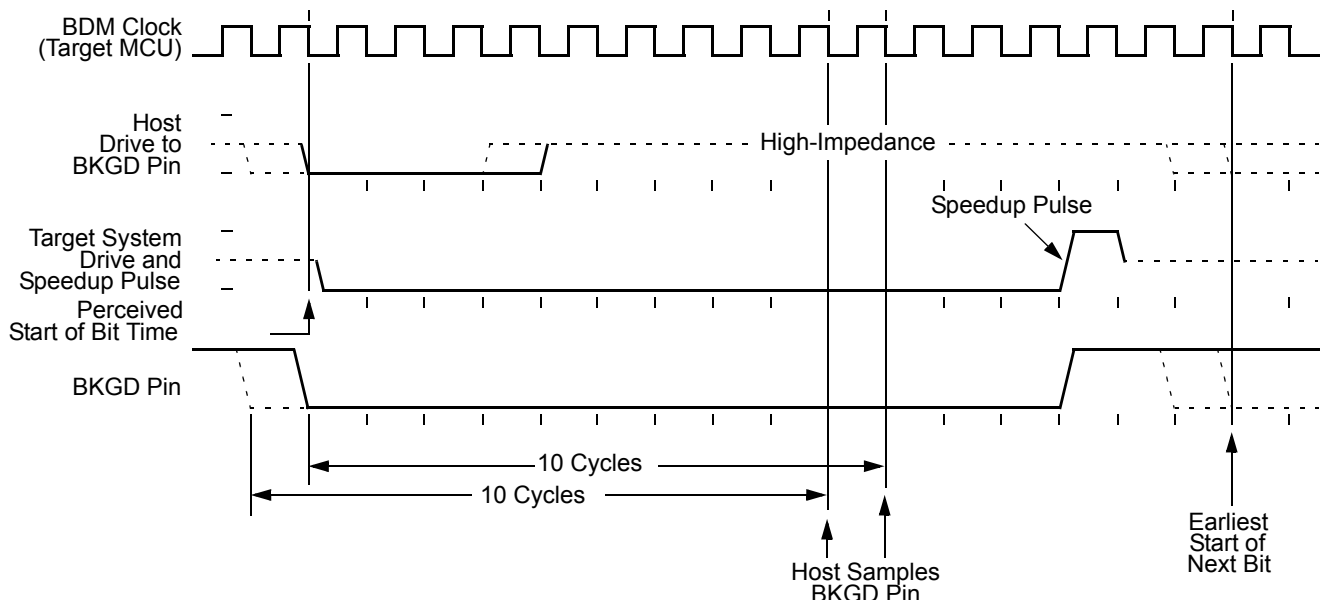


Figure 7-9. BDM Target-to-Host Serial Bit Timing (Logic 0)

edge or level sensitive with polarity control. Table 15-23 gives a brief description of the different combinations of control bits and their effect on the external trigger function.

In order to avoid maybe false trigger events please enable the external digital input via ATDDIEN register first and in the following enable the external trigger mode by bit ETRIGE.

Table 15-23. External Trigger Control Bits

ETRIGLE	ETRIGP	ETRIGE	SCAN	Description
X	X	0	0	Ignores external trigger. Performs one conversion sequence and stops.
X	X	0	1	Ignores external trigger. Performs continuous conversion sequences.
0	0	1	X	Trigger falling edge sensitive. Performs one conversion sequence per trigger.
0	1	1	X	Trigger rising edge sensitive. Performs one conversion sequence per trigger.
1	0	1	X	Trigger low level sensitive. Performs continuous conversions while trigger level is active.
1	1	1	X	Trigger high level sensitive. Performs continuous conversions while trigger level is active.

In either level or edge sensitive mode, the first conversion begins when the trigger is received.

Once ETRIGE is enabled a conversion must be triggered externally after writing to ATDCTL5 register.

During a conversion in edge sensitive mode, if additional trigger events are detected the overrun error flag ETORF is set.

If level sensitive mode is active and the external trigger de-asserts and later asserts again during a conversion sequence, this does not constitute an overrun. Therefore, the flag is not set. If the trigger is left active in level sensitive mode when a sequence is about to complete, another sequence will be triggered immediately.

15.4.2.2 General-Purpose Digital Port Operation

Each ATD input pin can be switched between analog or digital input functionality. An analog multiplexer makes each ATD input pin selected as analog input available to the A/D converter.

The pad of the ATD input pin is always connected to the analog input channel of the analog multiplexer.

Each pad input signal is buffered to the digital port register.

This buffer can be turned on or off with the ATDDIEN register for each ATD input pin.

This is important so that the buffer does not draw excess current when an ATD input pin is selected as analog input to the ADC10B16C.

Clock A is used as an input to an 8-bit down counter. This down counter loads a user programmable scale value from the scale register (PWMSCLA). When the down counter reaches one, a pulse is output and the 8-bit counter is re-loaded. The output signal from this circuit is further divided by two. This gives a greater range with only a slight reduction in granularity. Clock SA equals clock A divided by two times the value in the PWMSCLA register.

NOTE

$$\text{Clock SA} = \text{Clock A} / (2 * \text{PWMSCLA})$$

When PWMSCLA = \$00, PWMSCLA value is considered a full scale value of 256. Clock A is thus divided by 512.

Similarly, clock B is used as an input to an 8-bit down counter followed by a divide by two producing clock SB. Thus, clock SB equals clock B divided by two times the value in the PWMSCLB register.

NOTE

$$\text{Clock SB} = \text{Clock B} / (2 * \text{PWMSCLB})$$

When PWMSCLB = \$00, PWMSCLB value is considered a full scale value of 256. Clock B is thus divided by 512.

As an example, consider the case in which the user writes \$FF into the PWMSCLA register. Clock A for this case will be E (bus clock) divided by 4. A pulse will occur at a rate of once every 255×4 E cycles. Passing this through the divide by two circuit produces a clock signal at an E divided by 2040 rate. Similarly, a value of \$01 in the PWMSCLA register when clock A is E divided by 4 will produce a clock at an E divided by 8 rate.

Writing to PWMSCLA or PWMSCLB causes the associated 8-bit down counter to be re-loaded. Otherwise, when changing rates the counter would have to count down to \$01 before counting at the proper rate. Forcing the associated counter to re-load the scale register value every time PWMSCLA or PWMSCLB is written prevents this.

NOTE

Writing to the scale registers while channels are operating can cause irregularities in the PWM outputs.

19.4.1.3 Clock Select

Each PWM channel has the capability of selecting one of four clocks, clock A, clock SA, clock B or clock SB. The clock selection is done with the PCLKx control bits in the PWMCLK register and PCLKABx control bits in PWMCLKAB register. For backward compatibility consideration, the reset value of PWMCLK and PWMCLKAB configures following default clock selection.

For channels 0, 1, 4, and 5 the clock choices are clock A.

For channels 2, 3, 6, and 7 the clock choices are clock B.

NOTE

Changing clock control bits while channels are operating can cause irregularities in the PWM outputs.

indicating that the received byte can be read. If the receive interrupt enable bit, RIE, in SCI control register 2 (SCICR2) is also set, the RDRF flag generates an RDRF interrupt request.

20.4.6.3 Data Sampling

The RT clock rate. The RT clock is an internal signal with a frequency 16 times the baud rate. To adjust for baud rate mismatch, the RT clock (see [Figure 20-21](#)) is re-synchronized:

- After every start bit
- After the receiver detects a data bit change from logic 1 to logic 0 (after the majority of data bit samples at RT8, RT9, and RT10 returns a valid logic 1 and the majority of the next RT8, RT9, and RT10 samples returns a valid logic 0)

To locate the start bit, data recovery logic does an asynchronous search for a logic 0 preceded by three logic 1s. When the falling edge of a possible start bit occurs, the RT clock begins to count to 16.

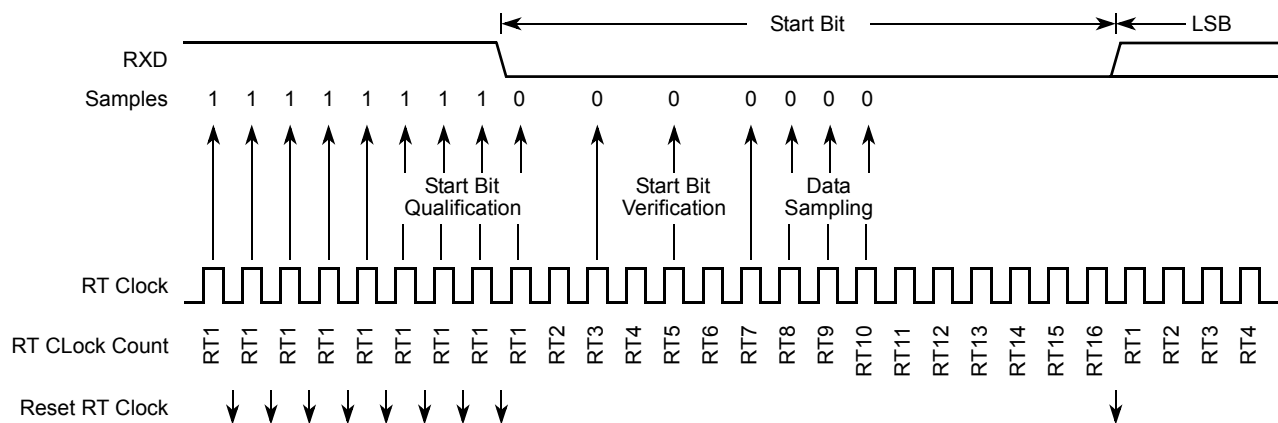


Figure 20-21. Receiver Data Sampling

To verify the start bit and to detect noise, data recovery logic takes samples at RT3, RT5, and RT7. [Figure 20-17](#) summarizes the results of the start bit verification samples.

Table 20-17. Start Bit Verification

RT3, RT5, and RT7 Samples	Start Bit Verification	Noise Flag
000	Yes	0
001	Yes	1
010	Yes	1
011	No	0
100	Yes	1
101	No	0
110	No	0
111	No	0

If start bit verification is not successful, the RT clock is reset and a new search for a start bit begins.

Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0005 SPIDRL	R	R7	R6	R5	R4	R3	R2	R1	R0
	W	T7	T6	T5	T4	T3	T2	T1	T0
0x0006 Reserved	R								
	W								
0x0007 Reserved	R								
	W								

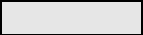
 = Unimplemented or Reserved

Figure 21-2. SPI Register Summary

21.3.2 Register Descriptions

This section consists of register descriptions in address order. Each description includes a standard register diagram with an associated figure number. Details of register bit and field function follow the register diagrams, in bit order.

21.3.2.1 SPI Control Register 1 (SPICR1)

Module Base +0x0000

	7	6	5	4	3	2	1	0
R	SPIE	SPE	SPTIE	MSTR	CPOL	CPHA	SSOE	LSBFE
W								
Reset	0	0	0	0	0	1	0	0

Figure 21-3. SPI Control Register 1 (SPICR1)

Read: Anytime

Write: Anytime

Table 21-1. SPICR1 Field Descriptions

Field	Description
7 SPIE	SPI Interrupt Enable Bit — This bit enables SPI interrupt requests, if SPIF or MODF status flag is set. 0 SPI interrupts disabled. 1 SPI interrupts enabled.
6 SPE	SPI System Enable Bit — This bit enables the SPI system and dedicates the SPI port pins to SPI system functions. If SPE is cleared, SPI is disabled and forced into idle state, status bits in SPISR register are reset. 0 SPI disabled (lower power consumption). 1 SPI enabled, port pins are dedicated to SPI functions.
5 SPTIE	SPI Transmit Interrupt Enable — This bit enables SPI interrupt requests, if SPTEF flag is set. 0 SPTEF interrupt disabled. 1 SPTEF interrupt enabled.

Table 25-63. Program EEPROM Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] < 010 at command launch
		Set if CCOBIX[2:0] > 101 at command launch
		Set if command not available in current mode (see Table 25-27)
		Set if an invalid global address [17:0] is supplied
		Set if a misaligned word address is supplied (global address [0] != 0)
		Set if the requested group of words breaches the end of the EEPROM block
	FPVIOL	Set if the selected area of the EEPROM memory is protected
	MGSTAT1	Set if any errors have been encountered during the verify operation
	MGSTAT0	Set if any non-correctable errors have been encountered during the verify operation

25.4.6.16 Erase EEPROM Sector Command

The Erase EEPROM Sector operation will erase all addresses in a sector of the EEPROM block.

Table 25-64. Erase EEPROM Sector Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x12	Global address [17:16] to identify EEPROM block
001	Global address [15:0] anywhere within the sector to be erased. See Section 25.1.2.2 for EEPROM sector size.	

Upon clearing CCIF to launch the Erase EEPROM Sector command, the Memory Controller will erase the selected Flash sector and verify that it is erased. The CCIF flag will set after the Erase EEPROM Sector operation has completed.

Table 25-65. Erase EEPROM Sector Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 001 at command launch
		Set if command not available in current mode (see Table 25-27)
		Set if an invalid global address [17:0] is suppliedsee Table 25-3)
		Set if a misaligned word address is supplied (global address [0] != 0)
	FPVIOL	Set if the selected area of the EEPROM memory is protected
	MGSTAT1	Set if any errors have been encountered during the verify operation
	MGSTAT0	Set if any non-correctable errors have been encountered during the verify operation

Table 26-19. P-Flash Protection Higher Address Range

FPHS[1:0]	Global Address Range	Protected Size
00	0x3_F800–0x3_FFFF	2 Kbytes
01	0x3_F000–0x3_FFFF	4 Kbytes
10	0x3_E000–0x3_FFFF	8 Kbytes
11	0x3_C000–0x3_FFFF	16 Kbytes

Table 26-20. P-Flash Protection Lower Address Range

FPLS[1:0]	Global Address Range	Protected Size
00	0x3_8000–0x3_83FF	1 Kbyte
01	0x3_8000–0x3_87FF	2 Kbytes
10	0x3_8000–0x3_8FFF	4 Kbytes
11	0x3_8000–0x3_9FFF	8 Kbytes

All possible P-Flash protection scenarios are shown in [Figure 26-14](#) . Although the protection scheme is loaded from the Flash memory at global address 0x3_FF0C during the reset sequence, it can be changed by the user. The P-Flash protection scheme can be used by applications requiring reprogramming in single chip mode while providing as much protection as possible if reprogramming is not required.

The user code stored in the P-Flash memory must have a method of receiving the backdoor keys from an external stimulus. This external stimulus would typically be through one of the on-chip serial ports.

If the KEYEN[1:0] bits are in the enabled state (see [Section 26.3.2.2](#)), the MCU can be unsecured by the backdoor key access sequence described below:

1. Follow the command sequence for the Verify Backdoor Access Key command as explained in [Section 26.4.6.11](#)
2. If the Verify Backdoor Access Key command is successful, the MCU is unsecured and the SEC[1:0] bits in the FSEC register are forced to the unsecure state of 10

The Verify Backdoor Access Key command is monitored by the Memory Controller and an illegal key will prohibit future use of the Verify Backdoor Access Key command. A reset of the MCU is the only method to re-enable the Verify Backdoor Access Key command. The security as defined in the Flash security byte (0x3_FF0F) is not changed by using the Verify Backdoor Access Key command sequence. The backdoor keys stored in addresses 0x3_FF00-0x3_FF07 are unaffected by the Verify Backdoor Access Key command sequence. The Verify Backdoor Access Key command sequence has no effect on the program and erase protections defined in the Flash protection register, FPROT.

After the backdoor keys have been correctly matched, the MCU will be unsecured. After the MCU is unsecured, the sector containing the Flash security byte can be erased and the Flash security byte can be reprogrammed to the unsecure state, if desired. In the unsecure state, the user has full control of the contents of the backdoor keys by programming addresses 0x3_FF00-0x3_FF07 in the Flash configuration field.

26.5.2 Unsecuring the MCU in Special Single Chip Mode using BDM

A secured MCU can be unsecured in special single chip mode by using the following method to erase the P-Flash and EEPROM memory:

1. Reset the MCU into special single chip mode
2. Delay while the BDM executes the Erase Verify All Blocks command write sequence to check if the P-Flash and EEPROM memories are erased
3. Send BDM commands to disable protection in the P-Flash and EEPROM memory
4. Execute the Erase All Blocks command write sequence to erase the P-Flash and EEPROM memory. Alternatively the Unsecure Flash command can be executed, if so the steps 5 and 6 below are skipped.
5. After the CCIF flag sets to indicate that the Erase All Blocks operation has completed, reset the MCU into special single chip mode
6. Delay while the BDM executes the Erase Verify All Blocks command write sequence to verify that the P-Flash and EEPROM memory are erased

If the P-Flash and EEPROM memory are verified as erased, the MCU will be unsecured. All BDM commands will now be enabled and the Flash security byte may be programmed to the unsecure state by continuing with the following steps:

7. Send BDM commands to execute the Program P-Flash command write sequence to program the Flash security byte to the unsecured state

Table 28-11. Flash Security States

SEC[1:0]	Status of Security
00	SECURED
01	SECURED ¹
10	UNSECURED
11	SECURED

¹ Preferred SEC state to set MCU to secured state.

The security function in the Flash module is described in [Section 28.5](#).

28.3.2.3 Flash CCOB Index Register (FCCOBIX)

The FCCOBIX register is used to index the FCCOB register for Flash memory operations.

Offset Module Base + 0x0002

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	CCOBIX[2:0]		
W								
Reset	0	0	0	0	0	0	0	0


 = Unimplemented or Reserved

Figure 28-7. FCCOB Index Register (FCCOBIX)

CCOBIX bits are readable and writable while remaining bits read 0 and are not writable.

Table 28-12. FCCOBIX Field Descriptions

Field	Description
2–0 CCOBIX[1:0]	Common Command Register Index — The CCOBIX bits are used to select which word of the FCCOB register array is being read or written to. See 28.3.2.11 Flash Common Command Object Register (FCCOB),” for more details.

28.3.2.4 Flash Reserved0 Register (FRSV0)

This Flash register is reserved for factory testing.

Offset Module Base + 0x000C

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

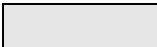
 = Unimplemented or Reserved

Figure 28-8. Flash Reserved0 Register (FRSV0)

All bits in the FRSV0 register read 0 and are not writable.

Table 30-17. FPROT Field Descriptions (continued)

Field	Description
2 FPLDIS	Flash Protection Lower Address Range Disable — The FPLDIS bit determines whether there is a protected/unprotected area in a specific region of the P-Flash memory beginning with global address 0x3_8000. 0 Protection/Unprotection enabled 1 Protection/Unprotection disabled
1–0 FPLS[1:0]	Flash Protection Lower Address Size — The FPLS bits determine the size of the protected/unprotected area in P-Flash memory as shown in Table 30-20 . The FPLS bits can only be written to while the FPLDIS bit is set.

Table 30-18. P-Flash Protection Function

FPOPEN	FPHDIS	FPLDIS	Function ¹
1	1	1	No P-Flash Protection
1	1	0	Protected Low Range
1	0	1	Protected High Range
1	0	0	Protected High and Low Ranges
0	1	1	Full P-Flash Memory Protected
0	1	0	Unprotected Low Range
0	0	1	Unprotected High Range
0	0	0	Unprotected High and Low Ranges

¹ For range sizes, refer to [Table 30-19](#) and [Table 30-20](#).

Table 30-19. P-Flash Protection Higher Address Range

FPHS[1:0]	Global Address Range	Protected Size
00	0x3_F800–0x3_FFFF	2 Kbytes
01	0x3_F000–0x3_FFFF	4 Kbytes
10	0x3_E000–0x3_FFFF	8 Kbytes
11	0x3_C000–0x3_FFFF	16 Kbytes

Table 30-20. P-Flash Protection Lower Address Range

FPLS[1:0]	Global Address Range	Protected Size
00	0x3_8000–0x3_83FF	1 Kbyte
01	0x3_8000–0x3_87FF	2 Kbytes
10	0x3_8000–0x3_8FFF	4 Kbytes
11	0x3_8000–0x3_9FFF	8 Kbytes

All possible P-Flash protection scenarios are shown in [Figure 30-14](#). Although the protection scheme is loaded from the Flash memory at global address 0x3_FF0C during the reset sequence, it can be changed by the user. The P-Flash protection scheme can be used by applications requiring reprogramming in single chip mode while providing as much protection as possible if reprogramming is not required.

Upon clearing CCIF to launch the Set User Margin Level command, the Memory Controller will set the user margin level for the targeted block and then set the CCIF flag.

NOTE

When the EEPROM block is targeted, the EEPROM user margin levels are applied only to the EEPROM reads. However, when the P-Flash block is targeted, the P-Flash user margin levels are applied to both P-Flash and EEPROM reads. It is not possible to apply user margin levels to the P-Flash block only.

Valid margin level settings for the Set User Margin Level command are defined in [Table 31-55](#).

Table 31-55. Valid Set User Margin Level Settings

CCOB (CCOBIX=001)	Level Description
0x0000	Return to Normal Level
0x0001	User Margin-1 Level ¹
0x0002	User Margin-0 Level ²

¹ Read margin to the erased state

² Read margin to the programmed state

Table 31-56. Set User Margin Level Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 001 at command launch.
		Set if command not available in current mode (see Table 31-27).
		Set if an invalid margin level setting is supplied.
	FPVIOL	None
	MGSTAT1	None
	MGSTAT0	None

NOTE

User margin levels can be used to check that Flash memory contents have adequate margin for normal level read operations. If unexpected results are encountered when checking Flash memory contents at user margin levels, a potential loss of information has been detected.

31.4.6.13 Set Field Margin Level Command

The Set Field Margin Level command, valid in special modes only, causes the Memory Controller to set the margin level specified for future read operations of the P-Flash or EEPROM block.

Appendix B

Detailed Register Address Map

Revision History

Version Number	Revision Date	Description of Changes
Rev 0.05	30-Aug-2010	<ul style="list-style-type: none"> Updated ADCCTL2 register in Appendix B, “Detailed Register Address Map”. Updated CPMUOSC register in Appendix B, “Detailed Register Address Map”.
Rev 0.06	18-Oct-2010	<ul style="list-style-type: none"> Updated ADC registers in Appendix B, “Detailed Register Address Map”.
Rev 0.07	9-Nov-2010	<ul style="list-style-type: none"> Updated CPMU registers in Appendix B, “Detailed Register Address Map”.
Rev 0.08	4-Dec-2010	<ul style="list-style-type: none"> Updated PIM registers in Appendix B, “Detailed Register Address Map”.
Rev 0.09	24-Apr-2012	<ul style="list-style-type: none"> Typos and formatting

B.1 Detailed Register Map

The following tables show the detailed register map of the MC9S12G-Family.

NOTE

This is a summary of all register bits implemented on MC9S12G devices. Each member of the MC9S12G-Family implements the subset of registers, which is associated with its feature set (see [Table 1-1](#)).

0x0000–0x0009 Port Integration Module (PIM) Map 1 of 6

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0000	PORTA	R W	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA 0
0x0001	PORTB	R W	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
0x0002	DDRA	R W	DDRA7	DDRA6	DDRA5	DDRA4	DDRA3	DDRA2	DDRA1	DDRA0
0x0003	DDRB	R W	DDRB7	DDRB6	DDRB5	DDRB4	DDRB3	DDRB2	DDRB1	DDRB0
0x0004	PORTC	R W	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
0x0005	PORTD	R W	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
0x0006	DDRC	R W	DDRC7	DDRC6	DDRC5	DDRC4	DDRC3	DDRC2	DDRC1	DDRC0
0x0007	DDRD	R W	DDRD7	DDRD6	DDRD5	DDRD4	DDRD3	DDRD2	DDRD1	DDRD0
0x0008	PORTE	R W	0	0	0	0	0	0	PE1	PE0
0x0009	DDRE	R W	0	0	0	0	0	0	DDRE1	DDRE0