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Details	
Product Status	Active
Core Processor	12V1
Core Size	16-Bit
Speed	25MHz
Connectivity	CANbus, IrDA, LINbus, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	54
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3.13V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s9s12g64f0vlh

Chapter 1
Device Overview MC9S12G-Family

Revision History

Version Number	Revision Date	Description of Changes
Rev 0.27	1-Apr-2011	• Typos and formatting
Rev 0.28	11-May-2011	•
Rev 0.29	10-Jan-2011	• Corrected Figure 1-4
Rev 0.30	10-Feb-2012	• Updated Table 1-5(added mask set 1N75C) • Typos and formatting
Rev 0.31	15-Mar-2012	• Updated Table 1-1 (added S12GSA devices) • Updated Figure 1-1 • Updated Table 1-5 (added S12GA devices) • Added Section 1.8.2, “S12GNA16 and S12GNA32” • Added Section 1.8.5, “S12GA48 and S12GA64” • Added Section 1.8.7, “S12GA96 and S12GA128” • Typos and formatting
Rev 0.32	07-May-2012	• Updated Section 1.19, “BDM Clock Source Connectivity” • Typos and formatting
Rev 0.33	27-Sep-2012	• Corrected Figure 1-4 • Corrected Figure 1-5 • Corrected Figure 1-6
Rev 0.34	25-Jan-2013	Added KGD option for the S12GA192 and the S12GA240 • Updated Table 1-1 • Corrected Table 1-2 • Corrected Table 1-6
Rev 0.35	02-Jul-2014	• Corrected Table 1-2
Rev 0.36	14-Jun-2017	• Extended Table 1-5

1.1 Introduction

The MC9S12G-Family is an optimized, automotive, 16-bit microcontroller product line focused on low-cost, high-performance, and low pin-count. This family is intended to bridge between high-end 8-bit microcontrollers and high-performance 16-bit microcontrollers, such as the MC9S12XS-Family. The MC9S12G-Family is targeted at generic automotive applications requiring CAN or LIN/J2602 communication. Typical examples of these applications include body controllers, occupant detection, door modules, seat controllers, RKE receivers, smart actuators, lighting modules, and smart junction boxes.

The MC9S12G-Family uses many of the same features found on the MC9S12XS- and MC9S12P-Family, including error correction code (ECC) on flash memory, a fast analog-to-digital converter (ADC) and a frequency modulated phase locked loop (IPLL) that improves the EMC performance.

1.7.2.15 PT[7:0] — Port TI/O Signals

PT[7:0] are general-purpose input or output signals. They can have a pull-up or pull-down device selected and enabled on per signal basis. Out of reset the pull devices are disabled .

1.7.2.16 AN[15:0] — ADC Input Signals

AN[15:0] are the analog inputs of the Analog-to-Digital Converter.

1.7.2.17 ACMP Signals

1.7.2.17.1 ACMPP — Non-Inverting Analog Comparator Input

ACMPP is the non-inverting input of the analog comparator.

1.7.2.17.2 ACMPM — Inverting Analog Comparator Input

ACMPM is the inverting input of the analog comparator.

1.7.2.17.3 ACMPO — Analog Comparator Output

ACMPO is the output of the analog comparator.

1.7.2.18 DAC Signals

1.7.2.18.1 DACU[1:0] Output Pins

These analog pins is used for the unbuffered analog output Voltages from the DAC0 and the DAC1 resistor network output, when the according mode is selected.

1.7.2.18.2 AMP[1:0] Output Pins

These analog pins are used for the buffered analog outputs Voltage from the operational amplifier outputs, when the according mode is selected.

1.7.2.18.3 AMPP[1:0] Input Pins

These analog input pins areused as input signals for the operational amplifiers positive input pins when the according mode is selected.

1.7.2.18.4 AMPM[1:0] Input Pins

These analog input pins are used as input signals for the operational amplifiers negative input pin when the according mode is selected.

Table 1-19. 64-Pin LQFP Pinout for S12GA48 and S12GA64

	Function <----lowest-----PRIORITY-----highest---->					Power Supply	Internal Pull Resistor	
Package Pin	Pin	2nd Func.	3rd Func.	4th Func	5th Func		CTRL	Reset State
57	PS5	MOSI0	—	—	—	V_{DDX}	PERS/PPSS	Up
58	PS6	SCK0	—	—	—	V_{DDX}	PERS/PPSS	Up
59	PS7	API_EXTCLK	ECLK	$\overline{SS0}$	—	V_{DDX}	PERS/PPSS	Up
60	PM0	RXCAN	—	—	—	V_{DDX}	PERM/PPSM	Disabled
61	PM1	TXCAN	—	—	—	V_{DDX}	PERM/PPSM	Disabled
62	PM2	—	—	—	—	V_{DDX}	PERM/PPSM	Disabled
63	PM3	—	—	—	—	V_{DDX}	PERM/PPSM	Disabled
64	PJ7	KWJ7	—	—	—	V_{DDX}	PERJ/PPSJ	Up

[1] The regular I/O characteristics (see Section A.2, “I/O Characteristics”) apply if the EXTAL/XTAL function is disabled

Table 1-25. 100-Pin LQFP Pinout for S12GA96 and S12GA128

	Function <----lowest-----PRIORITY-----highest---->				Power Supply	Internal Pull Resistor	
Package Pin	Pin	2nd Func.	3rd Func.	4th Func.		CTRL	Reset State
86	PS4	MISO0	—	—	V_{DDX}	PERS/PPSS	Up
87	PS5	MOSI0	—	—	V_{DDX}	PERS/PPSS	Up
88	PS6	SCK0	—	—	V_{DDX}	PERS/PPSS	Up
89	PS7	API_EXTCLK	$\overline{SS0}$	—	V_{DDX}	PERS/PPSS	Up
90	VSSX2	—	—	—	—	—	—
91	VDDX2	—	—	—	—	—	—
92	PM0	RXCAN	—	—	V_{DDX}	PERM/PPSM	Disabled
93	PM1	TXCAN	—	—	V_{DDX}	PERM/PPSM	Disabled
94	PD4	—	—	—	V_{DDX}	PUCR/PUPDE	Disabled
95	PD5	—	—	—	V_{DDX}	PUCR/PUPDE	Disabled
96	PD6	—	—	—	V_{DDX}	PUCR/PUPDE	Disabled
97	PD7	—	—	—	V_{DDX}	PUCR/PUPDE	Disabled
98	PM2	RXD2	—	—	V_{DDX}	PERM/PPSM	Disabled
99	PM3	TXD2	—	—	V_{DDX}	PERM/PPSM	Disabled
100	PJ7	KWJ7	$\overline{SS2}$	—	V_{DDX}	PERJ/PPSJ	Up

[1] The regular I/O characteristics (see Section A.2, “I/O Characteristics”) apply if the EXTAL/XTAL function is disabled

1.8.9 S12GA192 and S12GA240

1.8.9.1 Pinout 48-Pin LQFP

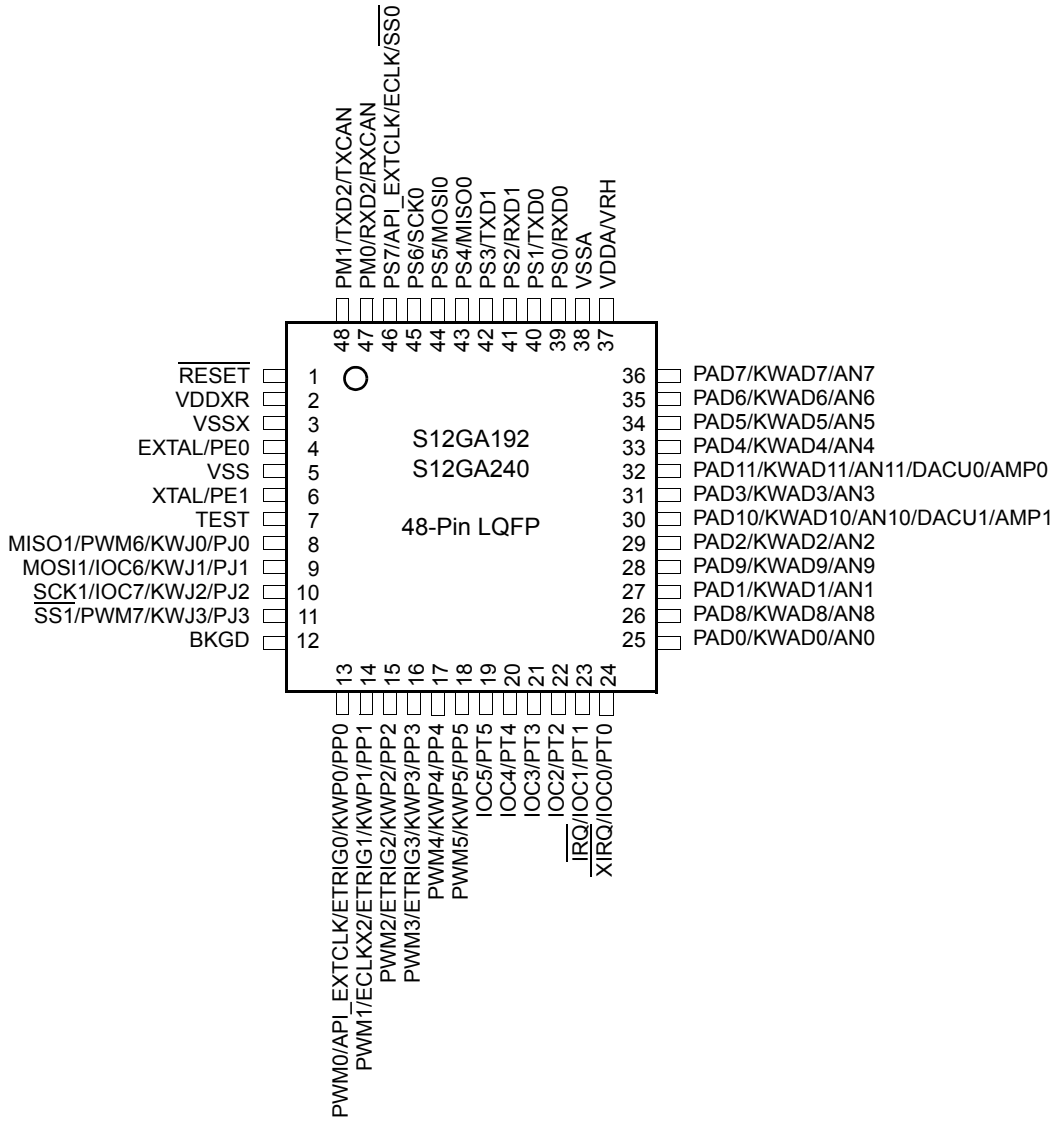


Figure 1-24. 48-Pin LQFP Pinout for S12GA192 and S12GA240

Table 1-29. 48-Pin LQFP Pinout for S12GA192 and S12GA240

	Function <----lowest-----PRIORITY-----highest---->					Power Supply	Internal Pull Resistor	
Package Pin	Pin	2nd Func.	3rd Func.	4th Func	5th Func		CTRL	Reset State
1	RESET	—	—	—	—	V_{DDX}	PULLUP	

Chapter 4
Reference Voltage Attenuator (RVAV1)

Revision History

Rev. No. (Item No.)	Date (Submitted By)	Sections Affected	Substantial Change(s)
V00.05	09 Jun 2010		• Added appendix title in note to reference reduced ADC clock • Orthographical corrections aligned to Freescale Publications Style Guide
V00.06	01 Jul 2010		• Aligned to S12 register guidelines
V01.00	18 Oct 2010		• Initial version

4.1 Introduction

The reference voltage attenuator (RVA) provides a circuit for reduction of the ADC reference voltage difference VRH-VSSA to gain more ADC resolution.

4.2 Features

The RVA has the following features:

- Attenuation of ADC reference voltage with low long-term drift

4.3 Block Diagram

The block diagram of the RVA module is shown below.

Refer to device overview section “ADC VRH/VRL Signal Connection” for connection of RVA to pins and ADC module.

Write: All modes through BDM operation when not secured

NOTE

When BDM is made active, the CPU stores the content of its CCR register in the BDMCCR register. However, out of special single-chip reset, the BDMCCR is set to 0xD8 and not 0xD0 which is the reset value of the CCR register in this CPU mode. Out of reset in all other modes the BDMCCR register is read zero.

When entering background debug mode, the BDM CCR holding register is used to save the condition code register of the user's program. It is also used for temporary storage in the standard BDM firmware mode. The BDM CCR holding register can be written to modify the CCR value.

7.3.2.2 BDM Program Page Index Register (BDMPPR)

Register Global Address 0x3_FF08

	7	6	5	4	3	2	1	0
R	BPAE	0	0	0	BPP3	BPP2	BPP1	BPP0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented, Reserved

Figure 7-5. BDM Program Page Register (BDMPPR)

Read: All modes through BDM operation when not secured

Write: All modes through BDM operation when not secured

Table 7-4. BDMPPR Field Descriptions

Field	Description
7 BPAE	**BDM Program Page Access Enable Bit** — BPAE enables program page access for BDM hardware and firmware read/write instructions The BDM hardware commands used to access the BDM registers (READ_BD and WRITE_BD) can not be used for program page accesses even if the BPAE bit is set. 0 BDM Program Paging disabled 1 BDM Program Paging enabled
3–0 BPP[3:0]	**BDM Program Page Index Bits 3–0** — These bits define the selected program page. For more detailed information regarding the program page window scheme, please refer to the S12S_MMC Block Guide.

7.3.3 Family ID Assignment

The family ID is an 8-bit value located in the BDM ROM in active BDM (at global address: 0x3_FF0F). The read-only value is a unique family ID which is 0xC2 for devices with an HCS12S core.

7.4 Functional Description

The BDM receives and executes commands from a host via a single wire serial interface. There are two types of BDM commands: hardware and firmware commands.

The clock source for the COP is either ACLK, IRCCLK or OSCCLK depending on the setting of the COPOSCSEL0 and COPOSCSEL1 bit (see also Table 10-6).
In Stop Mode with PSTP=1 (Pseudo Stop Mode), COPOSCSEL0=1 and COPOSCEL1=0 and PCE=1 the COP continues to run, else the COP counter halts in Stop Mode with COPOSCSEL1 =0.
In Full Stop Mode and Pseudo Stop Mode with COPOSCSEL1=1 the COP continues to run.

0x003C

	7	6	5	4	3	2	1	0
R	WCOP	RSBCK	0	0	0	CR2	CR1	CR0
W			WRTMASK					
Reset	F	0	0	0	0	F	F	F

After de-assert of System Reset the values are automatically loaded from the Flash memory. See Device specification for details.

= Unimplemented or Reserved

Figure 10-12. S12CPMU COP Control Register (CPMUCOP)

Read: Anytime

Write:

1. RSBCK: Anytime in Special Mode; write to “1” but not to “0” in Normal Mode
2. WCOP, CR2, CR1, CR0:
   - Anytime in Special Mode, when WRTMASK is 0, otherwise it has no effect
   - Write once in Normal Mode, when WRTMASK is 0, otherwise it has no effect.
     - Writing CR[2:0] to “000” has no effect, but counts for the “write once” condition.
     - Writing WCOP to “0” has no effect, but counts for the “write once” condition.

When a non-zero value is loaded from Flash to CR[2:0] the COP time-out period is started.

A change of the COPOSCSEL0 or COPSOCSEL1 bit (writing a different value) or loosing UPOSC status while COPOSCSEL1 is clear and COPOSCSEL0 is set, re-starts the COP time-out period.

In Normal Mode the COP time-out period is restarted if either of these conditions is true:

1. Writing a non-zero value to CR[2:0] (anytime in Special Mode, once in Normal Mode) with WRTMASK = 0.
2. Writing WCOP bit (anytime in Special Mode, once in Normal Mode) with WRTMASK = 0.
3. Changing RSBCK bit from “0” to “1”.

In Special Mode, any write access to CPMUCOP register restarts the COP time-out period.

10.4 Functional Description

10.4.1 Phase Locked Loop with Internal Filter (PLL)

The PLL is used to generate a high speed PLLCLK based on a low frequency REFCLK.

The REFCLK is by default the IRCCLK which is trimmed to f_{IRC1M_TRIM}=1MHz.

If using the oscillator (OSCE=1) REFCLK will be based on OSCCLK. For increased flexibility, OSCCLK can be divided in a range of 1 to 16 to generate the reference frequency REFCLK using the REFDIV[3:0] bits. Based on the SYNDIV[5:0] bits the PLL generates the VCOCLK by multiplying the reference clock by a 2, 4, 6,... 126, 128. Based on the POSTDIV[4:0] bits the VCOCLK can be divided in a range of 1,2, 3, 4, 5, 6,... to 32 to generate the PLLCLK.

If oscillator is enabled (OSCE=1) $$f_{REF} = \frac{f_{OSC}}{(REFDIV + 1)}$$

If oscillator is disabled (OSCE=0) $$f_{REF} = f_{IRC1M}$$

$$f_{VCO} = 2 \times f_{REF} \times (SYNDIV + 1)$$

If PLL is locked (LOCK=1) $$f_{PLL} = \frac{f_{VCO}}{(POSTDIV + 1)}$$

If PLL is not locked (LOCK=0) $$f_{PLL} = \frac{f_{VCO}}{4}$$

If PLL is selected (PLLSEL=1) $$f_{bus} = \frac{f_{PLL}}{2}$$

NOTE

Although it is possible to set the dividers to command a very high clock frequency, do not exceed the specified bus frequency limit for the MCU.

Several examples of PLL divider settings are shown in Table 10-25. The following rules help to achieve optimum stability and shortest lock time:

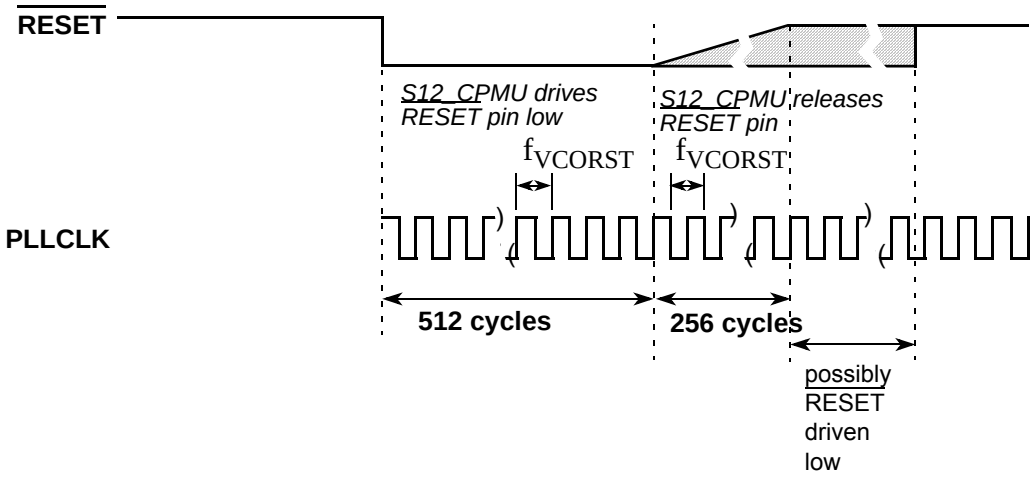
- Use lowest possible f_{VCO} / f_{REF} ratio (SYNDIV value).
- Use highest possible REFCLK frequency f_{REF}.

Table 10-25. Examples of PLL Divider Settings

f_{osc}	REFDIV[3:0]	f_{REF}	REFFRQ[1:0]	SYNDIV[5:0]	f_{VCO}	VCOFRQ[1:0]	POSTDIV[4:0]	f_{PLL}	f_{bus}
off	$00	1MHz	00	$18	50MHz	01	$03	12.5MHz	6.25MHz

The internal reset of the MCU remains asserted while the reset generator completes the 768 PLLCLK cycles long reset sequence. In case the RESET pin is externally driven low for more than these 768 PLLCLK cycles (External Reset), the internal reset remains asserted longer.

Figure 10-34. RESET Timing



10.5.2.1 Clock Monitor Reset

If the external oscillator is enabled (OSCE=1) in case of loss of oscillation or the oscillator frequency is below the failure assert frequency f_{CMFA} (see device electrical characteristics for values), the S12CPMU generates a Clock Monitor Reset.In Full Stop Mode the external oscillator and the clock monitor are disabled.

10.5.2.2 Computer Operating Properly Watchdog (COP) Reset

The COP (free running watchdog timer) enables the user to check that a program is running and sequencing properly. When the COP is being used, software is responsible for keeping the COP from timing out. If the COP times out it is an indication that the software is no longer being executed in the intended sequence; thus COP reset is generated.

The clock source for the COP is either ACLK, IRCCLK or OSCCLK depending on the setting of the COPOSCSEL0 and COPOSCSEL1 bit.
In Stop Mode with PSTP=1 (Pseudo Stop Mode), COPOSCSEL0=1 and COPOSCEL1=0 and PCE=1 the COP continues to run, else the COP counter halts in Stop Mode with COPOSCSEL1 =0.
In Pseudo Stop Mode and Full Stop Mode with COPOSCSEL1=1 the COP continues to run.

Table 10-28.gives an overview of the COP condition (run, static) in Stop Mode depending on legal configuration and status bit settings:

12.1.3 Block Diagram

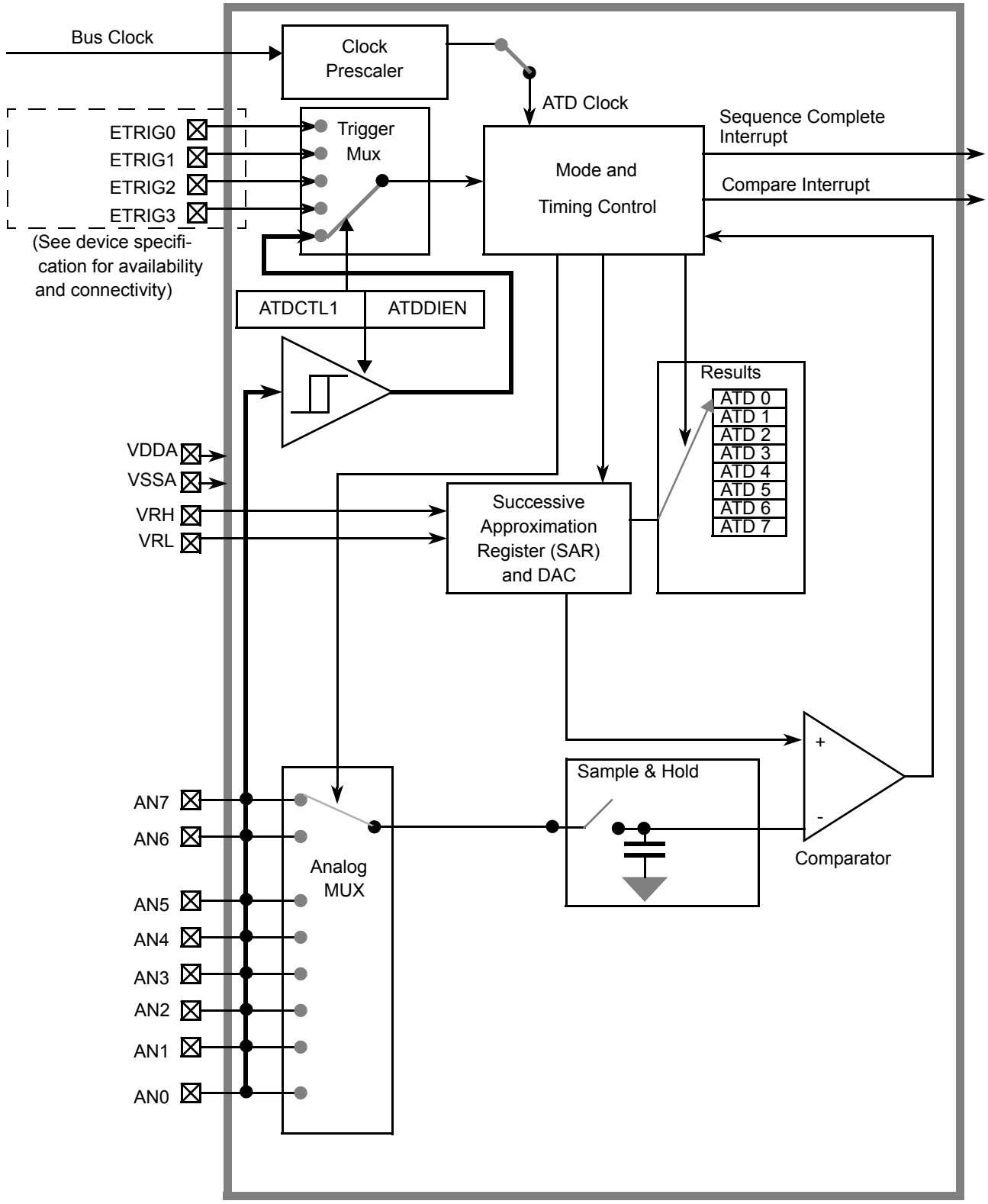


Figure 12-1. ADC12B8C Block Diagram

13.1.2 Modes of Operation

13.1.2.1 Conversion Modes

There is software programmable selection between performing **single** or **continuous conversion** on a **single channel** or **multiple channels**.

13.1.2.2 MCU Operating Modes

- **Stop Mode**
  Entering Stop Mode aborts any conversion sequence in progress and if a sequence was aborted restarts it after exiting stop mode. This has the same effect/consequences as starting a conversion sequence with write to ATDCTL5. So after exiting from stop mode with a previously aborted sequence all flags are cleared etc.
- **Wait Mode**
  ADC10B12C behaves same in Run and Wait Mode. For reduced power consumption continuous conversions should be aborted before entering Wait mode.
- **Freeze Mode**
  In Freeze Mode the ADC10B12C will either continue or finish or stop converting according to the FRZ1 and FRZ0 bits. This is useful for debugging and emulation.

15.3.2 Register Descriptions

This section describes in address order all the ADC10B16C registers and their individual bits.

15.3.2.1 ATD Control Register 0 (ATDCTL0)

Writes to this register will abort current conversion sequence.

Module Base + 0x0000

	7	6	5	4	3	2	1	0
R	Reserved	0	0	0	WRAP3	WRAP2	WRAP1	WRAP0
W								
Reset	0	0	0	0	1	1	1	1

= Unimplemented or Reserved

Figure 15-3. ATD Control Register 0 (ATDCTL0)

Read: Anytime

Write: Anytime, in special modes always write 0 to Reserved Bit 7.

Table 15-1. ATDCTL0 Field Descriptions

Field	Description
3-0 WRAP[3-0]	**Wrap Around Channel Select Bits** — These bits determine the channel for wrap around when doing multi-channel conversions. The coding is summarized in Table 15-2.

Table 15-2. Multi-Channel Wrap Around Coding

WRAP3	WRAP2	WRAP1	WRAP0	Multiple Channel Conversions (MULT = 1) Wraparound to AN0 after Converting
0	0	0	0	Reserved[1]
0	0	0	1	AN1
0	0	1	0	AN2
0	0	1	1	AN3
0	1	0	0	AN4
0	1	0	1	AN5
0	1	1	0	AN6
0	1	1	1	AN7
1	0	0	0	AN8
1	0	0	1	AN9
1	0	1	0	AN10
1	0	1	1	AN11
1	1	0	0	AN12
1	1	0	1	AN13
1	1	1	0	AN14
1	1	1	1	AN15

28.3.2.9.1 P-Flash Protection Restrictions

The general guideline is that P-Flash protection can only be added and not removed. Table 28-21 specifies all valid transitions between P-Flash protection scenarios. Any attempt to write an invalid scenario to the FPROT register will be ignored. The contents of the FPROT register reflect the active protection scenario. See the FPHS and FPLS bit descriptions for additional restrictions.

Table 28-21. P-Flash Protection Scenario Transitions

From Protection Scenario	To Protection Scenario[1]							
	0	1	2	3	4	5	6	7
0	X	X	X	X				
1		X		X				
2			X	X				
3				X				
4				X	X			
5			X	X	X	X		
6		X		X	X		X	
7	X	X	X	X	X	X	X	X

1 Allowed transitions marked with X, see Figure 28-14 for a definition of the scenarios.

28.3.2.10 EEPROM Protection Register (EEPROT)

The EEPROT register defines which EEPROM sectors are protected against program and erase operations.

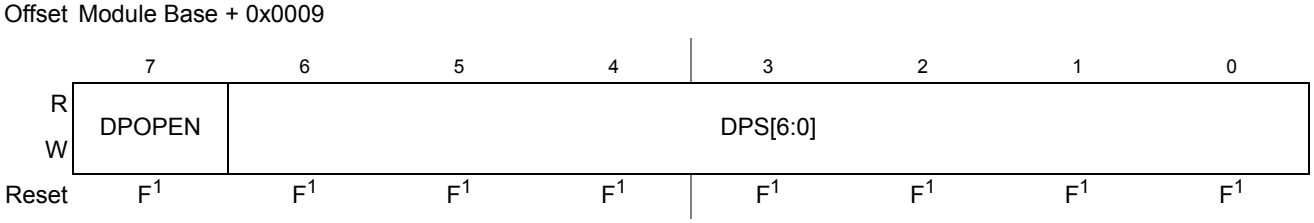


Figure 28-15. EEPROM Protection Register (EEPROT)

1 Loaded from IFR Flash configuration field, during reset sequence.

The (unreserved) bits of the EEPROT register are writable with the restriction that protection can be added but not removed. Writes must increase the DPS value and the DPOPEN bit can only be written from 1 (protection disabled) to 0 (protection enabled). If the DPOPEN bit is set, the state of the DPS bits is irrelevant.

During the reset sequence, fields DPOPEN and DPS of the EEPROT register are loaded with the contents of the EEPROM protection byte in the Flash configuration field at global address 0x3_FF0D located in

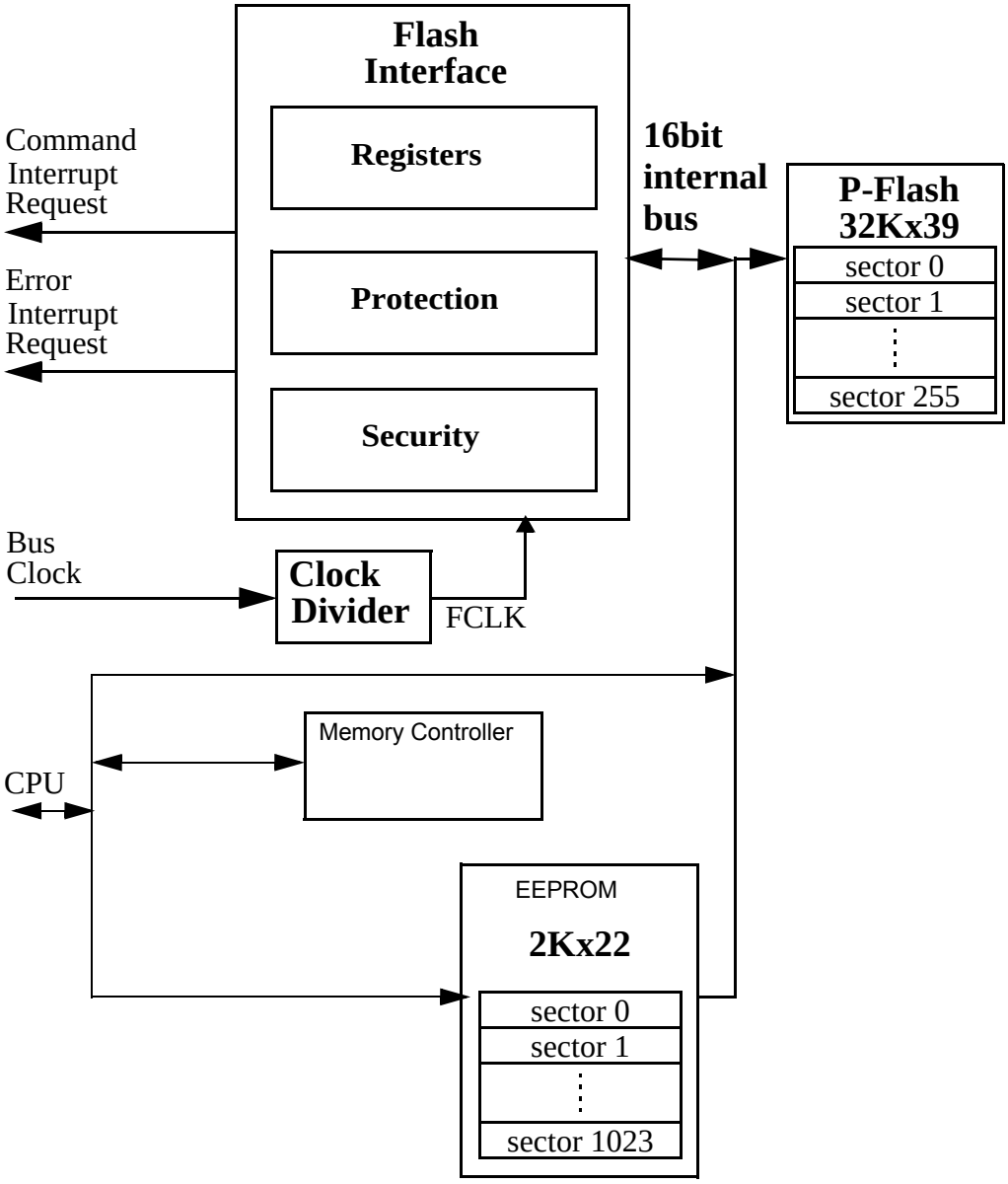


Figure 29-1. FTMRG128K1 Block Diagram

29.2 External Signal Description

The Flash module contains no signals that connect off-chip.

29.3.2.11 Flash Common Command Object Register (FCCOB)

The FCCOB is an array of six words addressed via the CCOBIX index found in the FCCOBIX register. Byte wide reads and writes are allowed to the FCCOB register.

Offset Module Base + 0x000A

	7	6	5	4	3	2	1	0
R W	CCOB[15:8]							
Reset	0	0	0	0	0	0	0	0

Figure 29-16. Flash Common Command Object High Register (FCCOBHI)

Offset Module Base + 0x000B

	7	6	5	4	3	2	1	0
R W	CCOB[7:0]							
Reset	0	0	0	0	0	0	0	0

Figure 29-17. Flash Common Command Object Low Register (FCCOBLO)

29.3.2.11.1 FCCOB - NVM Command Mode

NVM command mode uses the indexed FCCOB register to provide a command code and its relevant parameters to the Memory Controller. The user first sets up all required FCCOB fields and then initiates the command's execution by writing a 1 to the CCIF bit in the FSTAT register (a 1 written by the user clears the CCIF command completion flag to 0). When the user clears the CCIF bit in the FSTAT register all FCCOB parameter fields are locked and cannot be changed by the user until the command completes (as evidenced by the Memory Controller returning CCIF to 1). Some commands return information to the FCCOB register array.

The generic format for the FCCOB parameter fields in NVM command mode is shown in Table 29-24. The return values are available for reading after the CCIF flag in the FSTAT register has been returned to 1 by the Memory Controller. Writes to the unimplemented parameter fields (CCOBIX = 110 and CCOBIX = 111) are ignored with reads from these fields returning 0x0000.

Table 29-24 shows the generic Flash command format. The high byte of the first word in the CCOB array contains the command code, followed by the parameters for this specific Flash command. For details on the FCCOB settings required by each command, see the Flash command descriptions in Section 29.4.6.

Table 29-24. FCCOB - NVM Command Mode (Typical Usage)

CCOBIX[2:0]	Byte	FCCOB Parameter Fields (NVM Command Mode)
000	HI	FCMD[7:0] defining Flash command
	LO	6'h0, Global address [17:16]
001	HI	Global address [15:8]
	LO	Global address [7:0]

Table 30-36. Erase Verify P-Flash Section Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x03	Global address [17:16] of a P-Flash block
001	Global address [15:0] of the first phrase to be verified	
010	Number of phrases to be verified	

Upon clearing CCIF to launch the Erase Verify P-Flash Section command, the Memory Controller will verify the selected section of Flash memory is erased. The CCIF flag will set after the Erase Verify P-Flash Section operation has completed. If the section is not erased, it means blank check failed, both MGSTAT bits will be set.

Table 30-37. Erase Verify P-Flash Section Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 010 at command launch
		Set if command not available in current mode (see Table 30-27)
		Set if an invalid global address [17:0] is supplied see Table 30-3)
		Set if a misaligned phrase address is supplied (global address [2:0] != 000)
		Set if the requested section crosses a the P-Flash address boundary
	FPVIOL	None
	MGSTAT1	Set if any errors have been encountered during the read or if blank check failed.
	MGSTAT0	Set if any non-correctable errors have been encountered during the read or if blank check failed.

30.4.6.4 Read Once Command

The Read Once command provides read access to a reserved 64 byte field (8 phrases) located in the nonvolatile information register of P-Flash. The Read Once field is programmed using the Program Once command described in Section 30.4.6.6. The Read Once command must not be executed from the Flash block containing the Program Once reserved field to avoid code runaway.

Table 30-38. Read Once Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x04	Not Required
001	Read Once phrase index (0x0000 - 0x0007)	
010	Read Once word 0 value	
011	Read Once word 1 value	
100	Read Once word 2 value	
101	Read Once word 3 value	

Table 31-14. FERCNFG Field Descriptions

Field	Description
1 DFDIE	**Double Bit Fault Detect Interrupt Enable** — The DFDIE bit controls interrupt generation when a double bit fault is detected during a Flash block read operation. 0 DFDIF interrupt disabled 1 An interrupt will be requested whenever the DFDIF flag is set (see Section 31.3.2.8)
0 SFDIE	**Single Bit Fault Detect Interrupt Enable** — The SFDIE bit controls interrupt generation when a single bit fault is detected during a Flash block read operation. 0 SFDIF interrupt disabled whenever the SFDIF flag is set (see Section 31.3.2.8) 1 An interrupt will be requested whenever the SFDIF flag is set (see Section 31.3.2.8)

31.3.2.7 Flash Status Register (FSTAT)

The FSTAT register reports the operational status of the Flash module.

Offset Module Base + 0x0006

	7	6	5	4	3	2	1	0
R	CCIF	0	ACCERR	FPVIOL	MGBUSY	RSVD	MGSTAT[1:0]	
W								
Reset	1	0	0	0	0	0	0[1]	0[1]

= Unimplemented or Reserved

Figure 31-11. Flash Status Register (FSTAT)

[1] Reset value can deviate from the value shown if a double bit fault is detected during the reset sequence (see Section 31.6).

CCIF, ACCERR, and FPVIOL bits are readable and writable, MGBUSY and MGSTAT bits are readable but not writable, while remaining bits read 0 and are not writable.

Table 31-15. FSTAT Field Descriptions

Field	Description
7 CCIF	**Command Complete Interrupt Flag** — The CCIF flag indicates that a Flash command has completed. The CCIF flag is cleared by writing a 1 to CCIF to launch a command and CCIF will stay low until command completion or command violation. 0 Flash command in progress 1 Flash command has completed
5 ACCERR	**Flash Access Error Flag** — The ACCERR bit indicates an illegal access has occurred to the Flash memory caused by either a violation of the command write sequence (see Section 31.4.4.2) or issuing an illegal Flash command. While ACCERR is set, the CCIF flag cannot be cleared to launch a command. The ACCERR bit is cleared by writing a 1 to ACCERR. Writing a 0 to the ACCERR bit has no effect on ACCERR. 0 No access error detected 1 Access error detected
4 FPVIOL	**Flash Protection Violation Flag** —The FPVIOL bit indicates an attempt was made to program or erase an address in a protected area of P-Flash or EEPROM memory during a command write sequence. The FPVIOL bit is cleared by writing a 1 to FPVIOL. Writing a 0 to the FPVIOL bit has no effect on FPVIOL. While FPVIOL is set, it is not possible to launch a command or start a command write sequence. 0 No protection violation detected 1 Protection violation detected

Upon clearing CCIF to launch the Read Once command, a Read Once phrase is fetched and stored in the FCCOB indexed register. The CCIF flag will set after the Read Once operation has completed. Valid phrase index values for the Read Once command range from 0x0000 to 0x0007. During execution of the Read Once command, any attempt to read addresses within P-Flash block will return invalid data.

Table 31-39. Read Once Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 001 at command launch
		Set if command not available in current mode (see Table 31-27)
		Set if an invalid phrase index is supplied
	FPVIOL	None
	MGSTAT1	Set if any errors have been encountered during the read
	MGSTAT0	Set if any non-correctable errors have been encountered during the read

31.4.6.5 Program P-Flash Command

The Program P-Flash operation will program a previously erased phrase in the P-Flash memory using an embedded algorithm.

CAUTION

A P-Flash phrase must be in the erased state before being programmed. Cumulative programming of bits within a Flash phrase is not allowed.

Table 31-40. Program P-Flash Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x06	Global address [17:16] to identify P-Flash block
001	Global address [15:0] of phrase location to be programmed[1]	
010	Word 0 program value	
011	Word 1 program value	
100	Word 2 program value	
101	Word 3 program value	

[1] Global address [2:0] must be 000

Upon clearing CCIF to launch the Program P-Flash command, the Memory Controller will program the data words to the supplied global address and will then proceed to verify the data words read back as expected. The CCIF flag will set after the Program P-Flash operation has completed.

Table A-24. ADC Conversion Performance 5V range (Junction Temperature From +150°C To +160°C)

S12GN16, S12GN32								
Supply voltage 4.5V < V_{DDA} < 5.5 V, 150°C < T_J < 160°C, V_{REF} = V_{RH} - V_{RL} = V_{DDA}, f_{ADCCLK} = 8.0MHz The values are tested to be valid with no port AD output drivers switching simultaneous with conversions.								
Num	**C**	**Rating**[1]		**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	M	Resolution	10-Bit	LSB		5		mV
2	M	Differential Nonlinearity	10-Bit	DNL		±0.5		counts
3	M	Integral Nonlinearity	10-Bit	INL		±1		counts
4	M	Absolute Error[2]	10-Bit[3] 10-Bit[4]	AE		±2 ±2		counts
5	C	Resolution	8-Bit	LSB		20		mV
6	C	Differential Nonlinearity	8-Bit	DNL		±0.3		counts
7	C	Integral Nonlinearity	8-Bit	INL		±0.5		counts
8	C	Absolute Error[2]	8-Bit	AE		±1		counts

1 The 8-bit mode operation is structurally tested in production test. Absolute values are tested in 10-bit mode.

2 These values include the quantization error which is inherently 1/2 count for any A/D converter.

3 LQFP 48 and bigger

4 LQFP 32 and smaller

Table A-25. ADC Conversion Performance 3.3V range (Junction Temperature From –40°C To +150°C)

S12GNA16, S12GNA32, S12GAS48, S12GA64, S12GA96, S12GA128, S12GA192 and S12GA240								
Supply voltage 3.13V < V_{DDA} < 4.5 V, -40°C < T_J < 150°C, V_{REF} = V_{RH} - V_{RL} = V_{DDA}, f_{ADCCLK} = 8.0MHz The values are tested to be valid with no port AD output drivers switching simultaneous with conversions.								
Num	**C**	**Rating**[1]		**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	P	Resolution	12-Bit	LSB		0.80		mV
2	P	Differential Nonlinearity	12-Bit	DNL	-6	±3	6	counts
3	P	Integral Nonlinearity	12-Bit	INL	-7	±3	7	counts
4	P	Absolute Error[2]	12-Bit	AE	-8	±4	8	counts
5	C	Resolution	10-Bit	LSB		3.22		mV
6	C	Differential Nonlinearity	10-Bit	DNL	-1.5	±1	1.5	counts
7	C	Integral Nonlinearity	10-Bit	INL	-2	±1	2	counts
8	C	Absolute Error[2]	10-Bit	AE	-3	±2	3	counts
9	C	Resolution	8-Bit	LSB		12.89		mV
10	C	Differential Nonlinearity	8-Bit	DNL	-0.5	±0.3	0.5	counts
11	C	Integral Nonlinearity	8-Bit	INL	-1	±0.5	1	counts
12	C	Absolute Error[2]	8-Bit	AE	-1.5	±1	1.5	counts

1 The 8-bit and 10-bit mode operation is structurally tested in production test. Absolute values are tested in 12-bit mode.