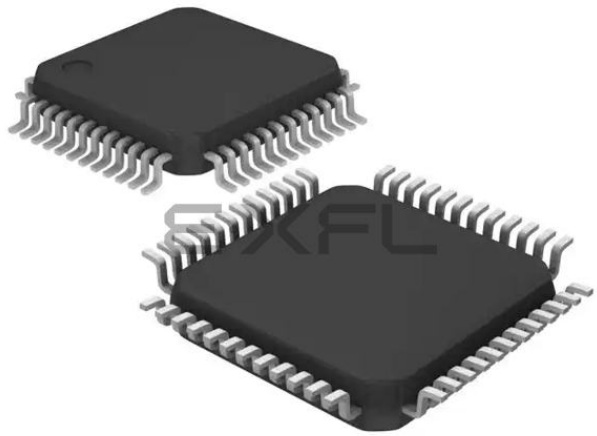

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Details	
Product Status	Active
Core Processor	12V1
Core Size	16-Bit
Speed	25MHz
Connectivity	CANbus, IrDA, LINbus, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	40
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3.13V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 150°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s9s12g64f0wlf

1.3.15 Reference Voltage Attenuator (RVA)

- Attenuation of ADC reference voltage with low long-term drift

1.3.16 Digital-to-Analog Converter Module (DAC)

- 1 digital-analog converter channel (per module) with:
  - 8 bit resolution
  - full and reduced output voltage range
  - buffered or unbuffered analog output voltage usable
- operational amplifier stand alone usable

1.3.17 Analog Comparator (ACMP)

- Low offset, low long-term offset drift
- Selectable interrupt on rising, falling, or rising and falling edges of comparator output
- Option to output comparator signal on an external pin
- Option to trigger timer input capture events

1.3.18 On-Chip Voltage Regulator (VREG)

- Linear voltage regulator with bandgap reference
- Low-voltage detect (LVD) with low-voltage interrupt (LVI)
- Power-on reset (POR) circuit
- Low-voltage reset (LVR)

1.3.19 Background Debug (BDM)

- Non-intrusive memory access commands
- Supports in-circuit programming of on-chip nonvolatile memory

1.3.20 Debugger (DBG)

- Trace buffer with depth of 64 entries
- Three comparators (A, B and C)
  - Access address comparisons with optional data comparisons
  - Program counter comparisons
  - Exact address or address range comparisons
- Two types of comparator matches
  - Tagged This matches just before a specific instruction begins execution
  - Force This is valid on the first instruction boundary after a match occurs
- Four trace modes

Address	Module	Size (Bytes)
0x03C8–0x03CF	DAC1 (Digital to Analog Converter)[8]	8
0x03D0–0x03FF	Reserved	48

1 The SCI1 is not available on the S12GN8, S12GN16, S12GN32, and S12GN32 devices
2 The SCI2 is not available on the S12GN8, S12GN16, S12GN32, S12GN32, S12G48, and S12G64 devices
3 The SPI1 is not available on the S12GN8, S12GN16, S12GN24, and S12GN32 devices
4 The SPI2 is not available on the S12GN8, S12GN16, S12GN32, S12GN32, S12G48, and S12G64 devices
5 The CAN is not available on the S12GN8, S12GN16, S12GN24, S12GN32, and S12GN48 devices
6 The ACMP is only available on the S12GN8, S12GN16, S12GN24, S12GN32, S12GN48,S12GN48, S12G48, and S12G64 devices
7 The RVA is only available on the S12GA192 and S12GA240 devices
8 DAC0 and DAC1 are only available on the S12GA192 and S12GA240 devices

NOTE

Reserved register space shown in Table 1-3 is not allocated to any module. This register space is reserved for future use. Writing to these locations has no effect. Read access to these locations returns zero.

Figure 1-2 shows S12G CPU and BDM local address translation to the global memory map as a graphical representation. In conjunction Table 1-4 shows the address ranges and mapping to 256K global memory space for P-Flash, EEPROM and RAM. The whole 256K global memory space is visible through the P-Flash window located in the 64k local memory map located at 0x8000 - 0xBFFF using the PPAGE register.

Table 1-4. MC9S12G-Family Memory Parameters

Feature	S12GN16	S12GN32	S12G48 S12GN48	S12G64	S12G96	S12G128	S12G192 S12GA192	S12G240 S12GA240
P-Flash size	16KB	32KB	48KB	64KB	96KB	128KB	192KB	240KB
PF_LOW	0x3C000	0x38000	0x34000	0x30000	0x28000	0x20000	0x10000	0x04000
PF_LOW_UNP (unpaged)[1]	0xC000	0x8000	0x4000	—	—	—	—	—
PPAGES	0x0F	0x0E - 0x0F	0x0D - 0x0F	0x0C - 0x0F	0x0A - 0x0F	0x08 - 0x0F	0x04 - 0x0F	0x01 - 0x0F
EEPROM [Bytes]	512	1024	1536	2048	3072	4096	4096	4096
EEPROM_HI	0x05FF	0x07FF	0x09FF	0x0BFF	0x0FFF	0x13FF	0x13FF	0x13FF

Table 1-25. 100-Pin LQFP Pinout for S12GA96 and S12GA128

	Function <----lowest-----PRIORITY-----highest---->				Power Supply	Internal Pull Resistor	
Package Pin	Pin	2nd Func.	3rd Func.	4th Func.		CTRL	Reset State
1	PJ6	KWJ6	SCK2	—	V_{DDX}	PERJ/PPSJ	Up
2	PJ5	KWJ5	MOSI2	—	V_{DDX}	PERJ/PPSJ	Up
3	PJ4	KWJ4	MISO2	—	V_{DDX}	PERJ/PPSJ	Up
4	PA0	—	—	—	V_{DDX}	PUCR/PUPAE	Disabled
5	PA1	—	—	—	V_{DDX}	PUCR/PUPAE	Disabled
6	PA2	—	—	—	V_{DDX}	PUCR/PUPAE	Disabled
7	PA3	—	—	—	V_{DDX}	PUCR/PUPAE	Disabled
8	RESET	—	—	—	V_{DDX}	PULLUP	
9	VDDX1	—	—	—	—	—	—
10	VDDR	—	—	—	—	—	—
11	VSSX1	—	—	—	—	—	—
12	PE0[1]	EXTAL	—	—	V_{DDX}	PUCR/PDPEE	Down
13	VSS	—	—	—	—	—	—
14	PE1[1]	XTAL	—	—	V_{DDX}	PUCR/PDPEE	Down
15	TEST	—	—	—	N.A.	$\overline{\text{RESET}}$ pin	Down
16	PA4	—	—	—	V_{DDX}	PUCR/PUPAE	Disabled
17	PA5	—	—	—	V_{DDX}	PUCR/PUPAE	Disabled
18	PA6	—	—	—	V_{DDX}	PUCR/PUPAE	Disabled
19	PA7	—	—	—	V_{DDX}	PUCR/PUPAE	Disabled
20	PJ0	KWJ0	MISO1	—	V_{DDX}	PERJ/PPSJ	Up
21	PJ1	KWJ1	MOSI1	—	V_{DDX}	PERJ/PPSJ	Up
22	PJ2	KWJ2	SCK1	—	V_{DDX}	PERJ/PPSJ	Up
23	PJ3	KWJ3	$\overline{\text{SS1}}$	—	V_{DDX}	PERJ/PPSJ	Up
24	BKGD	MODC	—	—	V_{DDX}	PUCR/BKPUE	Up
25	PB0	ECLK	—	—	V_{DDX}	PUCR/PUPBE	Disabled
26	PB1	API_EXTCLK	—	—	V_{DDX}	PUCR/PUPBE	Disabled
27	PB2	ECLKX2	—	—	V_{DDX}	PUCR/PUPBE	Disabled

Table 2-20. Block Register Map (G2) (continued)

Global Address Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0258 PTP	R	PTP7	PTP6	PTP5	PTP4	PTP3	PTP2	PTP1	PTP0
	W								
0x0259 PTIP	R	PTIP7	PTIP6	PTIP5	PTIP4	PTIP3	PTIP2	PTIP1	PTIP0
	W								
0x025A DDRP	R	DDRP7	DDRP6	DDRP5	DDRP4	DDRP3	DDRP2	DDRP1	DDRP0
	W								
0x025B Reserved	R	0	0	0	0	0	0	0	0
	W								
0x025C PERP	R	PERP7	PERP6	PERP5	PERP4	PERP3	PERP2	PERP1	PERP0
	W								
0x025D PPSP	R	PPSP7	PPSP6	PPSP5	PPSP4	PPSP3	PPSP2	PPSP1	PPSP0
	W								
0x025E PIEP	R	PIEP7	PIEP6	PIEP5	PIEP4	PIEP3	PIEP2	PIEP1	PIEP0
	W								
0x025F PIFP	R	PIFP7	PIFP6	PIFP5	PIFP4	PIFP3	PIFP2	PIFP1	PIFP0
	W								
0x0260–0x0261 Reserved	R	Reserved for ACMP							
	W								
0x0262–0x0266 Reserved	R	0	0	0	0	0	0	0	0
	W								
0x0267 Reserved	R	Reserved	Reserved	0	0	0	0	0	Reserved
	W								
0x0268 PTJ	R	PTJ7	PTJ6	PTJ5	PTJ4	PTJ3	PTJ2	PTJ1	PTJ0
	W								
0x0269 PTIJ	R	PTIJ7	PTIJ6	PTIJ5	PTIJ4	PTIJ3	PTIJ2	PTIJ1	PTIJ0
	W								
0x026A DDRJ	R	DDRJ7	DDRJ6	DDRJ5	DDRJ4	DDRJ3	DDRJ2	DDRJ1	DDRJ0
	W								
0x026B Reserved	R	0	0	0	0	0	0	0	0
	W								

= Unimplemented or Reserved

2.4.3.15 Port T Data Register (PTT)

Address 0x0240 (G1, G2) Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	PTT7	PTT6	PTT5	PTT4	PTT3	PTT2	PTT1	PTT0
W								
Reset	0	0	0	0	0	0	0	0

Address 0x0240 (G3) Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	0	0	PTT5	PTT4	PTT3	PTT2	PTT1	PTT0
W								
Reset	0	0	0	0	0	0	0	0

Figure 2-16. Port T Data Register (PTT)

[1] Read: Anytime. The data source is depending on the data direction value.
Write: Anytime

Table 2-35. PTT Register Field Descriptions

Field	Description
7-0 PTT	**Port T general-purpose input/output data**—Data Register When not used with an alternative signal, the associated pin can be used as general-purpose I/O. In general-purpose output mode the port data register bit value is driven to the pin. If the associated data direction bit is set to 1, a read returns the value of the port data register bit, otherwise the buffered pin input state is read.

2.4.3.16 Port T Input Register (PTIT)

Address 0x0241 (G1, G2) Access: User read only[1]

	7	6	5	4	3	2	1	0
R	PTIT7	PTIT6	PTIT5	PTIT4	PTIT3	PTIT2	PTIT1	PTIT0
W								
Reset	0	0	0	0	0	0	0	0

Address 0x0241 (G3) Access: User read only[1]

	7	6	5	4	3	2	1	0
R	0	0	PTIT5	PTIT4	PTIT3	PTIT2	PTIT1	PTIT0
W								
Reset	0	0	0	0	0	0	0	0

Figure 2-17. Port T Input Register (PTIT)

[1] Read: Anytime
Write:Never

Table 2-82. AN Routing Options

PRR1AN	Associated Pins
0	AN10 - PAD10 AN11 - PAD11 AN13 - PAD13 AN14 - PAD14 AN15 - PAD15
1	AN10 - PC0 AN11 - PC1 AN13 - PC2 AN14 - PC3 AN15 - PC4

2.4.3.57 Port AD Pull Enable Register (PER0AD)

Address 0x0278 (G1, G2) Access: User read/write[1]

	7	6	5	4	3	2	1	0
R W	PER0AD7	PER0AD6	PER0AD5	PER0AD4	PER0AD3	PER0AD2	PER0AD1	PER0AD0
Reset	0	0	0	0	0	0	0	0

Address 0x0278 (G3) Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	0	0	0	0	PER0AD3	PER0AD2	PER0AD1	PER0AD0
W								
Reset	0	0	0	0	0	0	0	0

Figure 2-56. Port AD Pullup Enable Register (PER0AD)

[1] Read: Anytime
Write: Anytime

Table 2-83. PER0AD Register Field Descriptions

Field	Description
7-0 PER0AD	**Port AD pull enable**—Enable pull device on input pin This bit controls whether a pull device on the associated port input pin is active. If a pin is used as output this bit has no effect. The polarity is selected by the related polarity select register bit. 1 Pull device enabled 0 Pull device disabled

Table 11-11. ATD Behavior in Freeze Mode (Breakpoint)

FRZ1	FRZ0	Behavior in Freeze Mode
0	1	Reserved
1	0	Finish current conversion, then freeze
1	1	Freeze Immediately

11.3.2.5 ATD Control Register 4 (ATDCTL4)

Writes to this register will abort current conversion sequence.

Module Base + 0x0004

Figure 11-7. ATD Control Register 4 (ATDCTL4)

Read: Anytime

Write: Anytime

Table 11-12. ATDCTL4 Field Descriptions

Field	Description
7–5 SMP[2:0]	**Sample Time Select** — These three bits select the length of the sample time in units of ATD conversion clock cycles. Note that the ATD conversion clock period is itself a function of the prescaler value (bits PRS4-0). Table 11-13 lists the available sample time lengths.
4–0 PRS[4:0]	**ATD Clock Prescaler** — These 5 bits are the binary prescaler value PRS. The ATD conversion clock frequency is calculated as follows: $f_{ATDCLK} = \frac{f_{BUS}}{2 \times (PRS + 1)}$ Refer to Device Specification for allowed frequency range of f_{ATDCLK}.

Table 11-13. Sample Time Select

SMP2	SMP1	SMP0	Sample Time in Number of ATD Clock Cycles
0	0	0	4
0	0	1	6
0	1	0	8
0	1	1	10
1	0	0	12
1	0	1	16
1	1	0	20
1	1	1	24

This buffer can be turned on or off with the ATDDIEN register for each ATD input pin.
This is important so that the buffer does not draw excess current when an ATD input pin is selected as analog input to the ADC12B8C.

12.5 Resets

At reset the ADC12B8C is in a power down state. The reset state of each individual bit is listed within the Register Description section (see Section 12.3.2, “Register Descriptions”) which details the registers and their bit-field.

12.6 Interrupts

The interrupts requested by the ADC12B8C are listed in Table 12-24. Refer to MCU specification for related vector address and priority.

Table 12-24. ATD Interrupt Vectors

Interrupt Source	CCR Mask	Local Enable
Sequence Complete Interrupt	I bit	ASCIE in ATDCTL2
Compare Interrupt	I bit	ACMPIE in ATDCTL2

See Section 12.3.2, “Register Descriptions” for further details.

15.5 Resets

At reset the ADC10B16C is in a power down state. The reset state of each individual bit is listed within the Register Description section (see Section 15.3.2, “Register Descriptions”) which details the registers and their bit-field.

15.6 Interrupts

The interrupts requested by the ADC10B16C are listed in Table 15-24. Refer to MCU specification for related vector address and priority.

Table 15-24. ATD Interrupt Vectors

Interrupt Source	CCR Mask	Local Enable
Sequence Complete Interrupt	I bit	ASCIE in ATDCTL2
Compare Interrupt	I bit	ACMPIE in ATDCTL2

See Section 15.3.2, “Register Descriptions” for further details.

Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0025 RESERVED	R	0	0	0	0	0	0	0	0
	W								
0x0026 RESERVED	R	0	0	0	0	0	0	0	0
	W								
0x0027 RESERVED	R	0	0	0	0	0	0	0	0
	W								

= Unimplemented or Reserved

Figure 19-2. The scalable PWM Register Summary (Sheet 1 of 4)

1 The related bit is available only if corresponding channel exists.

2 The register is available only if corresponding channel exists.

19.3.2.1 PWM Enable Register (PWME)

Each PWM channel has an enable bit (PWMEx) to start its waveform output. When any of the PWMEx bits are set (PWMEx = 1), the associated PWM output is enabled immediately. However, the actual PWM waveform is not available on the associated PWM output until its clock source begins its next cycle due to the synchronization of PWMEx and the clock source.

NOTE

The first PWM cycle after enabling the channel can be irregular.

An exception to this is when channels are concatenated. Once concatenated mode is enabled (CONxx bits set in PWMCTL register), enabling/disabling the corresponding 16-bit PWM channel is controlled by the low order PWMEx bit. In this case, the high order bytes PWMEx bits have no effect and their corresponding PWM output lines are disabled.

While in run mode, if all existing PWM channels are disabled (PWMEx–0 = 0), the prescaler counter shuts off for power savings.

Module Base + 0x0000

	7	6	5	4	3	2	1	0
R W	PWME7	PWME6	PWME5	PWME4	PWME3	PWME2	PWME1	PWME0
Reset	0	0	0	0	0	0	0	0

Figure 19-3. PWM Enable Register (PWME)

Read: Anytime

Write: Anytime

20.3.1 Module Memory Map and Register Definition

The memory map for the SCI module is given below in Figure 20-2. The address listed for each register is the address offset. The total address for each register is the sum of the base address for the SCI module and the address offset for each register.

20.3.2 Register Descriptions

This section consists of register descriptions in address order. Each description includes a standard register diagram with an associated figure number. Writes to a reserved register locations do not have any effect and reads of these locations return a zero. Details of register bit and field function follow the register diagrams, in bit order.

Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0000 SCIBDH[1]	R	IREN	TNP1	TNP0	SBR12	SBR11	SBR10	SBR9	SBR8
	W								
0x0001 SCIBDL[1]	R	SBR7	SBR6	SBR5	SBR4	SBR3	SBR2	SBR1	SBR0
	W								
0x0002 SCICR1[1]	R	LOOPS	SCISWAI	RSRC	M	WAKE	ILT	PE	PT
	W								
0x0000 SCIASR1[2]	R	RXEDGIF	0	0	0	0	BERRV	BERRIF	BKDIF
	W								
0x0001 SCIACR1[2]	R	RXEDGIE	0	0	0	0	0	BERRIE	BKDIE
	W								
0x0002 SCIACR2[2]	R	0	0	0	0	0	BERRM1	BERRM0	BKDFE
	W								
0x0003 SCICR2	R	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK
	W								
0x0004 SCISR1	R	TDRE	TC	RDRF	IDLE	OR	NF	FE	PF
	W								
0x0005 SCISR2	R	AMAP	0	0	TXPOL	RXPOL	BRK13	TXDIR	RAF
	W								

= Unimplemented or Reserved

Figure 20-2. SCI Register Summary (Sheet 1 of 2)

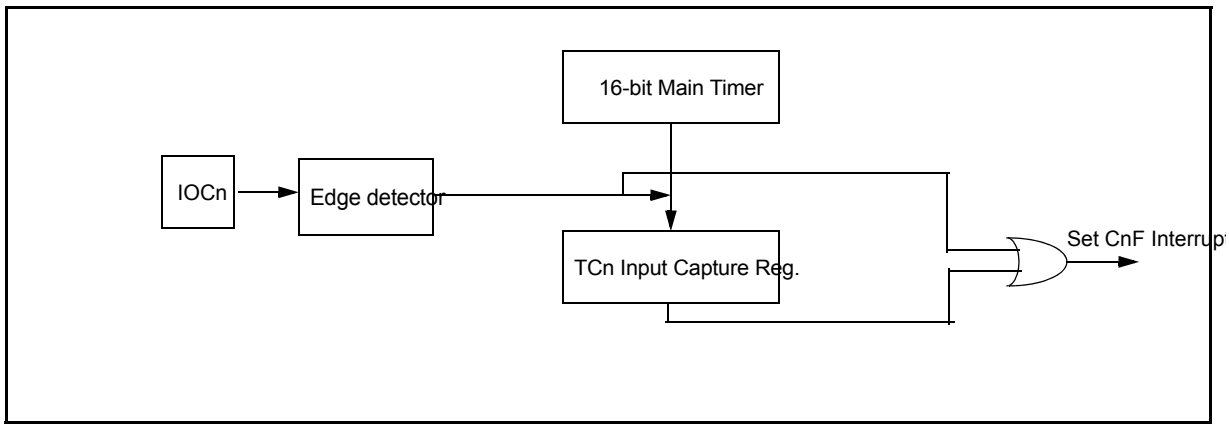

Figure 22-2. Interrupt Flag Setting

22.2 External Signal Description

The TIM16B6CV3 module has a selected number of external pins. Refer to device specification for exact number.

22.2.1 IOC5 - IOC0 — Input Capture and Output Compare Channel 5-0

Those pins serve as input capture or output compare for TIM16B6CV3 channel .

NOTE

For the description of interrupts see Section 22.6, “Interrupts”.

22.3 Memory Map and Register Definition

This section provides a detailed description of all memory and registers.

22.3.1 Module Memory Map

The memory map for the TIM16B6CV3 module is given below in Figure 22-3. The address listed for each register is the address offset. The total address for each register is the sum of the base address for the TIM16B6CV3 module and the address offset for each register.

22.3.2 Register Descriptions

This section consists of register descriptions in address order. Each description includes a standard register diagram with an associated figure number. Details of register bit and field function follow the register diagrams, in bit order.

Table 23-25. TIM16B8CV3 Interrupts

Interrupt	Offset	Vector	Priority	Source	Description
C[7:0]F	—	—	—	Timer Channel 7–0	Active high timer channel interrupts 7–0
PAOVI	—	—	—	Pulse Accumulator Input	Active high pulse accumulator input interrupt
PAOVF	—	—	—	Pulse Accumulator Overflow	Pulse accumulator overflow interrupt
TOF	—	—	—	Timer Overflow	Timer Overflow interrupt

The TIM16B8CV3 could use up to 11 interrupt vectors. The interrupt vector offsets and interrupt numbers are chip dependent.

23.6.1 Channel [7:0] Interrupt (C[7:0]F)

This active high outputs will be asserted by the module to request a timer channel 7 – 0 interrupt. The TIM block only generates the interrupt and does not service it. Only bits related to implemented channels are valid.

23.6.2 Pulse Accumulator Input Interrupt (PAOVI)

This active high output will be asserted by the module to request a timer pulse accumulator input interrupt. The TIM block only generates the interrupt and does not service it.

23.6.3 Pulse Accumulator Overflow Interrupt (PAOVF)

This active high output will be asserted by the module to request a timer pulse accumulator overflow interrupt. The TIM block only generates the interrupt and does not service it.

23.6.4 Timer Overflow Interrupt (TOF)

This active high output will be asserted by the module to request a timer overflow interrupt. The TIM block only generates the interrupt and does not service it.

Table 24-39. Program P-Flash Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 101 at command launch
		Set if command not available in current mode (see Table 24-25)
		Set if an invalid global address [17:0] is supplied see Table 24-3)[1]
		Set if a misaligned phrase address is supplied (global address [2:0] != 000)
	FPVIOL	Set if the global address [17:0] points to a protected area
	MGSTAT1	Set if any errors have been encountered during the verify operation
	MGSTAT0	Set if any non-correctable errors have been encountered during the verify operation

1 As defined by the memory map for FTMRG32K1.

24.4.6.6 Program Once Command

The Program Once command restricts programming to a reserved 64 byte field (8 phrases) in the nonvolatile information register located in P-Flash. The Program Once reserved field can be read using the Read Once command as described in Section 24.4.6.4. The Program Once command must only be issued once since the nonvolatile information register in P-Flash cannot be erased. The Program Once command must not be executed from the Flash block containing the Program Once reserved field to avoid code runaway.

Table 24-40. Program Once Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x07	Not Required
001	Program Once phrase index (0x0000 - 0x0007)	
010	Program Once word 0 value	
011	Program Once word 1 value	
100	Program Once word 2 value	
101	Program Once word 3 value	

Upon clearing CCIF to launch the Program Once command, the Memory Controller first verifies that the selected phrase is erased. If erased, then the selected phrase will be programmed and then verified with read back. The CCIF flag will remain clear, setting only after the Program Once operation has completed.

The reserved nonvolatile information register accessed by the Program Once command cannot be erased and any attempt to program one of these phrases a second time will not be allowed. Valid phrase index values for the Program Once command range from 0x0000 to 0x0007. During execution of the Program Once command, any attempt to read addresses within P-Flash will return invalid data.

30.3.2.9 P-Flash Protection Register (FPROT)

The FPROT register defines which P-Flash sectors are protected against program and erase operations.

Offset Module Base + 0x0008

	7	6	5	4	3	2	1	0
R	FPOPEN	RNV6	FPHDIS	FPHS[1:0]		FPLDIS	FPLS[1:0]	
W								
Reset	F[1]	F[1]	F[1]	F[1]	F[1]	F[1]	F[1]	F[1]

= Unimplemented or Reserved

Figure 30-13. Flash Protection Register (FPROT)

[1] Loaded from IFR Flash configuration field, during reset sequence.

The (unreserved) bits of the FPROT register are writable with the restriction that the size of the protected region can only be increased (see Section 30.3.2.9.1, “P-Flash Protection Restrictions,” and Table 30-21).

During the reset sequence, the FPROT register is loaded with the contents of the P-Flash protection byte in the Flash configuration field at global address 0x3_FF0C located in P-Flash memory (see Table 30-4) as indicated by reset condition ‘F’ in Figure 30-13. To change the P-Flash protection that will be loaded during the reset sequence, the upper sector of the P-Flash memory must be unprotected, then the P-Flash protection byte must be reprogrammed. If a double bit fault is detected while reading the P-Flash phrase containing the P-Flash protection byte during the reset sequence, the FPOPEN bit will be cleared and remaining bits in the FPROT register will be set to leave the P-Flash memory fully protected.

Trying to alter data in any protected area in the P-Flash memory will result in a protection violation error and the FPVIOL bit will be set in the FSTAT register. The block erase of a P-Flash block is not possible if any of the P-Flash sectors contained in the same P-Flash block are protected.

Table 30-17. FPROT Field Descriptions

Field	Description
7 FPOPEN	**Flash Protection Operation Enable** — The FPOPEN bit determines the protection function for program or erase operations as shown in Table 30-18 for the P-Flash block. 0 When FPOPEN is clear, the FPHDIS and FPLDIS bits define unprotected address ranges as specified by the corresponding FPHS and FPLS bits 1 When FPOPEN is set, the FPHDIS and FPLDIS bits enable protection for the address range specified by the corresponding FPHS and FPLS bits
6 RNV[6]	**Reserved Nonvolatile Bit** — The RNV bit should remain in the erased state for future enhancements.
5 FPHDIS	**Flash Protection Higher Address Range Disable** — The FPHDIS bit determines whether there is a protected/unprotected area in a specific region of the P-Flash memory ending with global address 0x3_FFFF. 0 Protection/Unprotection enabled 1 Protection/Unprotection disabled
4–3 FPHS[1:0]	**Flash Protection Higher Address Size** — The FPHS bits determine the size of the protected/unprotected area in P-Flash memory as shown inTable 30-19. The FPHS bits can only be written to while the FPHDIS bit is set.

Table A-12. CPMU Configuration for Pseudo Stop Current Measurement

CPMU REGISTER	Bit settings/Conditions
CPMUOSC	OSCE=1, External Square wave on EXTAL f_{EXTAL}=4MHz, V_{IH}= 1.8V, V_{IL}=0V
CPMURTI	RTDEC=0, RTR[6:4]=111, RTR[3:0]=1111;
CPMUCOP	WCOP=1, CR[2:0]=111

Table A-13. CPMU Configuration for Run/Wait and Full Stop Current Measurement

CPMU REGISTER	Bit settings/Conditions
CPMUSYNR	VCOFRQ[1:0]=01,SYNDIV[5:0] = 24
CPMUPOSTDIV	POSTDIV[4:0]=0
CPMUCLKS	PLLSEL=1
CPMUOSC	OSCE=0, Reference clock for PLL is f_{ref}=f_{irc1m} trimmed to 1MHz
API settings for STOP current measurement	
CPMUAPICTL	APIEA=0, APIFE=1, APIE=0
CPMUAPITR	trimmed to 10Khz
CPMUAPIRH/RL	set to $FFFF

Table A-14. Peripheral Configurations for Run & Wait Current Measurement

Peripheral	Configuration
MSCAN	Configured to loop-back mode using a bit rate of 1Mbit/s
SPI	Configured to master mode, continuously transmit data (0x55 or 0xAA) at 1Mbit/s
SCI	Configured into loop mode, continuously transmit data (0x55) at speed of 57600 baud
PWM	Configured to toggle its pins at the rate of 40kHz
ADC	The peripheral is configured to operate at its maximum specified frequency and to continuously convert voltages on all input channels in sequence.

0x0180–0x023F Reserved

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0180-0x023F	Reserved	R	0	0	0	0	0	0	0	0
		W								

0x0240–0x025F Port Integration Module (PIM) Map 4 of 6

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0240	PTT	R	PTT7	PTT6	PTT5	PTT4	PTT3	PTT2	PTT1	PTT0
		W								
0x0241	PTIT	R	PTIT7	PTIT6	PTIT5	PTIT4	PTIT3	PTIT2	PTIT1	PTIT0
		W								
0x0242	DDRT	R	DDRT7	DDRT6	DDRT5	DDRT4	DDRT3	DDRT2	DDRT1	DDRT0
		W								
0x0243	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0244	PERT	R	PERT7	PERT6	PERT5	PERT4	PERT3	PERT2	PERT1	PERT0
		W								
0x0245	PPST	R	PPST7	PPST6	PPST5	PPST4	PPST3	PPST2	PPST1	PPST0
		W								
0x0246-0x0247	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0248	PTS	R	PTS7	PTS6	PTS5	PTS4	PTS3	PTS2	PTS1	PTS0
		W								
0x0249	PTIS	R	PTIS7	PTIS6	PTIS5	PTIS4	PTIS3	PTIS2	PTIS1	PTIS0
		W								
0x024A	DDRS	R	DDRS7	DDRS6	DDRS5	DDRS4	DDRS3	DDRS2	DDRS1	DDRS0
		W								
0x024B	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x024C	PERS	R	PERS7	PERS6	PERS5	PERS4	PERS3	PERS2	PERS1	PERS0
		W								
0x024D	PPSS	R	PPSS7	PPSS6	PPSS5	PPSS4	PPSS3	PPSS2	PPSS1	PPSS0
		W								
0x024E	WOMS	R	WOMS7	WOMS6	WOMS5	WOMS4	WOMS3	WOMS2	WOMS1	WOMS0
		W								
0x024F	PRR0	R	PRR0P3	PRR0P2	PRR0T31	PRR0T30	PRR0T21	PRR0T20	PRR0S1	PRR0S0
		W								
0x0250	PTM	R	0	0	0	0	PTM3	PTM2	PTM1	PTM0
		W								
0x0251	PTIM	R	0	0	0	0	PTIM3	PTIM2	PTIM1	PTIM0
		W								
0x0252	DDRM	R	0	0	0	0	DDRM3	DDRM2	DDRM1	DDRM0
		W								
0x0253	Reserved	R	0	0	0	0	0	0	0	0
		W								

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5–1994.

3. DATUMS A, B, AND D TO BE DETERMINED AT DATUM PLANE H.

4. DIMENSIONS TO BE DETERMINED AT SEATING PLANE DATUM C.

5. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM DIMENSION BY MORE THAN 0.08 MM. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION: 0.07 MM.

6. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 MM PER SIDE. DIMENSIONS ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.

7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.

8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1 MM AND 0.25 MM FROM THE LEAD TIP.

MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

TITLE:	DOCUMENT NO: 98ASH70029A	REV: D
LOW PROFILE QUAD FLAT PACK (LQFP) 32 LEAD, 0.8 PITCH (7 X 7 X 1.4)	CASE NUMBER: 873A-03	19 MAY 2005
	STANDARD: JEDEC MS-026 BBA	