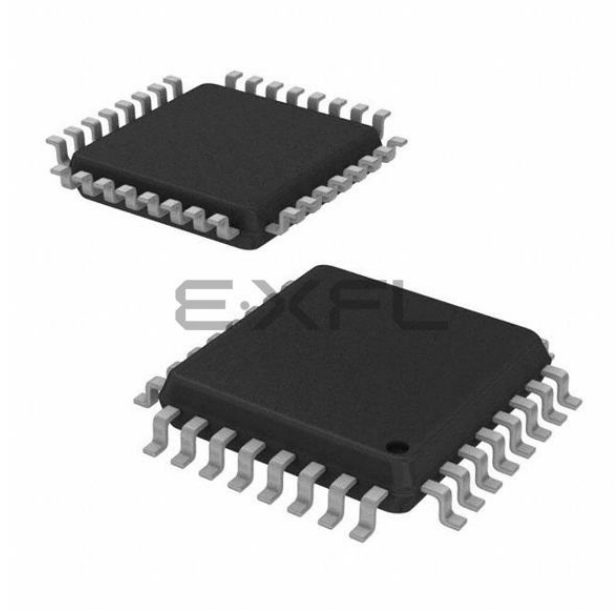

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Product Status	Active
Core Processor	12V1
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Speed	25MHz
Connectivity	CANbus, IrDA, LINbus, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	26
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3.13V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s9s12g64f1mlc

Chapter 1
Device Overview MC9S12G-Family

Revision History

Version Number	Revision Date	Description of Changes
Rev 0.27	1-Apr-2011	• Typos and formatting
Rev 0.28	11-May-2011	•
Rev 0.29	10-Jan-2011	• Corrected Figure 1-4
Rev 0.30	10-Feb-2012	• Updated Table 1-5(added mask set 1N75C) • Typos and formatting
Rev 0.31	15-Mar-2012	• Updated Table 1-1 (added S12GSA devices) • Updated Figure 1-1 • Updated Table 1-5 (added S12GA devices) • Added Section 1.8.2, “S12GNA16 and S12GNA32” • Added Section 1.8.5, “S12GA48 and S12GA64” • Added Section 1.8.7, “S12GA96 and S12GA128” • Typos and formatting
Rev 0.32	07-May-2012	• Updated Section 1.19, “BDM Clock Source Connectivity” • Typos and formatting
Rev 0.33	27-Sep-2012	• Corrected Figure 1-4 • Corrected Figure 1-5 • Corrected Figure 1-6
Rev 0.34	25-Jan-2013	Added KGD option for the S12GA192 and the S12GA240 • Updated Table 1-1 • Corrected Table 1-2 • Corrected Table 1-6
Rev 0.35	02-Jul-2014	• Corrected Table 1-2
Rev 0.36	14-Jun-2017	• Extended Table 1-5

1.1 Introduction

The MC9S12G-Family is an optimized, automotive, 16-bit microcontroller product line focused on low-cost, high-performance, and low pin-count. This family is intended to bridge between high-end 8-bit microcontrollers and high-performance 16-bit microcontrollers, such as the MC9S12XS-Family. The MC9S12G-Family is targeted at generic automotive applications requiring CAN or LIN/J2602 communication. Typical examples of these applications include body controllers, occupant detection, door modules, seat controllers, RKE receivers, smart actuators, lighting modules, and smart junction boxes.

The MC9S12G-Family uses many of the same features found on the MC9S12XS- and MC9S12P-Family, including error correction code (ECC) on flash memory, a fast analog-to-digital converter (ADC) and a frequency modulated phase locked loop (IPLL) that improves the EMC performance.

Table 1-2. Maximum Peripheral Availability per Package

Peripheral	20 TSSOP	32 LQFP	48 QFN	48 LQFP	64 LQFP	100 LQFP	KGD (Die)
DAC0	—	—	—	Yes	Yes	Yes	Yes
DAC1	—	—	—	Yes	Yes	Yes	Yes
ACMP	Yes	Yes	Yes	Yes	Yes	—	—
Total GPIO	14	26	40	40	54	86	86

1.2.2 Chip-Level Features

On-chip modules available within the family include the following features:

- S12 CPU core
- Up to 240 Kbyte on-chip flash with ECC
- Up to 4 Kbyte EEPROM with ECC
- Up to 11 Kbyte on-chip SRAM
- Phase locked loop (IPLL) frequency multiplier with internal filter
- 4–16 MHz amplitude controlled Pierce oscillator
- 1 MHz internal RC oscillator
- Timer module (TIM) supporting up to eight channels that provide a range of 16-bit input capture, output compare, counter, and pulse accumulator functions
- Pulse width modulation (PWM) module with up to eight x 8-bit channels
- Up to 16-channel, 10 or 12-bit resolution successive approximation analog-to-digital converter (ADC)
- Up to two 8-bit digital-to-analog converters (DAC)
- Up to one 5V analog comparator (ACMP)
- Up to three serial peripheral interface (SPI) modules
- Up to three serial communication interface (SCI) modules supporting LIN communications
- Up to one multi-scalable controller area network (MSCAN) module (supporting CAN protocol 2.0A/B)
- On-chip voltage regulator (VREG) for regulation of input supply and all internal voltages
- Autonomous periodic interrupt (API)
- Precision fixed voltage reference for ADC conversions
- Optional reference voltage attenuator module to increase ADC accuracy

1.3 Module Features

The following sections provide more details of the modules implemented on the MC9S12G-Family family.

1.7.2.15 PT[7:0] — Port TI/O Signals

PT[7:0] are general-purpose input or output signals. They can have a pull-up or pull-down device selected and enabled on per signal basis. Out of reset the pull devices are disabled .

1.7.2.16 AN[15:0] — ADC Input Signals

AN[15:0] are the analog inputs of the Analog-to-Digital Converter.

1.7.2.17 ACMP Signals

1.7.2.17.1 ACMPP — Non-Inverting Analog Comparator Input

ACMPP is the non-inverting input of the analog comparator.

1.7.2.17.2 ACMPM — Inverting Analog Comparator Input

ACMPM is the inverting input of the analog comparator.

1.7.2.17.3 ACMPO — Analog Comparator Output

ACMPO is the output of the analog comparator.

1.7.2.18 DAC Signals

1.7.2.18.1 DACU[1:0] Output Pins

These analog pins is used for the unbuffered analog output Voltages from the DAC0 and the DAC1 resistor network output, when the according mode is selected.

1.7.2.18.2 AMP[1:0] Output Pins

These analog pins are used for the buffered analog outputs Voltage from the operational amplifier outputs, when the according mode is selected.

1.7.2.18.3 AMPP[1:0] Input Pins

These analog input pins areused as input signals for the operational amplifiers positive input pins when the according mode is selected.

1.7.2.18.4 AMPM[1:0] Input Pins

These analog input pins are used as input signals for the operational amplifiers negative input pin when the according mode is selected.

Table 1-18. 48-Pin LQFP Pinout for S12GA48 and S12GA64

	Function <----lowest-----PRIORITY-----highest---->					Power Supply	Internal Pull Resistor	
Package Pin	Pin	2nd Func.	3rd Func.	4th Func	5th Func		CTRL	Reset State
30	PAD10	KWAD10	AN10	ACMPP		V_{DDA}	PER0AD/PPS0AD	Disabled
31	PAD3	KWAD3	AN3	—	—	V_{DDA}	PER1AD/PPS1AD	Disabled
32	PAD11	KWAD11	AN11	ACMPM		V_{DDA}	PER0AD/PPS0AD	Disabled
33	PAD4	KWAD4	AN4	—	—	V_{DDA}	PER1AD/PPS1AD	Disabled
34	PAD5	KWAD5	AN5	—	—	V_{DDA}	PER1AD/PPS0AD	Disabled
35	PAD6	KWAD6	AN6	—	—	V_{DDA}	PER1AD/PPS1AD	Disabled
36	PAD7	KWAD7	AN7	—	—	V_{DDA}	PER1AD/PPS1AD	Disabled
37	VDDA	VRH	—	—	—	—	—	—
38	VSSA	—	—	—	—	—	—	—
39	PS0	RXD0	—	—	—	V_{DDX}	PERS/PPSS	Up
40	PS1	TXD0	—	—	—	V_{DDX}	PERS/PPSS	Up
41	PS2	RXD1	—	—	—	V_{DDX}	PERS/PPSS	Up
42	PS3	TXD1	—	—	—	V_{DDX}	PERS/PPSS	Up
43	PS4	MISO0	—	—	—	V_{DDX}	PERS/PPSS	Up
44	PS5	MOSI0	—	—	—	V_{DDX}	PERS/PPSS	Up
45	PS6	SCK0	—	—	—	V_{DDX}	PERS/PPSS	Up
46	PS7	API_EXTCLK	ECLK	$\overline{SS0}$	—	V_{DDX}	PERS/PPSS	Up
47	PM0	RXCAN	—	—	—	V_{DDX}	PERM/PPSM	Disabled
48	PM1	TXCAN	—	—	—	V_{DDX}	PERM/PPSM	Disabled

[1] The regular I/O characteristics (see Section A.2, “I/O Characteristics”) apply if the EXTAL/XTAL function is disabled

Table 2-4. Signals and Priorities

Port	Pin	Signal	Signals per Device and Package (signal priority on pin from top to bottom)																				I/O	Description
			GA240 / GA192	G240 / G192	G128 / GA128 / G96 / GA96	GA240 / GA192	G240 / G192	G128 / GA128 / G96 / GA96	G64 / GA64 / G48 / GA48	GN48	GA240 / GA192	G240 / G192	G128 / GA128 / G96 / GA96	G64 / GA64 / G48 / GA48	GN48	GN32 / GNA32	GN16 / GNA16	G64 / G48	GN48	GN32	GN16	GN32	GN16		
			100			64					48							32				20			
M	PM3	TXD2	?	?	?	?	?	?																I/O	SCI transmit
		[PTM3]	?	?	?	?	?	?	?	?														I/O	GPIO
	PM2	RXD2	?	?	?	?	?	?																I	SCI receive
		[PTM2]	?	?	?	?	?	?	?	?														I/O	GPIO
	PM1	TXCAN	?	?	?	?	?	?	?		?	?	?	?				?						O	MSCAN transmit
		TXD2									?	?	?											I/O	SCI transmit
		TXD1																?	?					I/O	SCI transmit
		[PTM1]	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?			I/O	GPIO
	PM0	RXCAN	?	?	?	?	?	?	?		?	?	?	?				?						I	MSCAN receive
		RXD2									?	?	?											I	SCI receive
		RXD1																?	?					I	SCI receive
		[PTM0]	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?			I/O	GPIO

Legend	
?	Signal available on pin
?	Routing option on pin
?	Routing reset location
	Not available on pin

Table 2-12. Port S Pins PS7-0 (continued)

PS4	• The SPI0 MISO signal is mapped to this pin when used with the SPI function. Depending on the configuration of the enabled SPI0 the I/O state is forced to be input or output. • 20 TSSOP: The SCI0 RXD signal is mapped to this pin when used with the SCI function. If the SCI0 RXD signal is enabled and routed here the I/O state will be forced to input. • 20 TSSOP: The PWM channel 2 signal is mapped to this pin when used with the PWM function. If the PWM channel is enabled and routed here the I/O state is forced to output. • 32 LQFP: The PWM channel 4 signal is mapped to this pin when used with the PWM function. The enabled PWM channel forces the I/O state to be an output. • 20 TSSOP: The ADC ETRIG2 signal is mapped to this pin if PWM channel 2 is routed here. The enabled external trigger function has no effect on the I/O state. Refer to Section 2.6.4, “ADC External Triggers ETRIG3-0”. • Signal priority: 20 TSSOP: MISO0 > RXD0 > PWM2 > GPO 32 LQFP: MISO0 > PWM4 > GPO Others: MISO0 > GPO
PS3	• Except 20 TSSOP and 32 LQFP: The SCI1 TXD signal is mapped to this pin when used with the SCI function. If the SCI1 TXD signal is enabled the I/O state will depend on the SCI1 configuration. • Signal priority: 48/64/100 LQFP: TXD1 > GPO
PS2	• Except 20 TSSOP and 32 LQFP: The SCI1 RXD signal is mapped to this pin when used with the SCI function. If the SCI1 RXD signal is enabled the I/O state will be forced to be input. • Signal priority: 20 TSSOP and 32 LQFP: GPO Others: RXD1 > GPO
PS1	• Except 20 TSSOP: The SCI0 TXD signal is mapped to this pin when used with the SCI function. If the SCI0 TXD signal is enabled the I/O state will depend on the SCI0 configuration. • Signal priority: Except 20 TSSOP: TXD0 > GPO
PS0	• Except 20 TSSOP: The SCI0 RXD signal is mapped to this pin when used with the SCI function. If the SCI0 RXD signal is enabled the I/O state will be forced to be input. • Signal priority: 20 TSSOP: GPO Others: RXD0 > GPO

If an interrupt is pending when a TRACE1 command is issued, the interrupt stacking operation occurs but no user instruction is executed. Once back in standard BDM firmware execution, the program counter points to the first instruction in the interrupt service routine.

Be aware when tracing through the user code that the execution of the user code is done step by step but all peripherals are free running. Hence possible timing relations between CPU code execution and occurrence of events of other peripherals no longer exist.

Do not trace the CPU instruction BGND used for soft breakpoints. Tracing over the BGND instruction will result in a return address pointing to BDM firmware address space.

When tracing through user code which contains stop or wait instructions the following will happen when the stop or wait instruction is traced:

The CPU enters stop or wait mode and the TRACE1 command can not be finished before leaving the low power mode. This is the case because BDM active mode can not be entered after CPU executed the stop instruction. However all BDM hardware commands except the BACKGROUND command are operational after tracing a stop or wait instruction and still being in stop or wait mode. If system stop mode is entered (all bus masters are in stop mode) no BDM command is operational.

As soon as stop or wait mode is exited the CPU enters BDM active mode and the saved PC value points to the entry of the corresponding interrupt service routine.

In case the handshake feature is enabled the corresponding ACK pulse of the TRACE1 command will be discarded when tracing a stop or wait instruction. Hence there is no ACK pulse when BDM active mode is entered as part of the TRACE1 command after CPU exited from stop or wait mode. All valid commands sent during CPU being in stop or wait mode or after CPU exited from stop or wait mode will have an ACK pulse. The handshake feature becomes disabled only when system stop mode has been reached. Hence after a system stop mode the handshake feature must be enabled again by sending the ACK_ENABLE command.

7.4.11 Serial Communication Time Out

The host initiates a host-to-target serial transmission by generating a falling edge on the BKGD pin. If BKGD is kept low for more than 128 target clock cycles, the target understands that a SYNC command was issued. In this case, the target will keep waiting for a rising edge on BKGD in order to answer the SYNC request pulse. If the rising edge is not detected, the target will keep waiting forever without any time-out limit.

Consider now the case where the host returns BKGD to logic one before 128 cycles. This is interpreted as a valid bit transmission, and not as a SYNC request. The target will keep waiting for another falling edge marking the start of a new bit. If, however, a new falling edge is not detected by the target within 512 clock cycles since the last falling edge, a time-out occurs and the current command is discarded without affecting memory or the operating mode of the MCU. This is referred to as a soft-reset.

If a read command is issued but the data is not retrieved within 512 serial clock cycles, a soft-reset will occur causing the command to be disregarded. The data is not available for retrieval after the time-out has occurred. This is the expected behavior if the handshake protocol is not enabled. In order to allow the data to be retrieved even with a large clock frequency mismatch (between BDM and CPU) when the hardware

8.4.6 Tagging

A tag follows program information as it advances through the instruction queue. When a tagged instruction reaches the head of the queue a tag hit occurs and can initiate a state sequencer transition.

Each comparator control register features a TAG bit, which controls whether the comparator match causes a state sequencer transition immediately or tags the opcode at the matched address. If a comparator is enabled for tagged comparisons, the address stored in the comparator match address registers must be an opcode address.

Using Begin trigger together with tagging, if the tagged instruction is about to be executed then the transition to the next state sequencer state occurs. If the transition is to the Final State, tracing is started. Only upon completion of the tracing session can a breakpoint be generated. Using End alignment, when the tagged instruction is about to be executed and the next transition is to Final State then a breakpoint is generated immediately, before the tagged instruction is carried out.

R/W monitoring, access size (SZ) monitoring and data bus monitoring are not useful if tagging is selected, since the tag is attached to the opcode at the matched address and is not dependent on the data bus nor on the type of access. Thus these bits are ignored if tagging is selected.

When configured for range comparisons and tagging, the ranges are accurate only to word boundaries.

Tagging is disabled when the BDM becomes active.

8.4.7 Breakpoints

It is possible to generate breakpoints from channel transitions to final state or using software to write to the TRIG bit in the DBGC1 register.

8.4.7.1 Breakpoints From Comparator Channels

Breakpoints can be generated when the state sequencer transitions to the Final State. If configured for tagging, then the breakpoint is generated when the tagged opcode reaches the execution stage of the instruction queue.

If a tracing session is selected by the TSOURCE bit, breakpoints are requested when the tracing session has completed, thus if Begin aligned triggering is selected, the breakpoint is requested only on completion of the subsequent trace (see Table 8-42). If no tracing session is selected, breakpoints are requested immediately.

If the BRK bit is set, then the associated breakpoint is generated immediately independent of tracing trigger alignment.

Table 8-42. Breakpoint Setup For CPU Breakpoints

BRK	TALIGN	DBGBRK	Breakpoint Alignment
0	0	0	Fill Trace Buffer until trigger then disarm (no breakpoints)
0	0	1	Fill Trace Buffer until trigger, then breakpoint request occurs
0	1	0	Start Trace Buffer at trigger (no breakpoints)

10.3.2.15 Autonomous Clock Trimming Register (CPMUACLKTR)

The CPMUACLKTR register configures the trimming of the Autonomous Clock (ACLK - trimmable internal RC-Oscillator) which can be selected as clock source for some CPMU features.

0x02F3

	7	6	5	4	3	2	1	0
R	ACLKTR5	ACLKTR4	ACLKTR3	ACLKTR2	ACLKTR1	ACLKTR0	0	0
W								
Reset	F	F	F	F	F	F	0	0

After de-assert of System Reset a value is automatically loaded from the Flash memory.

Figure 10-19. Autonomous Periodical Interrupt Trimming Register (CPMUACLKTR)

Read: Anytime

Write: Anytime

Table 10-17. CPMUACLKTR Field Descriptions

Field	Description
7–2 ACLKTR[5:0]	**Autonomous Clock Trimming Bits** — See Table 10-18 for trimming effects. The ACLKTR[5:0] value represents a signed number influencing the ACLK period time.

Table 10-18. Trimming Effect of ACLKTR

Bit	Trimming Effect
ACLKTR[5]	Increases period
ACLKTR[4]	Decreases period less than ACLKTR[5] increased it
ACLKTR[3]	Decreases period less than ACLKTR[4]
ACLKTR[2]	Decreases period less than ACLKTR[3]
ACLKTR[1]	Decreases period less than ACLKTR[2]
ACLKTR[0]	Decreases period less than ACLKTR[1]

10.3.2.16 Autonomous Periodical Interrupt Rate High and Low Register (CPMUAPIRH / CPMUAPIRL)

The CPMUAPIRH and CPMUAPIRL registers allow the configuration of the autonomous periodical interrupt rate.

10.4 Functional Description

10.4.1 Phase Locked Loop with Internal Filter (PLL)

The PLL is used to generate a high speed PLLCLK based on a low frequency REFCLK.

The REFCLK is by default the IRCCLK which is trimmed to f_{IRC1M_TRIM}=1MHz.

If using the oscillator (OSCE=1) REFCLK will be based on OSCCLK. For increased flexibility, OSCCLK can be divided in a range of 1 to 16 to generate the reference frequency REFCLK using the REFDIV[3:0] bits. Based on the SYNDIV[5:0] bits the PLL generates the VCOCLK by multiplying the reference clock by a 2, 4, 6,... 126, 128. Based on the POSTDIV[4:0] bits the VCOCLK can be divided in a range of 1,2, 3, 4, 5, 6,... to 32 to generate the PLLCLK.

If oscillator is enabled (OSCE=1) $$f_{REF} = \frac{f_{OSC}}{(REFDIV + 1)}$$

If oscillator is disabled (OSCE=0) $$f_{REF} = f_{IRC1M}$$

$$f_{VCO} = 2 \times f_{REF} \times (SYNDIV + 1)$$

If PLL is locked (LOCK=1) $$f_{PLL} = \frac{f_{VCO}}{(POSTDIV + 1)}$$

If PLL is not locked (LOCK=0) $$f_{PLL} = \frac{f_{VCO}}{4}$$

If PLL is selected (PLLSEL=1) $$f_{bus} = \frac{f_{PLL}}{2}$$

NOTE

Although it is possible to set the dividers to command a very high clock frequency, do not exceed the specified bus frequency limit for the MCU.

Several examples of PLL divider settings are shown in Table 10-25. The following rules help to achieve optimum stability and shortest lock time:

- Use lowest possible f_{VCO} / f_{REF} ratio (SYNDIV value).
- Use highest possible REFCLK frequency f_{REF}.

Table 10-25. Examples of PLL Divider Settings

f_{osc}	REFDIV[3:0]	f_{REF}	REFFRQ[1:0]	SYNDIV[5:0]	f_{VCO}	VCOFRQ[1:0]	POSTDIV[4:0]	f_{PLL}	f_{bus}
off	$00	1MHz	00	$18	50MHz	01	$03	12.5MHz	6.25MHz

15.2 Signal Description

This section lists all inputs to the ADC10B16C block.

15.2.1 Detailed Signal Descriptions

15.2.1.1 AN*x* (*x* = 15, 14, 13, 12, 11, 10, 9, 8, 7, 6, 5, 4, 3, 2, 1, 0)

This pin serves as the analog input Channel *x*. It can also be configured as digital port or external trigger for the ATD conversion.

15.2.1.2 ETRIG3, ETRIG2, ETRIG1, ETRIG0

These inputs can be configured to serve as an external trigger for the ATD conversion.

Refer to device specification for availability and connectivity of these inputs!

15.2.1.3 VRH, VRL

VRH is the high reference voltage, VRL is the low reference voltage for ATD conversion.

15.2.1.4 VDDA, VSSA

These pins are the power supplies for the analog circuitry of the ADC10B16C block.

15.3 Memory Map and Register Definition

This section provides a detailed description of all registers accessible in the ADC10B16C.

15.3.1 Module Memory Map

Figure 15-2 gives an overview on all ADC10B16C registers.

NOTE

Register Address = Base Address + Address Offset, where the Base Address is defined at the MCU level and the Address Offset is defined at the module level.

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0000	ATDCTL0	R W	Reserved	0	0	0	WRAP3	WRAP2	WRAP1	WRAP0
0x0001	ATDCTL1	R W	ETRIGSEL	SRES1	SRES0	SMP_DIS	ETRIGCH3	ETRIGCH2	ETRIGCH1	ETRIGCH0
0x0002	ATDCTL2	R W	0	AFFC	Reserved	ETRIGLE	ETRIGP	ETRIGE	ASCIE	ACMPIE

= Unimplemented or Reserved

Figure 15-2. ADC10B16C Register Summary (Sheet 1 of 3)

Module Base + 0x0004 Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	WUPIF	CSCIF	RSTAT1	RSTAT0	TSTAT1	TSTAT0	OVRIF	RXF
W								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 18-8. MSCAN Receiver Flag Register (CANRFLG)

1 Read: Anytime
Write: Anytime when not in initialization mode, except RSTAT[1:0] and TSTAT[1:0] flags which are read-only; write of 1 clears flag; write of 0 is ignored

NOTE

The CANRFLG register is held in the reset state[1] when the initialization mode is active (INITRQ = 1 and INITAK = 1). This register is writable again as soon as the initialization mode is exited (INITRQ = 0 and INITAK = 0).

Table 18-11. CANRFLG Register Field Descriptions

Field	Description
7 WUPIF	**Wake-Up Interrupt Flag** — If the MSCAN detects CAN bus activity while in sleep mode (see Section 18.4.5.5, “MSCAN Sleep Mode,”) and WUPE = 1 in CANTCTL0 (see Section 18.3.2.1, “MSCAN Control Register 0 (CANCTL0)”), the module will set WUPIF. If not masked, a wake-up interrupt is pending while this flag is set. 0 No wake-up activity observed while in sleep mode 1 MSCAN detected activity on the CAN bus and requested wake-up
6 CSCIF	**CAN Status Change Interrupt Flag** — This flag is set when the MSCAN changes its current CAN bus status due to the actual value of the transmit error counter (TEC) and the receive error counter (REC). An additional 4-bit (RSTAT[1:0], TSTAT[1:0]) status register, which is split into separate sections for TEC/REC, informs the system on the actual CAN bus status (see Section 18.3.2.6, “MSCAN Receiver Interrupt Enable Register (CANRIER)”). If not masked, an error interrupt is pending while this flag is set. CSCIF provides a blocking interrupt. That guarantees that the receiver/transmitter status bits (RSTAT/TSTAT) are only updated when no CAN status change interrupt is pending. If the TECs/RECs change their current value after the CSCIF is asserted, which would cause an additional state change in the RSTAT/TSTAT bits, these bits keep their status until the current CSCIF interrupt is cleared again. 0 No change in CAN bus status occurred since last interrupt 1 MSCAN changed current CAN bus status
5-4 RSTAT[1:0]	**Receiver Status Bits** — The values of the error counters control the actual CAN bus status of the MSCAN. As soon as the status change interrupt flag (CSCIF) is set, these bits indicate the appropriate receiver related CAN bus status of the MSCAN. The coding for the bits RSTAT1, RSTAT0 is: 00 RxOK: $0 \le$ receive error counter < 96 01 RxWRN: $96 \le$ receive error counter < 128 10 RxERR: $128 \le$ receive error counter *11 Bus-off*[1]*: $256 \le$ transmit error counter*

1. The RSTAT[1:0], TSTAT[1:0] bits are not affected by initialization mode.

18.3.3.1.1 IDR0–IDR3 for Extended Identifier Mapping

Module Base + 0x00X0

	7	6	5	4	3	2	1	0
R W	ID28	ID27	ID26	ID25	ID24	ID23	ID22	ID21
Reset:	x	x	x	x	x	x	x	x

Figure 18-26. Identifier Register 0 (IDR0) — Extended Identifier Mapping

Table 18-27. IDR0 Register Field Descriptions — Extended

Field	Description
7-0 ID[28:21]	**Extended Format Identifier** — The identifiers consist of 29 bits (ID[28:0]) for the extended format. ID28 is the most significant bit and is transmitted first on the CAN bus during the arbitration procedure. The priority of an identifier is defined to be highest for the smallest binary number.

Module Base + 0x00X1

	7	6	5	4	3	2	1	0
R W	ID20	ID19	ID18	SRR (=1)	IDE (=1)	ID17	ID16	ID15
Reset:	x	x	x	x	x	x	x	x

Figure 18-27. Identifier Register 1 (IDR1) — Extended Identifier Mapping

Table 18-28. IDR1 Register Field Descriptions — Extended

Field	Description
7-5 ID[20:18]	**Extended Format Identifier —** The identifiers consist of 29 bits (ID[28:0]) for the extended format. ID28 is the most significant bit and is transmitted first on the CAN bus during the arbitration procedure. The priority of an identifier is defined to be highest for the smallest binary number.
4 SRR	**Substitute Remote Request** — This fixed recessive bit is used only in extended format. It must be set to 1 by the user for transmission buffers and is stored as received on the CAN bus for receive buffers.
3 IDE	**ID Extended** — This flag indicates whether the extended or standard identifier format is applied in this buffer. In the case of a receive buffer, the flag is set as received and indicates to the CPU how to process the buffer identifier registers. In the case of a transmit buffer, the flag indicates to the MSCAN what type of identifier to send. 0 Standard format (11 bit) 1 Extended format (29 bit)
2-0 ID[17:15]	**Extended Format Identifier —** The identifiers consist of 29 bits (ID[28:0]) for the extended format. ID28 is the most significant bit and is transmitted first on the CAN bus during the arbitration procedure. The priority of an identifier is defined to be highest for the smallest binary number.

20.1.2 Features

The SCI includes these distinctive features:

- Full-duplex or single-wire operation
- Standard mark/space non-return-to-zero (NRZ) format
- Selectable IrDA 1.4 return-to-zero-inverted (RZI) format with programmable pulse widths
- 13-bit baud rate selection
- Programmable 8-bit or 9-bit data format
- Separately enabled transmitter and receiver
- Programmable polarity for transmitter and receiver
- Programmable transmitter output parity
- Two receiver wakeup methods:
  - Idle line wakeup
  - Address mark wakeup
- Interrupt-driven operation with eight flags:
  - Transmitter empty
  - Transmission complete
  - Receiver full
  - Idle receiver input
  - Receiver overrun
  - Noise error
  - Framing error
  - Parity error
  - Receive wakeup on active edge
  - Transmit collision detect supporting LIN
  - Break Detect supporting LIN
- Receiver framing error detection
- Hardware parity checking
- 1/16 bit-time noise detection

20.1.3 Modes of Operation

The SCI functions the same in normal, special, and emulation modes. It has two low power modes, wait and stop modes.

- Run mode
- Wait mode
- Stop mode

Offset Module Base + 0x0012

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 24-23. Flash Reserved6 Register (FRSV6)

All bits in the FRSV6 register read 0 and are not writable.

24.3.2.19 Flash Reserved7 Register (FRSV7)

This Flash register is reserved for factory testing.

Offset Module Base + 0x0013

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 24-24. Flash Reserved7 Register (FRSV7)

All bits in the FRSV7 register read 0 and are not writable.

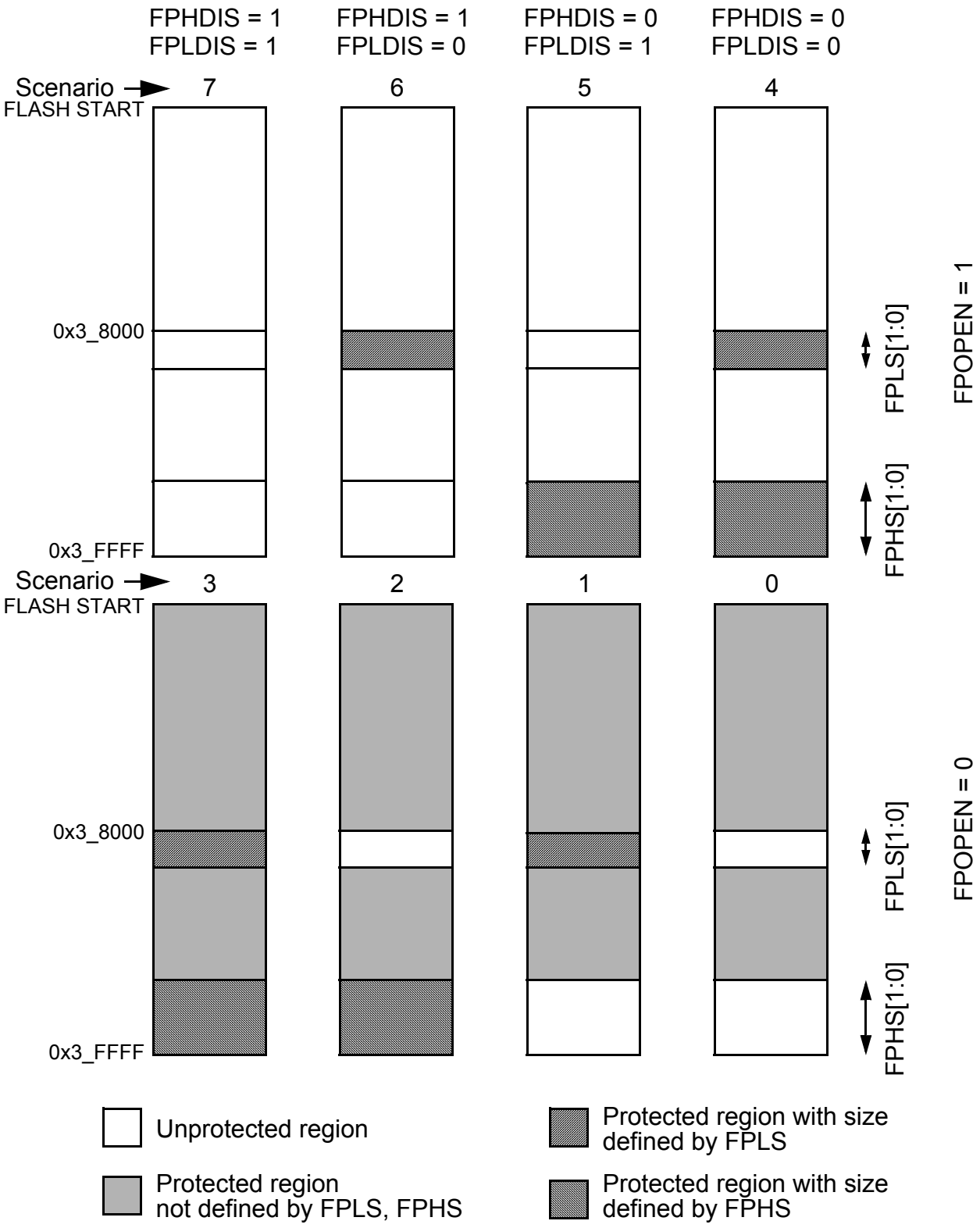


Figure 29-14. P-Flash Protection Scenarios

29.4.6 Flash Command Description

This section provides details of all available Flash commands launched by a command write sequence. The ACCERR bit in the FSTAT register will be set during the command write sequence if any of the following illegal steps are performed, causing the command not to be processed by the Memory Controller:

- Starting any command write sequence that programs or erases Flash memory before initializing the FCLKDIV register
- Writing an invalid command as part of the command write sequence
- For additional possible errors, refer to the error handling table provided for each command

If a Flash block is read during execution of an algorithm (CCIF = 0) on that same block, the read operation will return invalid data if both flags SFDIF and DFDIF are set. If the SFDIF or DFDIF flags were not previously set when the invalid read operation occurred, both the SFDIF and DFDIF flags will be set.

If the ACCERR or FPVIOL bits are set in the FSTAT register, the user must clear these bits before starting any command write sequence (see Section 29.3.2.7).

CAUTION

A Flash word or phrase must be in the erased state before being programmed. Cumulative programming of bits within a Flash word or phrase is not allowed.

29.4.6.1 Erase Verify All Blocks Command

The Erase Verify All Blocks command will verify that all P-Flash and EEPROM blocks have been erased.

Table 29-31. Erase Verify All Blocks Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x01	Not required

Upon clearing CCIF to launch the Erase Verify All Blocks command, the Memory Controller will verify that the entire Flash memory space is erased. The CCIF flag will set after the Erase Verify All Blocks operation has completed. If all blocks are not erased, it means blank check failed, both MGSTAT bits will be set.

Table 29-32. Erase Verify All Blocks Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 000 at command launch
	FPVIOL	None
	MGSTAT1	Set if any errors have been encountered during the reador if blank check failed .
	MGSTAT0	Set if any non-correctable errors have been encountered during the read or if blank check failed.

Chapter 30
192 KByte Flash Module (S12FTMRG192K2V1)

Table 30-1. Revision History

Revision Number	Revision Date	Sections Affected	Description of Changes
V01.06	23 Jun 2010	30.4.6.2/30-1107 30.4.6.12/30-1114 30.4.6.13/30-1115	Updated description of the commands RD1BLK, MLOADU and MLOADF
V01.07	20 aug 2010	30.4.6.2/30-1107 30.4.6.12/30-1114 30.4.6.13/30-1115	Updated description of the commands RD1BLK, MLOADU and MLOADF
Rev.1.27	31 Jan 2011	30.3.2.9/30-1090	Updated description of protection on Section 30.3.2.9

30.1 Introduction

The FTMRG192K2 module implements the following:

- 192Kbytes of P-Flash (Program Flash) memory
- 4Kbytes of EEPROM memory

The Flash memory is ideal for single-supply applications allowing for field reprogramming without requiring external high voltage sources for program or erase operations. The Flash module includes a memory controller that executes commands to modify Flash memory contents. The user interface to the memory controller consists of the indexed Flash Common Command Object (FCCOB) register which is written to with the command, global address, data, and any required command parameters. The memory controller must complete the execution of a command before the FCCOB register can be written to with a new command.

CAUTION

A Flash word or phrase must be in the erased state before being programmed. Cumulative programming of bits within a Flash word or phrase is not allowed.

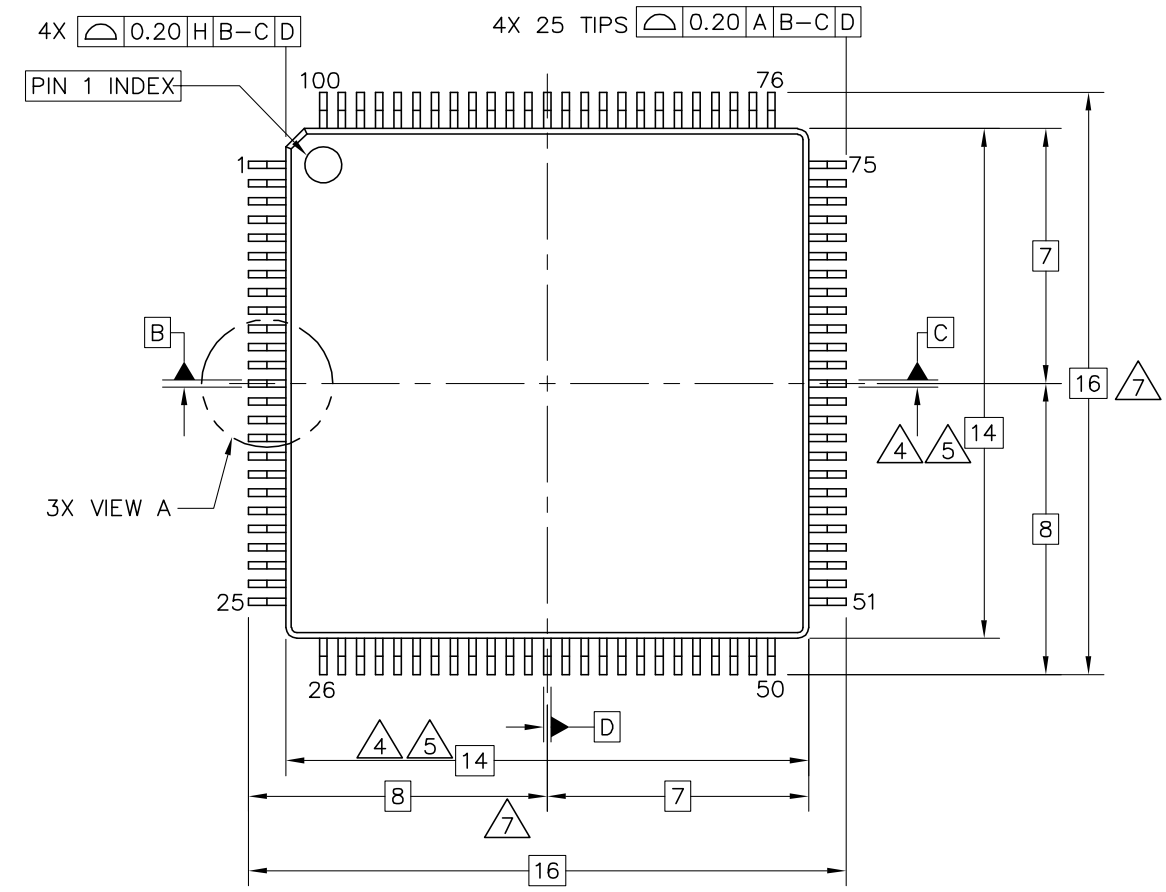
Table A-8. 5-V I/O Characteristics (Junction Temperature From –40°C To +150°C)

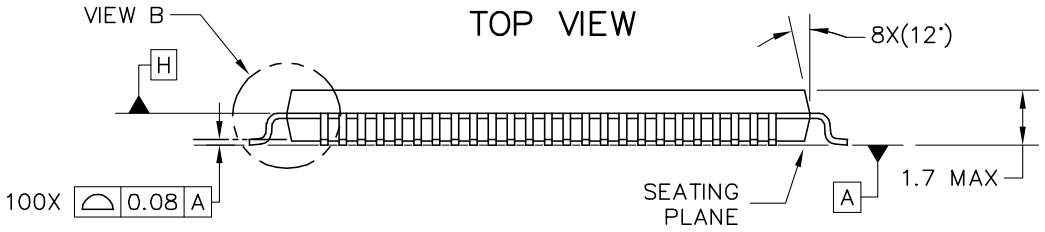
Conditions are 4.5 V < V_{DD35} < 5.5 V junction temperature from –40°C to +150°C, unless otherwise noted I/O Characteristics for all I/O pins except EXTAL, XTAL,TEST and supply pins.							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	P	Input high voltage	V_{IH}	0.65*V_{DD35}	—	—	V
2	T	Input high voltage	V_{IH}	—	—	V_{DD35}+0.3	V
3	P	Input low voltage	V_{IL}	—	—	0.35*V_{DD35}	V
4	T	Input low voltage	V_{IL}	V_{SSRX}–0.3	—	—	V
5	C	Input hysteresis	V_{HYS}	0.06*V_{DD35}	—	0.3*V_{DD35}	mV
6	P	Input leakage current (pins in high impedance input mode)[1] V_{in} = V_{DD35} or V_{SS35} +125°C to < T_J < 150°C +105°C to < T_J < 125° –40°C to < T_J < 105°C	I_{in}	 -1 -0.5 -0.4	 — — —	 1 0.5 0.4	µA
7	P	Output high voltage (pins in output mode) I_{OH} = –4 mA	V_{OH}	V_{DD35} – 0.8	—	—	V
8	P	Output low voltage (pins in output mode) I_{OL} = +4mA	V_{OL}	—	—	0.8	V
9	P	Internal pull up current V_{IH} min > input voltage > V_{IL} max	I_{PUL}	-10	—	-130	µA
10	P	Internal pull down current V_{IH} min > input voltage > V_{IL} max	I_{PDH}	10	—	130	µA
11	D	Input capacitance	C_{in}	—	7	—	pF
12	T	Injection current[2] Single pin limit Total device Limit, sum of all injected currents	 I_{ICS} I_{ICP}	 –2.5 –25	—	 2.5 25	mA

1 Maximum leakage current occurs at maximum operating temperature. Current decreases by approximately one-half for each 8°°C to 12°C° in the temperature range from 50°C to 125°C.

2 Refer to Section A.1.4, “Current Injection” for more details

D.1 100 LQFP Mechanical Dimensions





SIDE VIEW

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TITLE: 100 LEAD LQFP 14 X 14, 0.5 PITCH, 1.4 THICK	DOCUMENT NO: 98ASS23308W	REV: H
	CASE NUMBER: 983–02	25 MAY 2005
	STANDARD: NON–JEDEC	