Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	12V1
Core Size	16-Bit
Speed	25MHz
Connectivity	CANbus, IrDA, LINbus, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	86
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	3K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3.13V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s9s12g96f0cll

Chapter 26
48 KByte Flash Module (S12FTMRG48K1V1)

Chapter 27
64 KByte Flash Module (S12FTMRG64K1V1)

Table 1-15. 32-Pin LQFP Pinout for S12G48 and S12G64

	Function <----lowest-----PRIORITY-----highest---->					Power Supply	Internal Pull Resistor	
Package Pin	Pin	2nd Func.	3rd Func.	4th Func	5th Func		CTRL	Reset State
2	VDDXRA	VRH	—	—	—	—	—	—
3	VSSXA	—	—	—	—	—	—	—
4	PE0[1]	EXTAL	—	—	—	—	PUCR/PDPEE	Down
5	VSS	—	—	—	—	—	—	—
6	PE1[1]	XTAL	—	—	—	—	PUCR/PDPEE	Down
7	TEST	—	—	—	—	N.A.	$\overline{\text{RESET}}$ pin	Down
8	BKGD	MODC	—	—	—	V_{DDX}	PUCR/BKPUE	Up
9	PP0	KWP0	ETRIG0	API_EXTCLK	PWM0	V_{DDX}	PERP/PPSP	Disabled
10	PP1	KWP1	ETRIG1	ECLKX2	PWM1	V_{DDX}	PERP/PPSP	Disabled
11	PP2	KWP2	ETRIG2	PWM2	—	V_{DDX}	PERP/PPSP	Disabled
12	PP3	KWP3	ETRIG3	PWM3	—	V_{DDX}	PERP/PPSP	Disabled
13	PT3	IOC3	—	—	—	V_{DDX}	PERT/PPST	Disabled
14	PT2	IOC2	—	—	—	V_{DDX}	PERT/PPST	Disabled
15	PT1	IOC1	$\overline{\text{IRQ}}$	—	—	V_{DDX}	PERT/PPST	Disabled
16	PT0	IOC0	$\overline{\text{XIRQ}}$	—	—	V_{DDX}	PERT/PPST	Disabled
17	PAD0	KWAD0	AN0	—	—	V_{DDA}	PER1AD/PPS1AD	Disabled
18	PAD1	KWAD1	AN1	—	—	V_{DDA}	PER1AD/PPS1AD	Disabled
19	PAD2	KWAD2	AN2	—	—	V_{DDA}	PER1AD/PPS1AD	Disabled
20	PAD3	KWAD3	AN3	—	—	V_{DDA}	PER1AD/PPS1AD	Disabled
21	PAD4	KWAD4	AN4	—	—	V_{DDA}	PER1AD/PPS1AD	Disabled
22	PAD5	KWAD5	AN5	ACMPO	—	V_{DDA}	PER1AD/PPS1AD	Disabled
23	PAD6	KWAD6	AN6	ACMPP	—	V_{DDA}	PER1AD/PPS1AD	Disabled
24	PAD7	KWAD7	AN7	ACMPM	—	V_{DDA}	PER1AD/PPS1AD	Disabled
25	PS0	RXD0	—	—	—	V_{DDX}	PERS/PPSS	Up
26	PS1	TXD0	—	—	—	V_{DDX}	PERS/PPSS	Up
27	PS4	PWM4	MISO0	—	—	V_{DDX}	PERS/PPSS	Up
28	PS5	IOC4	MOSI0	—	—	V_{DDX}	PERS/PPSS	Up
29	PS6	IOC5	SCK0	—	—	V_{DDX}	PERS/PPSS	Up

Table 1-23. 48-Pin LQFP Pinout for S12GA96 and S12GA128

	Function <----lowest-----PRIORITY-----highest---->					Power Supply	Internal Pull Resistor	
Package Pin	Pin	2nd Func.	3rd Func.	4th Func	5th Func		CTRL	Reset State
2	VDDXR	—	—	—	—	—	—	—
3	VSSX	—	—	—	—	—	—	—
4	PE0[1]	EXTAL	—	—	—	V_{DDX}	PUCR/PDPEE	Down
5	VSS	—	—	—	—	—	—	—
6	PE1[1]	XTAL	—	—	—	V_{DDX}	PUCR/PDPEE	Down
7	TEST	—	—	—	—	N.A.	$\overline{\text{RESET}}$ pin	Down
8	PJ0	KWJ0	PWM6	MISO1	—	V_{DDX}	PERJ/PPSJ	Up
9	PJ1	KWJ1	IOC6	MOSI1	—	V_{DDX}	PERJ/PPSJ	Up
10	PJ2	KWJ2	IOC7	SCK1	—	V_{DDX}	PERJ/PPSJ	Up
11	PJ3	KWJ3	PWM7	$\overline{\text{SS1}}$	—	V_{DDX}	PERJ/PPSJ	Up
12	BKGD	MODC	—	—	—	V_{DDX}	PUCR/BKPUE	Up
13	PP0	KWP0	ETRIG0	API_EXTCLK	PWM0	V_{DDX}	PERP/PPSP	Disabled
14	PP1	KWP1	ETRIG1	ECLKX2	PWM1	V_{DDX}	PERP/PPSP	Disabled
15	PP2	KWP2	ETRIG2	PWM2	—	V_{DDX}	PERP/PPSP	Disabled
16	PP3	KWP3	ETRIG3	PWM3	—	V_{DDX}	PERP/PPSP	Disabled
17	PP4	KWP4	PWM4	—	—	V_{DDX}	PERP/PPSP	Disabled
18	PP5	KWP5	PWM5	—	—	V_{DDX}	PERP/PPSP	Disabled
19	PT5	IOC5	—	—	—	V_{DDX}	PERT/PPST	Disabled
20	PT4	IOC4	—	—	—	V_{DDX}	PERT/PPST	Disabled
21	PT3	IOC3	—	—	—	V_{DDX}	PERT/PPST	Disabled
22	PT2	IOC2	—	—	—	V_{DDX}	PERT/PPST	Disabled
23	PT1	IOC1	$\overline{\text{IRQ}}$	—	—	V_{DDX}	PERT/PPST	Disabled
24	PT0	IOC0	$\overline{\text{XIRQ}}$	—	—	V_{DDX}	PERT/PPST	Disabled
25	PAD0	KWAD0	AN0	—	—	V_{DDA}	PER1AD/PPS1AD	Disabled
26	PAD8	KWAD8	AN8	—	—	V_{DDA}	PER0AD/PPS0AD	Disabled
27	PAD1	KWAD1	AN1	—	—	V_{DDA}	PER1AD/PPS1AD	Disabled
28	PAD9	KWAD9	AN9		—	V_{DDA}	PER0AD/PPS0AD	Disabled
29	PAD2	KWAD2	AN2	—	—	V_{DDA}	PER1AD/PPS1AD	Disabled

1.12.3 Effects of Reset

When a reset occurs, MCU registers and control bits are initialized. Refer to the respective block sections for register reset states.

On each reset, the Flash module executes a reset sequence to load Flash configuration registers.

1.12.3.1 Flash Configuration Reset Sequence Phase

On each reset, the Flash module holds CPU activity while loading Flash module registers from the Flash memory. If double faults are detected in the reset phase, Flash module protection and security may be active on leaving reset. This is explained in more detail in the Flash module Section 29.1, “Introduction”.

1.12.3.2 Reset While Flash Command Active

If a reset occurs while any Flash command is in progress, that command will be immediately aborted. The state of the word being programmed or the sector/block being erased is not guaranteed.

1.12.3.3 I/O Pins

Refer to the PIM section for reset configurations of all peripheral module ports.

1.12.3.4 RAM

The RAM arrays are not initialized out of reset.

1.13 COP Configuration

The COP time-out rate bits CR[2:0] and the WCOP bit in the CPMUCOP register at address 0x003C are loaded from the Flash register FOPT. See Table 1-36 and Table 1-37 for coding. The FOPT register is loaded from the Flash configuration field byte at global address 0x3_FF0E during the reset sequence.

Table 1-36. Initial COP Rate Configuration

NV[2:0] in FOPT Register	CR[2:0] in CPMUCOP Register
000	111
001	110
010	101
011	100
100	011
101	010
110	001
111	000

2.3.9 Pins PM3-0

Table 2-13. Port M Pins PM3-0

PM3	• 64/100 LQFP: The SCI2 TXD signal is mapped to this pin when used with the SCI function. If the SCI2 TXD signal is enabled the I/O state will depend on the SCI2 configuration. • Signal priority: 64/100 LQFP: TXD2 > GPO
PM2	• 64/100 LQFP: The SCI2 RXD signal is mapped to this pin when used with the SCI function. If the SCI2 RXD signal is enabled the I/O state will be forced to be input. • Signal priority: 64/100 LQFP: RXD2 > GPO
PM1	• Except 20 TSSOP: The TXCAN signal is mapped to this pin when used with the CAN function. The enabled CAN forces the I/O state to be an output. • 32 LQFP: The SCI1 TXD signal is mapped to this pin when used with the SCI function. If the SCI1 TXD signal is enabled the I/O state will depend on the SCI1 configuration. • 48 LQFP: The SCI2 TXD signal is mapped to this pin when used with the SCI function. If the SCI2 TXD signal is enabled the I/O state will depend on the SCI2 configuration. • Signal priority: 32 LQFP: TXCAN > TXD1 > GPO 48 LQFP: TXCAN > TXD2 > GPO 64/100 LQFP: TXCAN > GPO
PM0	• Except 20 TSSOP: The RXCAN signal is mapped to this pin when used with the CAN function. The enabled CAN forces the I/O state to be an input. If CAN is active the selection of a pulldown device on the RXCAN input has no effect. • 32 LQFP: The SCI1 RXD signal is mapped to this pin when used with the SCI function. The enabled SCI1 RXD signal forces the I/O state to an input. • 48 LQFP: The SCI2 RXD signal is mapped to this pin when used with the SCI function. The enabled SCI2 RXD signal forces the I/O state to an input. • Signal priority: 32 LQFP: RXCAN > RXD1 > GPO 48 LQFP: RXCAN > RXD2 > GPO 64/100 LQFP: RXCAN > GPO

2.3.10 Pins PP7-0

Table 2-14. Port P Pins PP7-0

PP7-PP6	• 64/100 LQFP: The PWM channels 7 and 6 signal are mapped to these pins when used with the PWM function. The enabled PWM channel forces the I/O state to be an output. • 64/100 LQFP: Pin interrupts can be generated if enabled in input or output mode. • Signal priority: 64/100 LQFP: PWM > GPO
PP5-PP4	• 48/64/100 LQFP: The PWM channels 5 and 4 signal are mapped to these pins when used with the PWM function. The enabled PWM channel forces the I/O state to be an output. • 48/64/100 LQFP: Pin interrupts can be generated if enabled in input or output mode. • Signal priority: 48/64/100 LQFP: PWM > GPO

Table 2-21. Block Register Map (G3) (continued)

Global Address Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x000E–0x001B Non-PIM Address Range	R W	Non-PIM Address Range							
0x001C ECLKCTL	R	NECLK	NCLKX2	DIV16	EDIV4	EDIV3	EDIV2	EDIV1	EDIV0
	W								
0x001D Reserved	R	0	0	0	0	0	0	0	0
	W								
0x001E IRQCR	R	IRQE	IRQEN	0	0	0	0	0	0
	W								
0x001F Reserved	R	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	W								
0x0020–0x023F Non-PIM Address Range	R W	Non-PIM Address Range							
0x0240 PTT	R	0	0	PTT5	PTT4	PTT3	PTT2	PTT1	PTT0
	W								
0x0241 PTIT	R	0	0	PTIT5	PTIT4	PTIT3	PTIT2	PTIT1	PTIT0
	W								
0x0242 DDRT	R	0	0	DDRT5	DDRT4	DDRT3	DDRT2	DDRT1	DDRT0
	W								
0x0243 Reserved	R	0	0	0	0	0	0	0	0
	W								
0x0244 PERT	R	0	0	PERT5	PERT4	PERT3	PERT2	PERT1	PERT0
	W								
0x0245 PPST	R	0	0	PPST5	PPST4	PPST3	PPST2	PPST1	PPST0
	W								
0x0246 Reserved	R	0	0	0	0	0	0	0	0
	W								
0x0247 Reserved	R	0	0	0	0	0	0	0	0
	W								
0x0248 PTS	R	PTS7	PTS6	PTS5	PTS4	PTS3	PTS2	PTS1	PTS0
	W								

= Unimplemented or Reserved

[1] Read: Anytime
Write:
IRQE: Once in normal mode, anytime in special mode
IRQEN: Anytime

Table 2-34. IRQCR Register Field Descriptions

Field	Description
7 IRQE	**IRQ select edge sensitive only—** 1 $\overline{\text{IRQ}}$ pin configured to respond only to falling edges. Falling edges on the $\overline{\text{IRQ}}$ pin are detected anytime when IRQE=1 and will be cleared only upon a reset or the servicing of the IRQ interrupt. 0 $\overline{\text{IRQ}}$ pin configured for low level recognition
6 IRQEN	**IRQ enable—** 1 $\overline{\text{IRQ}}$ pin is connected to interrupt logic 0 $\overline{\text{IRQ}}$ pin is disconnected from interrupt logic

NOTE

If the input is driven to active level ($\overline{\text{IRQ}}$=0) a write access to set either IRQCR[IRQEN] and IRQCR[IRQE] to 1 simultaneously or to set IRQCR[IRQEN] to 1 when IRQCR[IRQE]=1 causes an IRQ interrupt to be generated if the I-bit is cleared. Refer to Section 2.6.3, “Enabling IRQ edge-sensitive mode”.

2.4.3.14 Reserved Register

Address 0x001F Access: User read/write[1]

	7	6	5	4	3	2	1	0
R W	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Reset	x	x	x	x	x	x	x	x

Figure 2-15. Reserved Register

[1] Read: Anytime
Write: Only in special mode

These reserved registers are designed for factory test purposes only and are not intended for general user access. Writing to these registers when in special mode can alter the module’s functionality.

Table 2-88. PIE1AD Register Field Descriptions

Field	Description
7-0 PIE1AD	**Port AD interrupt enable**— This bit enables or disables the edge sensitive pin interrupt on the associated pin. An interrupt can be generated if the pin is operating in input or output mode when in use with the general-purpose or related peripheral function. 1 Interrupt is enabled 0 Interrupt is disabled (interrupt flag masked)

2.4.3.63 Port AD Interrupt Flag Register (PIF0AD)

Address 0x027E (G1, G2) Access: User read/write[1]

	7	6	5	4	3	2	1	0
R W	PIF0AD7	PIF0AD6	PIF0AD5	PIF0AD4	PIF0AD3	PIF0AD2	PIF0AD1	PIF0AD0
Reset	0	0	0	0	0	0	0	0

Address 0x027E (G3) Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	0	0	0	0	PIF0AD3	PIF0AD2	PIF0AD1	PIF0AD0
W								
Reset	0	0	0	0	0	0	0	0

Figure 2-62. Port AD Interrupt Flag Register (PIF0AD)

[1] Read: Anytime
Write: Anytime, write 1 to clear

Table 2-89. PIF0AD Register Field Descriptions

Field	Description
7-0 PIF0AD	**Port AD interrupt flag**— This flag asserts after a valid active edge was detected on the related pin (see Section 2.5.4.2, “Pin Interrupts and Wakeup”). This can be a rising or a falling edge based on the state of the polarity select register. An interrupt will occur if the associated interrupt enable bit is set. Writing a logic “1” to the corresponding bit field clears the flag. 1 Active edge on the associated bit has occurred 0 No active edge occurred

Table 3-2. ACMPC Register Field Descriptions (continued)

Field	Description
5 ACICE	ACMP Input Capture Enable— Establishes internal link to a timer input capture channel. When enabled, the associated timer pin is disconnected from the timer input. Refer to ACE description to account for initialization delay on this path. 0 Timer link disabled 1 ACMP output connected to input capture channel 5
4 ACDIEN	ACMP Digital Input Buffer Enable— Enables the input buffers on ACMPP and ACMPM for the pins to be used with digital functions. **Note:** If this bit is set while simultaneously using the pin as an analog port, there is potentially increased power consumption because the digital input buffer may be in the linear region. 0 Input buffers disabled on ACMPP and ACMPM 1 Input buffers enabled on ACMPP and ACMPM
3-2 ACMOD [1:0]	ACMP Mode— Selects the type of compare event setting ACIF. 00 Flag setting disabled 01 Comparator output rising edge 10 Comparator output falling edge 11 Comparator output rising or falling edge
0 ACE	ACMP Enable— This bit enables the ACMP module and takes it into normal mode (see Section 3.5, “Modes of Operation”). This bit also connects the related input pins with the module’s low pass input filters. When the module is not enabled, it remains in low power shutdown mode. **Note:** After setting ACE=1 an initialization delay of 63 bus clock cycles must be accounted for. During this time the comparator output path to all subsequent logic (ACO, ACIF, timer link, excl. ACMPO) is held at its current state. When resetting ACE to 0 the current state of the comparator will be maintained. 0 ACMP disabled 1 ACMP enabled

3.6.2.2 ACMP Status Register (ACMPS)

Address 0x0261 Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	ACIF	ACO	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

Figure 3-4. ACMP Status Register (ACMPS)

[1] Read: Anytime
Write:
ACIF: Anytime, write 1 to clear
ACO: Never

4.6 Memory Map and Register Definition

4.6.1 Register Map

Table 4-1 shows the RVA register map.

Table 4-1. RVA Register Map

Global Address Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0276 RVACTL	R	0	0	0	0	0	0	0	RVAON
	W								

= Unimplemented or Reserved

4.6.2 Register Descriptions

4.6.2.1 RVA Control Register (RVACTL)

Address 0x0276 Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	RVAON
W								
Reset	0	0	0	0	0	0	0	0

Figure 4-2. RVA Control Register (RVACTL)

[1] Read: Anytime
Write: Anytime

Table 4-2. RVACTL Register Field Descriptions

Field	Description
0 RVAON	RVA On — This bit turns on the reference voltage attenuation. 0 RVA in bypass mode 1 RVA in attenuation mode

NOTE

This information is being provided so that the MCU integrator will be aware that such a conflict could occur.

The hardware handshake protocol is enabled by the ACK_ENABLE and disabled by the ACK_DISABLE BDM commands. This provides backwards compatibility with the existing POD devices which are not able to execute the hardware handshake protocol. It also allows for new POD devices, that support the hardware handshake protocol, to freely communicate with the target device. If desired, without the need for waiting for the ACK pulse.

The commands are described as follows:

- ACK_ENABLE — enables the hardware handshake protocol. The target will issue the ACK pulse when a CPU command is executed by the CPU. The ACK_ENABLE command itself also has the ACK pulse as a response.
- ACK_DISABLE — disables the ACK pulse protocol. In this case, the host needs to use the worst case delay time at the appropriate places in the protocol.

The default state of the BDM after reset is hardware handshake protocol disabled.

All the read commands will ACK (if enabled) when the data bus cycle has completed and the data is then ready for reading out by the BKGD serial pin. All the write commands will ACK (if enabled) after the data has been received by the BDM through the BKGD serial pin and when the data bus cycle is complete. See Section 7.4.3, “BDM Hardware Commands” and Section 7.4.4, “Standard BDM Firmware Commands” for more information on the BDM commands.

The ACK_ENABLE sends an ACK pulse when the command has been completed. This feature could be used by the host to evaluate if the target supports the hardware handshake protocol. If an ACK pulse is issued in response to this command, the host knows that the target supports the hardware handshake protocol. If the target does not support the hardware handshake protocol the ACK pulse is not issued. In this case, the ACK_ENABLE command is ignored by the target since it is not recognized as a valid command.

The BACKGROUND command will issue an ACK pulse when the CPU changes from normal to background mode. The ACK pulse related to this command could be aborted using the SYNC command.

The GO command will issue an ACK pulse when the CPU exits from background mode. The ACK pulse related to this command could be aborted using the SYNC command.

The GO_UNTIL command is equivalent to a GO command with exception that the ACK pulse, in this case, is issued when the CPU enters into background mode. This command is an alternative to the GO command and should be used when the host wants to trace if a breakpoint match occurs and causes the CPU to enter active background mode. Note that the ACK is issued whenever the CPU enters BDM, which could be caused by a breakpoint match or by a BGND instruction being executed. The ACK pulse related to this command could be aborted using the SYNC command.

The TRACE1 command has the related ACK pulse issued when the CPU enters background active mode after one instruction of the application program is executed. The ACK pulse related to this command could be aborted using the SYNC command.

register bytes (three address bus compare registers and a control register). Comparator C consists of four register bytes (three address bus compare registers and a control register).

Each set of comparator registers can be accessed using the COMRV bits in the DBGC1 register. Unimplemented registers (e.g. Comparator B data bus and data bus masking) read as zero and cannot be written. The control register for comparator B differs from those of comparators A and C.

Table 8-21. Comparator Register Layout

0x0028	CONTROL	Read/Write	Comparators A,B and C
0x0029	ADDRESS HIGH	Read/Write	Comparators A,B and C
0x002A	ADDRESS MEDIUM	Read/Write	Comparators A,B and C
0x002B	ADDRESS LOW	Read/Write	Comparators A,B and C
0x002C	DATA HIGH COMPARATOR	Read/Write	Comparator A only
0x002D	DATA LOW COMPARATOR	Read/Write	Comparator A only
0x002E	DATA HIGH MASK	Read/Write	Comparator A only
0x002F	DATA LOW MASK	Read/Write	Comparator A only

8.3.2.8.1 Debug Comparator Control Register (DBGXCTL)

The contents of this register bits 7 and 6 differ depending upon which comparator registers are visible in the 8-byte window of the DBG module register address map.

Address: 0x0028

	7	6	5	4	3	2	1	0
R W	SZE	SZ	TAG	BRK	RW	RWE	NDB	COMPE
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 8-13. Debug Comparator Control Register DBGACTL (Comparator A)

Address: 0x0028

	7	6	5	4	3	2	1	0
R W	SZE	SZ	TAG	BRK	RW	RWE	0	COMPE
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 8-14. Debug Comparator Control Register DBGBCTL (Comparator B)

Address: 0x0028

	7	6	5	4	3	2	1	0
R W	0	0	TAG	BRK	RW	RWE	0	COMPE
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 8-15. Debug Comparator Control Register DBGCCTL (Comparator C)

14.3.2.7 ATD Status Register 0 (ATDSTAT0)

This register contains the Sequence Complete Flag, overrun flags for external trigger and FIFO mode, and the conversion counter.

Module Base + 0x0006

	7	6	5	4	3	2	1	0
R	SCF	0	ETORF	FIFOR	CC3	CC2	CC1	CC0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 14-9. ATD Status Register 0 (ATDSTAT0)

Read: Anytime

Write: Anytime (No effect on (CC3, CC2, CC1, CC0))

Table 14-16. ATDSTAT0 Field Descriptions

Field	Description
7 SCF	**Sequence Complete Flag** — This flag is set upon completion of a conversion sequence. If conversion sequences are continuously performed (SCAN=1), the flag is set after each one is completed. This flag is cleared when one of the following occurs: A) Write “1” to SCF B) Write to ATDCTL5 (a new conversion sequence is started) C) If AFFC=1 and a result register is read 0 Conversion sequence not completed 1 Conversion sequence has completed
5 ETORF	**External Trigger Overrun Flag** — While in edge sensitive mode (ETRIGLE=0), if additional active edges are detected while a conversion sequence is in process the overrun flag is set. This flag is cleared when one of the following occurs: A) Write “1” to ETORF B) Write to ATDCTL0,1,2,3,4, ATDCMPE or ATDCMPHT (a conversion sequence is aborted) C) Write to ATDCTL5 (a new conversion sequence is started) 0 No External trigger overrun error has occurred 1 External trigger overrun error has occurred
4 FIFOR	**Result Register Overrun Flag** — This bit indicates that a result register has been written to before its associated conversion complete flag (CCF) has been cleared. This flag is most useful when using the FIFO mode because the flag potentially indicates that result registers are out of sync with the input channels. However, it is also practical for non-FIFO modes, and indicates that a result register has been overwritten before it has been read (i.e. the old data has been lost). This flag is cleared when one of the following occurs: A) Write “1” to FIFOR B) Write to ATDCTL0,1,2,3,4, ATDCMPE or ATDCMPHT (a conversion sequence is aborted) C) Write to ATDCTL5 (a new conversion sequence is started) 0 No overrun has occurred 1 Overrun condition exists (result register has been written while associated CCFx flag was still set)

Table 18-4. CANCTL1 Register Field Descriptions (continued)

Field	Description
1 SLPAK	**Sleep Mode Acknowledge** — This flag indicates whether the MSCAN module has entered sleep mode (see Section 18.4.5.5, “MSCAN Sleep Mode”). It is used as a handshake flag for the SLPRQ sleep mode request. Sleep mode is active when SLPRQ = 1 and SLPAK = 1. Depending on the setting of WUPE, the MSCAN will clear the flag if it detects activity on the CAN bus while in sleep mode. 0 Running — The MSCAN operates normally 1 Sleep mode active — The MSCAN has entered sleep mode
0 INITAK	**Initialization Mode Acknowledge** — This flag indicates whether the MSCAN module is in initialization mode (see Section 18.4.4.5, “MSCAN Initialization Mode”). It is used as a handshake flag for the INITRQ initialization mode request. Initialization mode is active when INITRQ = 1 and INITAK = 1. The registers CANCTL1, CANBTR0, CANBTR1, CANIDAC, CANIDAR0–CANIDAR7, and CANIDMR0–CANIDMR7 can be written only by the CPU when the MSCAN is in initialization mode. 0 Running — The MSCAN operates normally 1 Initialization mode active — The MSCAN has entered initialization mode

18.3.2.3 MSCAN Bus Timing Register 0 (CANBTR0)

The CANBTR0 register configures various CAN bus timing parameters of the MSCAN module.

Module Base + 0x0002 Access: User read/write[1]

	7	6	5	4	3	2	1	0
R W	SJW1	SJW0	BRP5	BRP4	BRP3	BRP2	BRP1	BRP0
Reset:	0	0	0	0	0	0	0	0

Figure 18-6. MSCAN Bus Timing Register 0 (CANBTR0)

[1] Read: Anytime
Write: Anytime in initialization mode (INITRQ = 1 and INITAK = 1)

Table 18-5. CANBTR0 Register Field Descriptions

Field	Description
7-6 SJW[1:0]	**Synchronization Jump Width** — The synchronization jump width defines the maximum number of time quanta (Tq) clock cycles a bit can be shortened or lengthened to achieve resynchronization to data transitions on the CAN bus (see Table 18-6).
5-0 BRP[5:0]	**Baud Rate Prescaler** — These bits determine the time quanta (Tq) clock which is used to build up the bit timing (see Table 18-7).

Table 18-6. Synchronization Jump Width

SJW1	SJW0	Synchronization Jump Width
0	0	1 Tq clock cycle
0	1	2 Tq clock cycles
1	0	3 Tq clock cycles
1	1	4 Tq clock cycles

Table 18-38. CPU vs. MSCAN Operating Modes

CPU Mode	MSCAN Mode			
	Normal	Reduced Power Consumption		
		Sleep	Power Down	Disabled (CANE=0)
RUN	CSWAI = X[1] SLPRQ = 0 SLPAK = 0	CSWAI = X SLPRQ = 1 SLPAK = 1		CSWAI = X SLPRQ = X SLPAK = X
WAIT	CSWAI = 0 SLPRQ = 0 SLPAK = 0	CSWAI = 0 SLPRQ = 1 SLPAK = 1	CSWAI = 1 SLPRQ = X SLPAK = X	CSWAI = X SLPRQ = X SLPAK = X
STOP			CSWAI = X SLPRQ = X SLPAK = X	CSWAI = X SLPRQ = X SLPAK = X

1 'X' means don't care.

18.4.5.1 Operation in Run Mode

As shown in Table 18-38, only MSCAN sleep mode is available as low power option when the CPU is in run mode.

18.4.5.2 Operation in Wait Mode

The WAI instruction puts the MCU in a low power consumption stand-by mode. If the CSWAI bit is set, additional power can be saved in power down mode because the CPU clocks are stopped. After leaving this power down mode, the MSCAN restarts and enters normal mode again.

While the CPU is in wait mode, the MSCAN can be operated in normal mode and generate interrupts (registers can be accessed via background debug mode).

18.4.5.3 Operation in Stop Mode

The STOP instruction puts the MCU in a low power consumption stand-by mode. In stop mode, the MSCAN is set in power down mode regardless of the value of the SLPRQ/SLPAK and CSWAI bits (Table 18-38).

18.4.5.4 MSCAN Normal Mode

This is a non-power-saving mode. Enabling the MSCAN puts the module from disabled mode into normal mode. In this mode the module can either be in initialization mode or out of initialization mode. See Section 18.4.4.5, "MSCAN Initialization Mode".

Chapter 19
Pulse-Width Modulator (S12PWM8B8CV2)

19.1 Introduction

The Version 2 of S12 PWM module is a channel scalable and optimized implementation of S12 PWM8B8C Version 1. The channel is scalable in pairs from PWM0 to PWM7 and the available channel number is 2, 4, 6 and 8. The shutdown feature has been removed and the flexibility to select one of four clock sources per channel has improved. If the corresponding channels exist and shutdown feature is not used, the Version 2 is fully software compatible to Version 1.

19.1.1 Features

The scalable PWM block includes these distinctive features:

- Up to eight independent PWM channels, scalable in pairs (PWM0 to PWM7)
- Available channel number could be 2, 4, 6, 8 (refer to device specification for exact number)
- Programmable period and duty cycle for each channel
- Dedicated counter for each PWM channel
- Programmable PWM enable/disable for each channel
- Software selection of PWM duty pulse polarity for each channel
- Period and duty cycle are double buffered. Change takes effect when the end of the effective period is reached (PWM counter reaches zero) or when the channel is disabled.
- Programmable center or left aligned outputs on individual channels
- Up to eight 8-bit channel or four 16-bit channel PWM resolution
- Four clock sources (A, B, SA, and SB) provide for a wide range of frequencies
- Programmable clock select logic

19.1.2 Modes of Operation

There is a software programmable option for low power consumption in wait mode that disables the input clock to the prescaler.

In freeze mode there is a software programmable option to disable the input clock to the prescaler. This is useful for emulation.

Wait: The prescaler keeps on running, unless PSWAI in PWMCTL is set to 1.

Freeze: The prescaler keeps on running, unless PFRZ in PWMCTL is set to 1.

20.4.5.5 LIN Transmit Collision Detection

This module allows to check for collisions on the LIN bus.

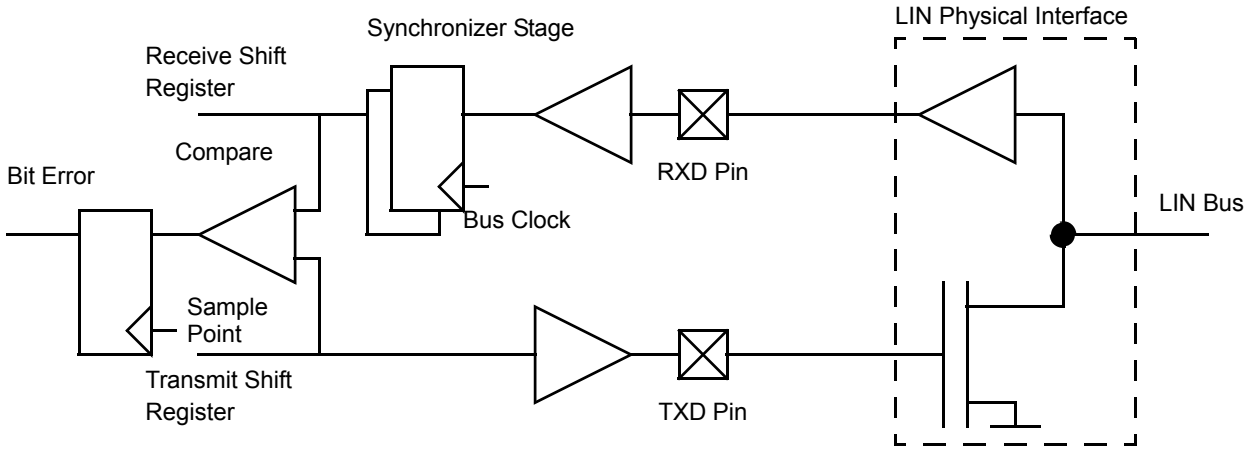

Figure 20-18. Collision Detect Principle

If the bit error circuit is enabled (BERRM[1:0] = 0:1 or = 1:0]), the error detect circuit will compare the transmitted and the received data stream at a point in time and flag any mismatch. The timing checks run when transmitter is active (not idle). As soon as a mismatch between the transmitted data and the received data is detected the following happens:

- The next bit transmitted will have a high level (TXPOL = 0) or low level (TXPOL = 1)
- The transmission is aborted and the byte in transmit buffer is discarded.
- the transmit data register empty and the transmission complete flag will be set
- The bit error interrupt flag, BERRIF, will be set.
- No further transmissions will take place until the BERRIF is cleared.

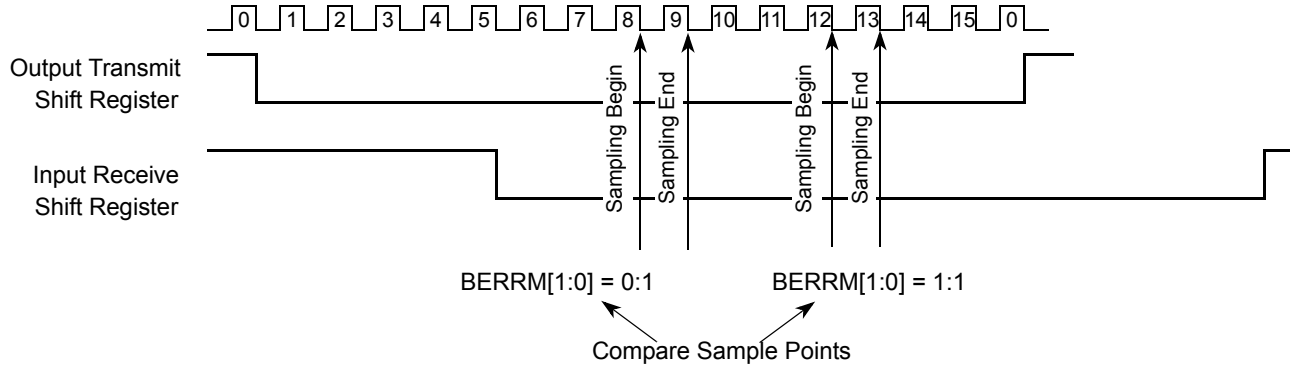

Figure 20-19. Timing Diagram Bit Error Detection

If the bit error detect feature is disabled, the bit error interrupt flag is cleared.

NOTE

The RXPOL and TXPOL bit should be set the same when transmission collision detect feature is enabled, otherwise the bit error interrupt flag may be set incorrectly.

Table 25-59. Set Field Margin Level Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 001 at command launch
		Set if command not available in current mode (see Table 25-27)
		Set if an invalid FlashBlockSelectionCode[1:0] is supplied (See Table 25-34)
		Set if an invalid margin level setting is supplied
	FPVIOL	None
	MGSTAT1	None
	MGSTAT0	None

CAUTION

Field margin levels must only be used during verify of the initial factory programming.

NOTE

Field margin levels can be used to check that Flash memory contents have adequate margin for data retention at the normal level setting. If unexpected results are encountered when checking Flash memory contents at field margin levels, the Flash memory contents should be erased and reprogrammed.

25.4.6.14 Erase Verify EEPROM Section Command

The Erase Verify EEPROM Section command will verify that a section of code in the EEPROM is erased. The Erase Verify EEPROM Section command defines the starting point of the data to be verified and the number of words.

Table 25-60. Erase Verify EEPROM Section Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x10	Global address [17:16] to identify the EEPROM block
001	Global address [15:0] of the first word to be verified	
010	Number of words to be verified	

Upon clearing CCIF to launch the Erase Verify EEPROM Section command, the Memory Controller will verify the selected section of EEPROM memory is erased. The CCIF flag will set after the Erase Verify EEPROM Section operation has completed. If the section is not erased, it means blank check failed, both MGSTAT bits will be set.

31.4.4.3 Valid Flash Module Commands

Table 31-27 present the valid Flash commands, as enabled by the combination of the functional MCU mode (Normal SingleChip NS, Special Singlechip SS) with the MCU security state (Unsecured, Secured).

Special Singlechip mode is selected by input mmc_ss_mode_ts2 asserted. MCU Secured state is selected by input mmc_secure input asserted.

Table 31-27. Flash Commands by Mode and Security State

FCMD	Command	Unsecured		Secured	
		NS[1]	SS[2]	NS[3]	SS[4]
0x01	Erase Verify All Blocks	*	*	*	*
0x02	Erase Verify Block	*	*	*	*
0x03	Erase Verify P-Flash Section	*	*	*	
0x04	Read Once	*	*	*	
0x06	Program P-Flash	*	*	*	
0x07	Program Once	*	*	*	
0x08	Erase All Blocks		*		*
0x09	Erase Flash Block	*	*	*	
0x0A	Erase P-Flash Sector	*	*	*	
0x0B	Unsecure Flash		*		*
0x0C	Verify Backdoor Access Key	*		*	
0x0D	Set User Margin Level	*	*	*	
0x0E	Set Field Margin Level		*		
0x10	Erase Verify EEPROM Section	*	*	*	
0x11	Program EEPROM	*	*	*	
0x12	Erase EEPROM Sector	*	*	*	

1 Unsecured Normal Single Chip mode
2 Unsecured Special Single Chip mode.
3 Secured Normal Single Chip mode.
4 Secured Special Single Chip mode.

31.4.4.4 P-Flash Commands

Table 31-28 summarizes the valid P-Flash commands along with the effects of the commands on the P-Flash block and other resources within the Flash module.

Table 31-28. P-Flash Commands

FCMD	Command	Function on P-Flash Memory
0x01	Erase Verify All Blocks	Verify that all P-Flash (and EEPROM) blocks are erased.

Table A-29. ADC Conversion Performance 5V range, RVA enabled

Supply voltage V_{DDA} =5.0 V, -40°C < T_J < 150°C. V_{RH} = 5.0V. f_{ADCCLK} = 0.25 .. 2MHz [1] The values are tested to be valid with no port AD/C output drivers switching simultaneous with conversions.								
Num	**C**	**Rating**		**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	P	Resolution	12-Bit	LSB		0.61		mV
2	P	Differential Nonlinearity	12-Bit	DNL		±3	±4	counts
3	P	Integral Nonlinearity	12-Bit	INL		±3.5	±5	counts
4	C	Absolute Error[2]	12-Bit	AE			±8	counts
5	P	internal VRH reference voltage	LQFP48, LQFP64, LQFP100	Vvrh_int	4.495		4.505	V
			KGD	Vvrh_int	4.490		4.510	V
6	P	internal VRL reference voltage	LQFP48, LQFP64, LQFP100	Vvrh_int	1.995		2.005V	V
			KGD	Vvrl_int	1.990		2.010V	V
7	C	VRH_INT drift vs temperature[3]		Vvrh_drift	-2		2	mV
8	C	VRL_INT drift vs temperature		Vvrl_drift	-2.5		2.5	mV
9	C	rva turn on settling time		$t_{settling\_on}$			2.5	µs
10	C	rva turn off settling time		$t_{settling\_off}$			1	µs

1 Upper limit of f_{ADCCLK} is restricted when RVA attenuation mode is engaged.

2 These values include the quantization error which is inherently 1/2 count for any A/D converter and the error of the internally generated reference values..

3 Please note: although different in value, drift of vrh_int and vrl_int will go in the same direction.