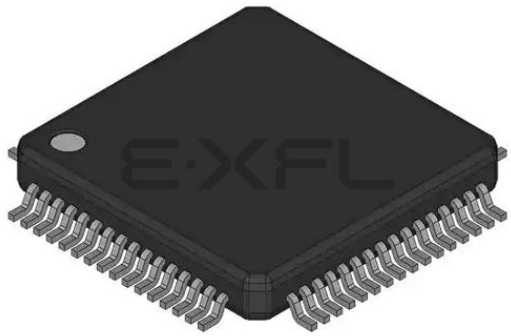

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Details	
Product Status	Active
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Connectivity	CANbus, IrDA, LINbus, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	54
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	3K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3.13V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
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Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=s9s12g96f0mlh

Table 1-15. 32-Pin LQFP Pinout for S12G48 and S12G64

	Function <----lowest-----PRIORITY-----highest---->					Power Supply	Internal Pull Resistor	
Package Pin	Pin	2nd Func.	3rd Func.	4th Func	5th Func		CTRL	Reset State
30	PS7	API_EXTCLK	ECLK	PWM5	$\overline{SS0}$	V_{DDX}	PERS/PPSS	Up
31	PM0	RXD1	RXCAN	—	—	V_{DDX}	PERM/PPSM	Disabled
32	PM1	TXD1	TXCAN	—	—	V_{DDX}	PERM/PPSM	Disabled

[1] The regular I/O characteristics (see Section A.2, “I/O Characteristics”) apply if the EXTAL/XTAL function is disabled

Table 1-19. 64-Pin LQFP Pinout for S12GA48 and S12GA64

	Function <----lowest-----PRIORITY-----highest---->					Power Supply	Internal Pull Resistor	
Package Pin	Pin	2nd Func.	3rd Func.	4th Func	5th Func		CTRL	Reset State
57	PS5	MOSI0	—	—	—	V_{DDX}	PERS/PPSS	Up
58	PS6	SCK0	—	—	—	V_{DDX}	PERS/PPSS	Up
59	PS7	API_EXTCLK	ECLK	$\overline{SS0}$	—	V_{DDX}	PERS/PPSS	Up
60	PM0	RXCAN	—	—	—	V_{DDX}	PERM/PPSM	Disabled
61	PM1	TXCAN	—	—	—	V_{DDX}	PERM/PPSM	Disabled
62	PM2	—	—	—	—	V_{DDX}	PERM/PPSM	Disabled
63	PM3	—	—	—	—	V_{DDX}	PERM/PPSM	Disabled
64	PJ7	KWJ7	—	—	—	V_{DDX}	PERJ/PPSJ	Up

[1] The regular I/O characteristics (see Section A.2, “I/O Characteristics”) apply if the EXTAL/XTAL function is disabled

Table 1-21. 64-Pin LQFP Pinout for S12G96 and S12G128

	Function <----lowest-----PRIORITY-----highest---->					Power Supply	Internal Pull Resistor	
Package Pin	Pin	2nd Func.	3rd Func.	4th Func	5th Func		CTRL	Reset State
1	PJ6	KWJ6	SCK2	—	—	V_{DDX}	PERJ/PPSJ	Up
2	PJ5	KWJ5	MOSI2	—	—	V_{DDX}	PERJ/PPSJ	Up
3	PJ4	KWJ4	MISO2	—	—	V_{DDX}	PERJ/PPSJ	Up
4	RESET	—	—	—	—	V_{DDX}	PULLUP	
5	VDDX	—	—	—	—	—	—	—
6	VDDR	—	—	—	—	—	—	—
7	VSSX	—	—	—	—	—	—	—
8	PE0[1]	EXTAL	—	—	—	V_{DDX}	PUCR/PDPEE	Down
9	VSS	—	—	—	—	—	—	—
10	PE1[1]	XTAL	—	—	—	V_{DDX}	PUCR/PDPEE	Down
11	TEST	—	—	—	—	N.A.	$\overline{\text{RESET}}$ pin	Down
12	PJ0	KWJ0	MISO1	—	—	V_{DDX}	PERJ/PPSJ	Up
13	PJ1	KWJ1	MOSI1	—	—	V_{DDX}	PERJ/PPSJ	Up
14	PJ2	KWJ2	SCK1	—	—	V_{DDX}	PERJ/PPSJ	Up
15	PJ3	KWJ3	$\overline{\text{SS1}}$	—	—	V_{DDX}	PERJ/PPSJ	Up
16	BKGD	MODC	—	—	—	V_{DDX}	PUCR/BKPUE	Up
17	PP0	KWP0	ETRIG0	API_EXTCLK	PWM0	V_{DDX}	PERP/PPSP	Disabled
18	PP1	KWP1	ETRIG1	ECLKX2	PWM1	V_{DDX}	PERP/PPSP	Disabled
19	PP2	KWP2	ETRIG2	PWM2	—	V_{DDX}	PERP/PPSP	Disabled
20	PP3	KWP3	ETRIG3	PWM3	—	V_{DDX}	PERP/PPSP	Disabled
21	PP4	KWP4	PWM4	—	—	V_{DDX}	PERP/PPSP	Disabled
22	PP5	KWP5	PWM5	—	—	V_{DDX}	PERP/PPSP	Disabled
23	PP6	KWP6	PWM6	—	—	V_{DDX}	PERP/PPSP	Disabled
24	PP7	KWP7	PWM7	—	—	V_{DDX}	PERP/PPSP	Disabled
25	PT7	IOC7	—	—	—	V_{DDX}	PERT/PPST	Disabled
26	PT6	IOC6	—	—	—	V_{DDX}	PERT/PPST	Disabled
27	PT5	IOC5	—	—	—	V_{DDX}	PERT/PPST	Disabled

Table 5-5. DIRECT Field Descriptions

Field	Description
7–0 DP[15:8]	**Direct Page Index Bits 15–8** — These bits are used by the CPU when performing accesses using the direct addressing mode. These register bits form bits [15:8] of the local address (see Figure 5-6).

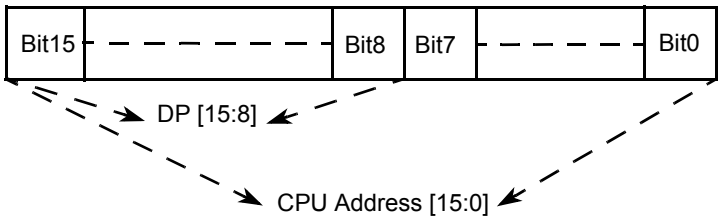


Figure 5-6. DIRECT Address Mapping

Example 5-1. This example demonstrates usage of the Direct Addressing Mode

```
MOVB     #$04,DIRECT       ;Set DIRECT register to 0x04. From this point on, all memory
                           ;accesses using direct addressing mode will be in the local
                           ;address range from 0x0400 to 0x04FF.
LDY      <$12              ;Load the Y index register from 0x0412 (direct access).
```

5.3.2.3 MMC Control Register (MMCCTL1)

Address: 0x0013

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	NVMRES
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 5-7. MMC Control Register (MMCCTL1)

Read: Anytime.

Write: Anytime.

The NVMRES bit maps 16k of internal NVM resources (see Section FTMRG) to the global address space 0x04000 to 0x07FFF.

Table 5-6. MODE Field Descriptions

Field	Description
0 NVMRES	Map internal NVM resources into the global memory map Write: Anytime This bit maps internal NVM resources into the global address space. 0 Program flash is mapped to the global address range from 0x04000 to 0x07FFF. 1 NVM resources are mapped to the global address range from 0x04000 to 0x07FFF.

NOTE

A write to this register starts the RTI time-out period. A change of the RTIOSCSEL bit (writing a different value or loosing UPOSC status) re-starts the RTI time-out period.

Table 10-9. CPMURTI Field Descriptions

Field	Description
7 RTDEC	**Decimal or Binary Divider Select Bit** — RTDEC selects decimal or binary based prescaler values. 0 Binary based divider value. See Table 10-10 1 Decimal based divider value. See Table 10-11
6–4 RTR[6:4]	**Real Time Interrupt Prescale Rate Select Bits** — These bits select the prescale rate for the RTI. See Table 10-10 and Table 10-11.
3–0 RTR[3:0]	**Real Time Interrupt Modulus Counter Select Bits** — These bits select the modulus counter target value to provide additional granularity.Table 10-10 and Table 10-11 show all possible divide values selectable by the CPMURTI register**.**

Table 10-10. RTI Frequency Divide Rates for RTDEC = 0

RTR[3:0]	RTR[6:4] =							
	000 (OFF)	**001 (2^{10})**	**010 (2^{11})**	**011 (2^{12})**	**100 (2^{13})**	**101 (2^{14})**	**110 (2^{15})**	**111 (2^{16})**
0000 (÷1)	OFF[1]	2^{10}	2^{11}	2^{12}	2^{13}	2^{14}	2^{15}	2^{16}
0001 (÷2)	OFF	$2x2^{10}$	$2x2^{11}$	$2x2^{12}$	$2x2^{13}$	$2x2^{14}$	$2x2^{15}$	$2x2^{16}$
0010 (÷3)	OFF	$3x2^{10}$	$3x2^{11}$	$3x2^{12}$	$3x2^{13}$	$3x2^{14}$	$3x2^{15}$	$3x2^{16}$
0011 (÷4)	OFF	$4x2^{10}$	$4x2^{11}$	$4x2^{12}$	$4x2^{13}$	$4x2^{14}$	$4x2^{15}$	$4x2^{16}$
0100 (÷5)	OFF	$5x2^{10}$	$5x2^{11}$	$5x2^{12}$	$5x2^{13}$	$5x2^{14}$	$5x2^{15}$	$5x2^{16}$
0101 (÷6)	OFF	$6x2^{10}$	$6x2^{11}$	$6x2^{12}$	$6x2^{13}$	$6x2^{14}$	$6x2^{15}$	$6x2^{16}$
0110 (÷7)	OFF	$7x2^{10}$	$7x2^{11}$	$7x2^{12}$	$7x2^{13}$	$7x2^{14}$	$7x2^{15}$	$7x2^{16}$
0111 (÷8)	OFF	$8x2^{10}$	$8x2^{11}$	$8x2^{12}$	$8x2^{13}$	$8x2^{14}$	$8x2^{15}$	$8x2^{16}$
1000 (÷9)	OFF	$9x2^{10}$	$9x2^{11}$	$9x2^{12}$	$9x2^{13}$	$9x2^{14}$	$9x2^{15}$	$9x2^{16}$
1001 (÷10)	OFF	$10x2^{10}$	$10x2^{11}$	$10x2^{12}$	$10x2^{13}$	$10x2^{14}$	$10x2^{15}$	$10x2^{16}$
1010 (÷11)	OFF	$11x2^{10}$	$11x2^{11}$	$11x2^{12}$	$11x2^{13}$	$11x2^{14}$	$11x2^{15}$	$11x2^{16}$
1011 (÷12)	OFF	$12x2^{10}$	$12x2^{11}$	$12x2^{12}$	$12x2^{13}$	$12x2^{14}$	$12x2^{15}$	$12x2^{16}$
1100 (÷13)	OFF	$13x2^{10}$	$13x2^{11}$	$13x2^{12}$	$13x2^{13}$	$13x2^{14}$	$13x2^{15}$	$13x2^{16}$
1101 (÷14)	OFF	$14x2^{10}$	$14x2^{11}$	$14x2^{12}$	$14x2^{13}$	$14x2^{14}$	$14x2^{15}$	$14x2^{16}$

12.2 Signal Description

This section lists all inputs to the ADC12B8C block.

12.2.1 Detailed Signal Descriptions

12.2.1.1 AN*x* (*x* = 7, 6, 5, 4, 3, 2, 1, 0)

This pin serves as the analog input Channel *x*. It can also be configured as digital port or external trigger for the ATD conversion.

12.2.1.2 ETRIG3, ETRIG2, ETRIG1, ETRIG0

These inputs can be configured to serve as an external trigger for the ATD conversion.

Refer to device specification for availability and connectivity of these inputs!

12.2.1.3 VRH, VRL

VRH is the high reference voltage, VRL is the low reference voltage for ATD conversion.

12.2.1.4 VDDA, VSSA

These pins are the power supplies for the analog circuitry of the ADC12B8C block.

12.3 Memory Map and Register Definition

This section provides a detailed description of all registers accessible in the ADC12B8C.

12.3.1 Module Memory Map

Figure 12-2 gives an overview on all ADC12B8C registers.

NOTE

Register Address = Base Address + Address Offset, where the Base Address is defined at the MCU level and the Address Offset is defined at the module level.

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0000	ATDCTL0	R W	Reserved	0	0	0	WRAP3	WRAP2	WRAP1	WRAP0
0x0001	ATDCTL1	R W	ETRIGSEL	SRES1	SRES0	SMP_DIS	ETRIGCH3	ETRIGCH2	ETRIGCH1	ETRIGCH0
0x0002	ATDCTL2	R W	0	AFFC	Reserved	ETRIGLE	ETRIGP	ETRIGE	ASCIE	ACMPIE

= Unimplemented or Reserved

Figure 12-2. ADC12B8C Register Summary (Sheet 1 of 2)

— The 14 most significant bits of the extended identifier plus the SRR and IDE bits of CAN 2.0B messages.

— The 11 bits of the standard identifier, the RTR and IDE bits of CAN 2.0A/B messages. Figure 18-41 shows how the first 32-bit filter bank (CANIDAR0–CANIDAR3, CANIDMR0–CANIDMR3) produces filter 0 and 1 hits. Similarly, the second filter bank (CANIDAR4–CANIDAR7, CANIDMR4–CANIDMR7) produces filter 2 and 3 hits.

- Eight identifier acceptance filters, each to be applied to the first 8 bits of the identifier. This mode implements eight independent filters for the first 8 bits of a CAN 2.0A/B compliant standard identifier or a CAN 2.0B compliant extended identifier.
  Figure 18-42 shows how the first 32-bit filter bank (CANIDAR0–CANIDAR3, CANIDMR0–CANIDMR3) produces filter 0 to 3 hits. Similarly, the second filter bank (CANIDAR4–CANIDAR7, CANIDMR4–CANIDMR7) produces filter 4 to 7 hits.
- Closed filter. No CAN message is copied into the foreground buffer RxFG, and the RXF flag is never set.

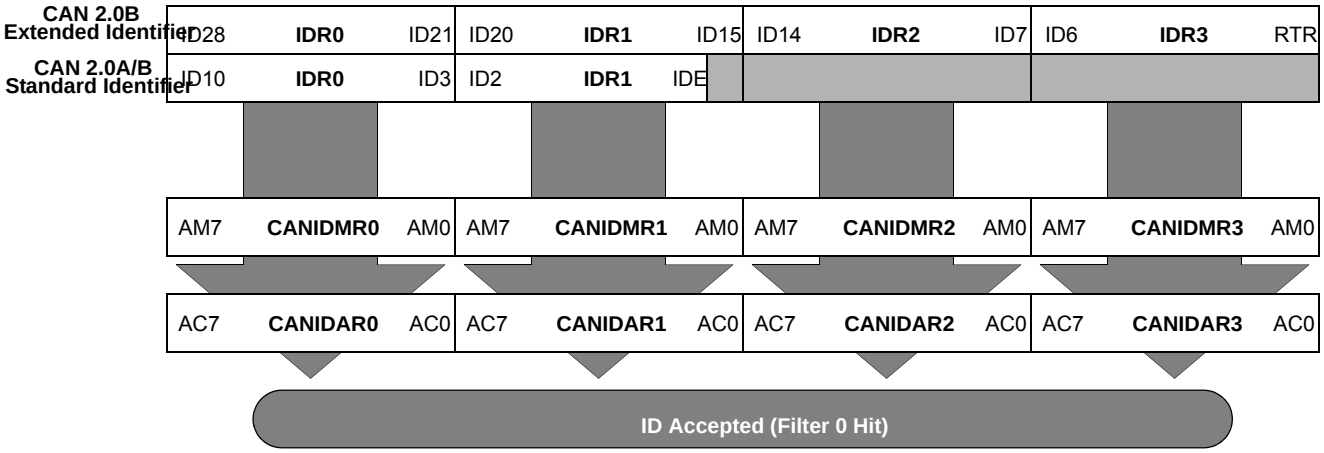


Figure 18-40. 32-bit Maskable Identifier Acceptance Filter

20.5.3.1.8 BKDIF Description

The BKDIF interrupt is set when a break signal was received. Clear BKDIF by writing a “1” to the SCIASR1 SCI alternative status register 1. This flag is also cleared if break detect feature is disabled.

20.5.4 Recovery from Wait Mode

The SCI interrupt request can be used to bring the CPU out of wait mode.

20.5.5 Recovery from Stop Mode

An active edge on the receive input can be used to bring the CPU out of stop mode.

Table 21-6. Example SPI Baud Rate Selection (25 MHz Bus Clock)

SPPR2	SPPR1	SPPR0	SPR2	SPR1	SPR0	Baud Rate Divisor	Baud Rate
0	0	1	0	1	0	16	1.5625 Mbit/s
0	0	1	0	1	1	32	781.25 kbit/s
0	0	1	1	0	0	64	390.63 kbit/s
0	0	1	1	0	1	128	195.31 kbit/s
0	0	1	1	1	0	256	97.66 kbit/s
0	0	1	1	1	1	512	48.83 kbit/s
0	1	0	0	0	0	6	4.16667 Mbit/s
0	1	0	0	0	1	12	2.08333 Mbit/s
0	1	0	0	1	0	24	1.04167 Mbit/s
0	1	0	0	1	1	48	520.83 kbit/s
0	1	0	1	0	0	96	260.42 kbit/s
0	1	0	1	0	1	192	130.21 kbit/s
0	1	0	1	1	0	384	65.10 kbit/s
0	1	0	1	1	1	768	32.55 kbit/s
0	1	1	0	0	0	8	3.125 Mbit/s
0	1	1	0	0	1	16	1.5625 Mbit/s
0	1	1	0	1	0	32	781.25 kbit/s
0	1	1	0	1	1	64	390.63 kbit/s
0	1	1	1	0	0	128	195.31 kbit/s
0	1	1	1	0	1	256	97.66 kbit/s
0	1	1	1	1	0	512	48.83 kbit/s
0	1	1	1	1	1	1024	24.41 kbit/s
1	0	0	0	0	0	10	2.5 Mbit/s
1	0	0	0	0	1	20	1.25 Mbit/s
1	0	0	0	1	0	40	625 kbit/s
1	0	0	0	1	1	80	312.5 kbit/s
1	0	0	1	0	0	160	156.25 kbit/s
1	0	0	1	0	1	320	78.13 kbit/s
1	0	0	1	1	0	640	39.06 kbit/s
1	0	0	1	1	1	1280	19.53 kbit/s
1	0	1	0	0	0	12	2.08333 Mbit/s
1	0	1	0	0	1	24	1.04167 Mbit/s
1	0	1	0	1	0	48	520.83 kbit/s
1	0	1	0	1	1	96	260.42 kbit/s
1	0	1	1	0	0	192	130.21 kbit/s
1	0	1	1	0	1	384	65.10 kbit/s
1	0	1	1	1	0	768	32.55 kbit/s
1	0	1	1	1	1	1536	16.28 kbit/s
1	1	0	0	0	0	14	1.78571 Mbit/s

[1] The register is available only if corresponding channel exists.

22.3.2.1 Timer Input Capture/Output Compare Select (TIOS)

Module Base + 0x0000

	7	6	5	4	3	2	1	0
R W	RESERVED	RESERVED	IOS5	IOS4	IOS3	IOS2	IOS1	IOS0
Reset	0	0	0	0	0	0	0	0

Figure 22-4. Timer Input Capture/Output Compare Select (TIOS)

Read: Anytime

Write: Anytime

Table 22-2. TIOS Field Descriptions

Note: Writing to unavailable bits has no effect. Reading from unavailable bits return a zero.

Field	Description
5:0 IOS[5:0]	Input Capture or Output Compare Channel Configuration 0 The corresponding implemented channel acts as an input capture. 1 The corresponding implemented channel acts as an output compare.

22.3.2.2 Timer Compare Force Register (CFORC)

Module Base + 0x0001

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W	RESERVED	RESERVED	FOC5	FOC4	FOC3	FOC2	FOC1	FOC0
Reset	0	0	0	0	0	0	0	0

Figure 22-5. Timer Compare Force Register (CFORC)

Read: Anytime but will always return 0x0000 (1 state is transient)

Write: Anytime

Table 22-3. CFORC Field Descriptions

Note: Writing to unavailable bits has no effect. Reading from unavailable bits return a zero.

Field	Description
5:0 FOC[5:0]	**Note: Force Output Compare Action for Channel 5:0** — A write to this register with the corresponding data bit(s) set causes the action which is programmed for output compare “x” to occur immediately. The action taken is the same as if a successful comparison had just taken place with the TCx register except the interrupt flag does not get set. If forced output compare on any channel occurs at the same time as the successful output compare then forced output compare action will take precedence and interrupt flag won’t get set.

CAUTION

The FCLKDIV register should never be written while a Flash command is executing (CCIF=0).

Table 25-7. FCLKDIV Field Descriptions

Field	Description
7 FDIVLD	Clock Divider Loaded 0 FCLKDIV register has not been written since the last reset 1 FCLKDIV register has been written since the last reset
6 FDIVLCK	Clock Divider Locked 0 FDIV field is open for writing 1 FDIV value is locked and cannot be changed. Once the lock bit is set high, only reset can clear this bit and restore writability to the FDIV field in normal mode.
5–0 FDIV[5:0]	**Clock Divider Bits** — FDIV[5:0] must be set to effectively divide BUSCLK down to 1 MHz to control timed events during Flash program and erase algorithms. Table 25-8 shows recommended values for FDIV[5:0] based on the BUSCLK frequency. Please refer to Section 25.4.4, “Flash Command Operations,” for more information.

Table 25-8. FDIV values for various BUSCLK Frequencies

BUSCLK Frequency (MHz)		FDIV[5:0]	BUSCLK Frequency (MHz)		FDIV[5:0]
MIN[1]	MAX[2]		MIN[1]	MAX[2]	
1.0	1.6	0x00	16.6	17.6	0x10
1.6	2.6	0x01	17.6	18.6	0x11
2.6	3.6	0x02	18.6	19.6	0x12
3.6	4.6	0x03	19.6	20.6	0x13
4.6	5.6	0x04	20.6	21.6	0x14
5.6	6.6	0x05	21.6	22.6	0x15
6.6	7.6	0x06	22.6	23.6	0x16
7.6	8.6	0x07	23.6	24.6	0x17
8.6	9.6	0x08	24.6	25.6	0x18
9.6	10.6	0x09			
10.6	11.6	0x0A			
11.6	12.6	0x0B			
12.6	13.6	0x0C			
13.6	14.6	0x0D			
14.6	15.6	0x0E			
15.6	16.6	0x0F			

1 BUSCLK is Greater Than this value.

2 BUSCLK is Less Than or Equal to this value.

Chapter 27
64 KByte Flash Module (S12FTMRG64K1V1)

Table 27-1. Revision History

Revision Number	Revision Date	Sections Affected	Description of Changes
V01.04	17 Jun 2010	27.4.6.1/27-950 27.4.6.2/27-951 27.4.6.3/27-951 27.4.6.14/27-961	Clarify Erase Verify Commands Descriptions related to the bits MGSTAT[1:0] of the register FSTAT.
V01.05	20 aug 2010	27.4.6.2/27-951 27.4.6.12/27-958 27.4.6.13/27-960	Updated description of the commands RD1BLK, MLOADU and MLOADF
Rev.1.27	31 Jan 2011	27.3.2.9/27-933	Updated description of protection on Section 27.3.2.9

27.1 Introduction

The FTMRG64K1 module implements the following:

- 64Kbytes of P-Flash (Program Flash) memory
- 2 Kbytes of EEPROM memory

The Flash memory is ideal for single-supply applications allowing for field reprogramming without requiring external high voltage sources for program or erase operations. The Flash module includes a memory controller that executes commands to modify Flash memory contents. The user interface to the memory controller consists of the indexed Flash Common Command Object (FCCOB) register which is written to with the command, global address, data, and any required command parameters. The memory controller must complete the execution of a command before the FCCOB register can be written to with a new command.

CAUTION

A Flash word or phrase must be in the erased state before being programmed. Cumulative programming of bits within a Flash word or phrase is not allowed.

The Flash memory may be read as bytes and aligned words. Read access time is one bus cycle for bytes and aligned words. For misaligned words access, the CPU has to perform twice the byte read access command. For Flash memory, an erased bit reads 1 and a programmed bit reads 0.

Table 27-61. Erase Verify EEPROM Section Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 010 at command launch
		Set if command not available in current mode (see Table 27-27)
		Set if an invalid global address [17:0] is supplied
		Set if a misaligned word address is supplied (global address [0] != 0)
		Set if the requested section breaches the end of the EEPROM block
	FPVIOL	None
	MGSTAT1	Set if any errors have been encountered during the read or if blank check failed.
	MGSTAT0	Set if any non-correctable errors have been encountered during the read or if blank check failed.

27.4.6.15 Program EEPROM Command

The Program EEPROM operation programs one to four previously erased words in the EEPROM block. The Program EEPROM operation will confirm that the targeted location(s) were successfully programmed upon completion.

CAUTION

A Flash word must be in the erased state before being programmed. Cumulative programming of bits within a Flash word is not allowed.

Table 27-62. Program EEPROM Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x11	Global address [17:16] to identify the EEPROM block
001	Global address [15:0] of word to be programmed	
010	Word 0 program value	
011	Word 1 program value, if desired	
100	Word 2 program value, if desired	
101	Word 3 program value, if desired	

Upon clearing CCIF to launch the Program EEPROM command, the user-supplied words will be transferred to the Memory Controller and be programmed if the area is unprotected. The CCOBIX index value at Program EEPROM command launch determines how many words will be programmed in the EEPROM block. The CCIF flag is set when the operation has completed.

28.4.6.3 Erase Verify P-Flash Section Command

The Erase Verify P-Flash Section command will verify that a section of code in the P-Flash memory is erased. The Erase Verify P-Flash Section command defines the starting point of the code to be verified and the number of phrases.

Table 28-36. Erase Verify P-Flash Section Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x03	Global address [17:16] of a P-Flash block
001	Global address [15:0] of the first phrase to be verified	
010	Number of phrases to be verified	

Upon clearing CCIF to launch the Erase Verify P-Flash Section command, the Memory Controller will verify the selected section of Flash memory is erased. The CCIF flag will set after the Erase Verify P-Flash Section operation has completed. If the section is not erased, it means blank check failed, both MGSTAT bits will be set.

Table 28-37. Erase Verify P-Flash Section Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 010 at command launch
		Set if command not available in current mode (see Table 28-27)
		Set if an invalid global address [17:0] is supplied see Table 28-3)[1]
		Set if a misaligned phrase address is supplied (global address [2:0] != 000)
		Set if the requested section crosses a the P-Flash address boundary
	FPVIOL	None
	MGSTAT1	Set if any errors have been encountered during the read[2] or if blank check failed.
	MGSTAT0	Set if any non-correctable errors have been encountered during the read[2] or if blank check failed.

1 As defined by the memory map for FTMRG96K1.

2 As found in the memory map for FTMRG96K1.

28.4.6.4 Read Once Command

The Read Once command provides read access to a reserved 64 byte field (8 phrases) located in the nonvolatile information register of P-Flash. The Read Once field is programmed using the Program Once command described in Section 28.4.6.6. The Read Once command must not be executed from the Flash block containing the Program Once reserved field to avoid code runaway.

Table 28-38. Read Once Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x04	Not Required

Table 28-49. Erase P-Flash Sector Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 001 at command launch
		Set if command not available in current mode (see Table 28-27)
		Set if an invalid global address [17:16] is supplied see Table 28-3)[1]
		Set if a misaligned phrase address is supplied (global address [2:0] != 000)
	FPVIOL	Set if the selected P-Flash sector is protected
	MGSTAT1	Set if any errors have been encountered during the verify operation
	MGSTAT0	Set if any non-correctable errors have been encountered during the verify operation

1 As defined by the memory map for FTMRG96K1.

28.4.6.10 Unsecure Flash Command

The Unsecure Flash command will erase the entire P-Flash and EEPROM memory space and, if the erase is successful, will release security.

Table 28-50. Unsecure Flash Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x0B	Not required

Upon clearing CCIF to launch the Unsecure Flash command, the Memory Controller will erase the entire P-Flash and EEPROM memory space and verify that it is erased. If the Memory Controller verifies that the entire Flash memory space was properly erased, security will be released. If the erase verify is not successful, the Unsecure Flash operation sets MGSTAT1 and terminates without changing the security state. During the execution of this command (CCIF=0) the user must not write to any Flash module register. The CCIF flag is set after the Unsecure Flash operation has completed.

Table 28-51. Unsecure Flash Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 000 at command launch
		Set if command not available in current mode (see Table 28-27)
	FPVIOL	Set if any area of the P-Flash or EEPROM memory is protected
	MGSTAT1	Set if any errors have been encountered during the verify operation[1]
	MGSTAT0	Set if any non-correctable errors have been encountered during the verify operation[1]

1 As found in the memory map for FTMRG96K1.

Table A-36. NVM Timing Characteristics)

, S12GN48, S12G48, S12G64, S12GA64									
Num	**Command**	**f_{NVMOP} cycle**	**f_{NVMBUS} cycle**	**Symbol**	**Min[1]**	**Typ[2]**	**Max[3]**	**Lfmax[4]**	**Unit**
1	Erase Verify All Blocks[5,6]	0	17937	t_{RD1ALL}	0.72	0.72	1.43	35.87	ms
2	Erase Verify Block (Pflash)[5]	0	16924	t_{RD1BLK_P}	0.68	0.68	1.35	33.85	ms
3	Erase Verify Block (EEPROM)[6]	0	1512	t_{RD1BLK_D}	0.06	0.06	0.12	3.02	ms
4	Erase Verify P-Flash Section	0	476	t_{RD1SEC}	19.04	19.04	38.08	952	ms
5	Read Once	0	445	t_{RDONCE}	17.8	17.8	17.8	445	µs
6	Program P-Flash (4 Word)	164	2925	t_{PGM_4}	0.27	0.28	0.63	11.91	ms
7	Program Once	164	2888	$t_{PGMONCE}$	0.27	0.28	0.28	3.09	ms
8	Erase All Blocks[5,6]	100066	18273	t_{ERSALL}	96.03	100.8	101.53	161.63	ms
9	Erase Flash Block (Pflash)[5]	100060	17157	t_{ERSBLK_P}	95.98	100.75	101.43	159.39	ms
10	Erase Flash Block (EEPROM)[6]	100060	1808	t_{ERSBLK_D}	95.37	100.13	100.2	128.69	ms
11	Erase P-Flash Sector	20015	865	t_{ERSPG}	19.1	20.05	20.08	26.75	ms
12	Unsecure Flash	100066	18351	t_{UNSECU}	96.03	100.8	101.53	161.78	ms
13	Verify Backdoor Access Key	0	481	t_{VFYKEY}	19.24	19.24	19.24	481	µs
14	Set User Margin Level	0	399	t_{MLOADU}	15.96	15.96	15.96	399	µs
15	Set Factory Margin Level	0	408	t_{MLOADF}	16.32	16.32	16.32	408	µs
16	Erase Verify EEPROM Section	0	546	$t_{DRD1SEC}$	0.02	0.02	0.04	1.09	ms
17	Program EEPROM (1 Word)	68	1565	t_{DPGM_1}	0.13	0.13	0.32	6.35	ms
18	Program EEPROM (2 Word)	136	2512	t_{DPGM_2}	0.23	0.24	0.54	10.22	ms
19	Program EEPROM (3 Word)	204	3459	t_{DPGM_3}	0.33	0.34	0.76	14.09	ms
20	Program EEPROM (4 Word)	272	4406	t_{DPGM_4}	0.44	0.45	0.98	17.96	ms
21	Erase EEPROM Sector	5015	753	t_{DERSPG}	4.81	5.05	20.57	37.88	ms

1 Minimum times are based on maximum f_{NVMOP} and maximum f_{NVMBUS}

2 Typical times are based on typical f_{NVMOP} and typical f_{NVMBUS}

3 Maximum times are based on typical f_{NVMOP} and typical f_{NVMBUS} plus aging

4 Lowest-frequency max times are based on minimum f_{NVMOP} and minimum f_{NVMBUS} plus aging

5 Affected by Pflash size

6 Affected by EEPROM size

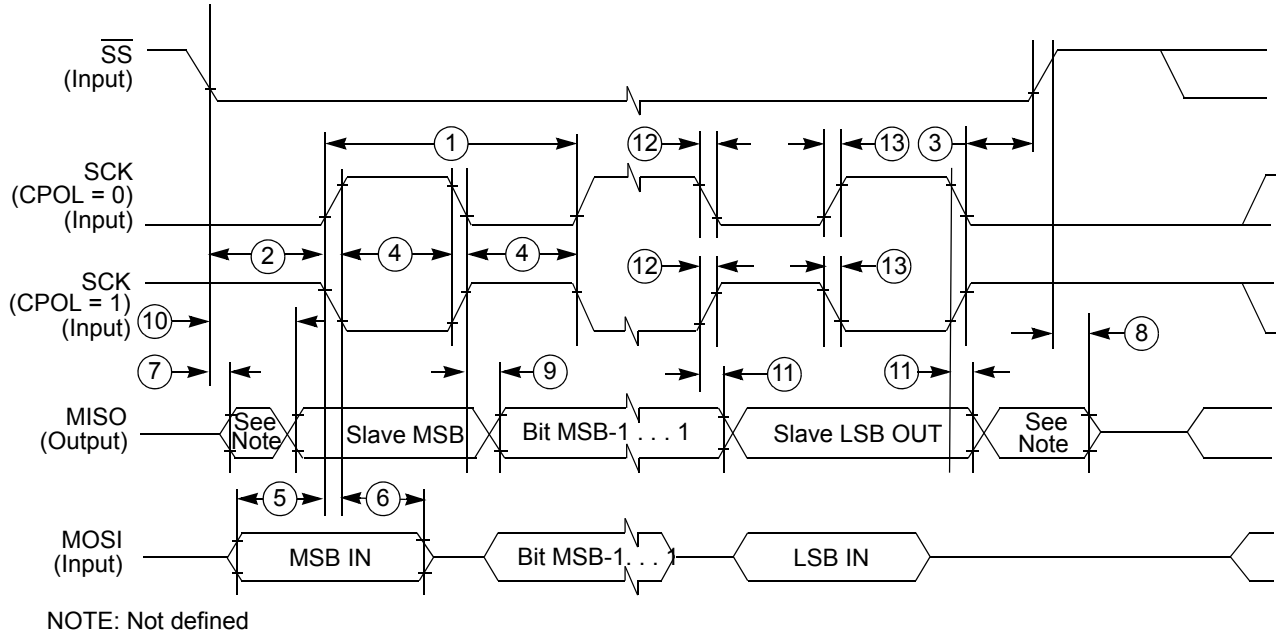
In Table A-51 the timing characteristics for master mode are listed.

Table A-51. SPI Master Mode Timing Characteristics

Conditions are 4.5 V < V_{DD35} < 5.5 V junction temperature from –40°C to T_{Jmax}.							
Num	**C**	**Characteristic**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	D	SCK Frequency	f_{sck}	1/2048	—	1/2	f_{bus}
1	D	SCK Period	t_{sck}	2	—	2048	t_{bus}
2	D	Enable Lead Time	t_L	—	1/2	—	t_{sck}
3	D	Enable Trail Time	t_T	—	1/2	—	t_{sck}
4	D	Clock (SCK) High or Low Time	t_{wsck}	—	1/2	—	t_{sck}
5	D	Data Setup Time (Inputs)	t_{su}	8	—	—	ns
6	D	Data Hold Time (Inputs)	t_{hi}	8	—	—	ns
9	D	Data Valid after SCK Edge	t_{vsck}	—	—	15	ns
10	D	Data Valid after $\overline{SS}$ fall (CPHA=0)	t_{vss}	—	—	15	ns
11	D	Data Hold Time (Outputs)	t_{ho}	0	—	—	ns
12	D	Rise and Fall Time Inputs	t_{rfi}	—	—	9	ns
13	D	Rise and Fall Time Outputs	t_{rfo}	—	—	9	ns

A.15.2 Slave Mode

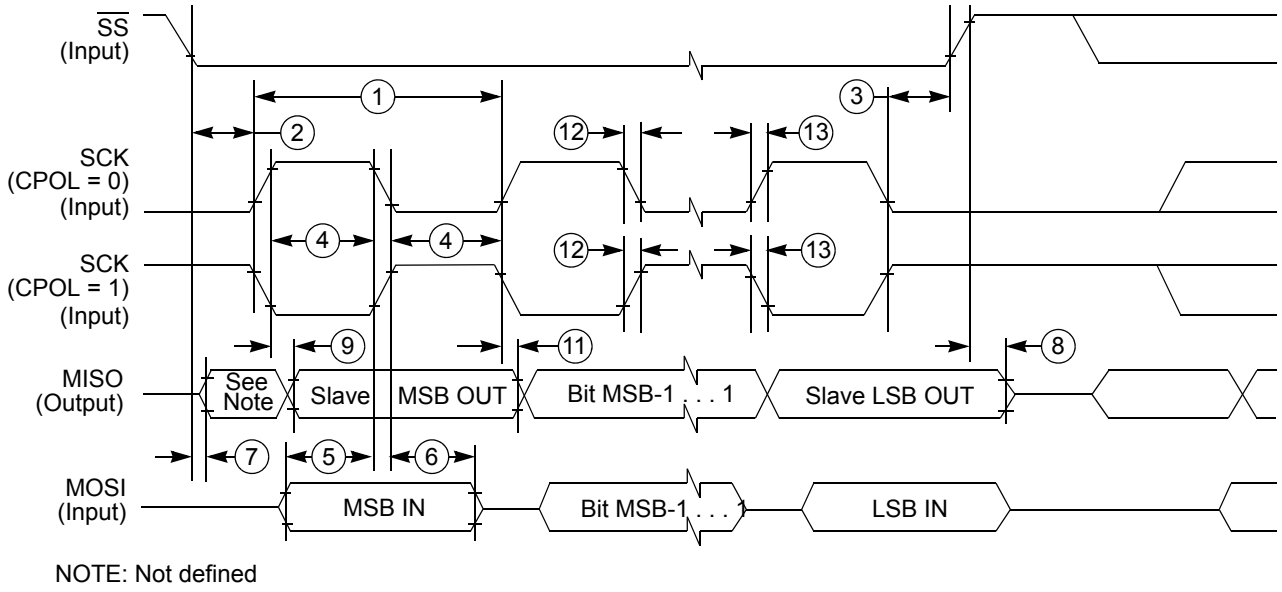
In Figure A-9 the timing diagram for slave mode with transmission format CPHA = 0 is depicted.



NOTE: Not defined

Figure A-9. SPI Slave Timing (CPHA = 0)

In Figure A-10 the timing diagram for slave mode with transmission format CPHA = 1 is depicted.



NOTE: Not defined

Figure A-10. SPI Slave Timing (CPHA = 1)

Appendix D
Package and Die Information

Revision History

Version Number	Revision Date	Description of Changes
Rev 0.01	2-Jan-2009	Initial release
Rev 0.02	25-Jan-2013	• Added D.7, “KGD Information”
Rev 0.03	31-Jan-2013	• Updated , “Bondpad Coordinates”