Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	12V1
Core Size	16-Bit
Speed	25MHz
Connectivity	CANbus, IrDA, LINbus, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	54
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	3K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3.13V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s9s12g96f0vlh

This document contains information for all constituent modules, with the exception of the CPU. For CPU information please refer to **CPU12-1** in the **CPU12 & CPU12X Reference Manual**

1.3.15 Reference Voltage Attenuator (RVA)

- Attenuation of ADC reference voltage with low long-term drift

1.3.16 Digital-to-Analog Converter Module (DAC)

- 1 digital-analog converter channel (per module) with:
  - 8 bit resolution
  - full and reduced output voltage range
  - buffered or unbuffered analog output voltage usable
- operational amplifier stand alone usable

1.3.17 Analog Comparator (ACMP)

- Low offset, low long-term offset drift
- Selectable interrupt on rising, falling, or rising and falling edges of comparator output
- Option to output comparator signal on an external pin
- Option to trigger timer input capture events

1.3.18 On-Chip Voltage Regulator (VREG)

- Linear voltage regulator with bandgap reference
- Low-voltage detect (LVD) with low-voltage interrupt (LVI)
- Power-on reset (POR) circuit
- Low-voltage reset (LVR)

1.3.19 Background Debug (BDM)

- Non-intrusive memory access commands
- Supports in-circuit programming of on-chip nonvolatile memory

1.3.20 Debugger (DBG)

- Trace buffer with depth of 64 entries
- Three comparators (A, B and C)
  - Access address comparisons with optional data comparisons
  - Program counter comparisons
  - Exact address or address range comparisons
- Two types of comparator matches
  - Tagged This matches just before a specific instruction begins execution
  - Force This is valid on the first instruction boundary after a match occurs
- Four trace modes

Table 1-22. 100-Pin LQFP Pinout for S12G96 and S12G128

	Function <----lowest-----PRIORITY-----highest---->				Power Supply	Internal Pull Resistor	
Package Pin	Pin	2nd Func.	3rd Func.	4th Func.		CTRL	Reset State
57	PAD1	KWAD1	AN1	—	V_{DDA}	PER1AD/PPS1AD	Disabled
58	PAD9	KWAD9	AN9	—	V_{DDA}	PER0AD/PPS0AD	Disabled
59	PAD2	KWAD2	AN2	—	V_{DDA}	PER1AD/PPS1AD	Disabled
60	PAD10	KWAD10	AN10	—	V_{DDA}	PER0AD/PPS0AD	Disabled
61	PAD3	KWAD3	AN3	—	V_{DDA}	PER1AD/PPS1AD	Disabled
62	PAD11	KWAD11	AN11	—	V_{DDA}	PER0AD/PPS0AD	Disabled
63	PAD4	KWAD4	AN4	—	V_{DDA}	PER1AD/PPS1AD	Disabled
64	PAD12	KWAD12	—	—	V_{DDA}	PER0AD/PPS0AD	Disabled
65	PAD5	KWAD5	AN5	—	V_{DDA}	PER1AD/PPS1AD	Disabled
66	PAD13	KWAD13	—	—	V_{DDA}	PER0AD/PPS0AD	Disabled
67	PAD6	KWAD6	AN6	—	V_{DDA}	PER1AD/PPS1AD	Disabled
68	PAD14	KWAD14	—	—	V_{DDA}	PER0AD/PPS0AD	Disabled
69	PAD7	KWAD7	AN7	—	V_{DDA}	PER1AD/PPS1AD	Disabled
70	PAD15	KWAD15	—	—	V_{DDA}	PER0AD/PPS0AD	Disabled
71	PC4	—	—	—	V_{DDA}	PUCR/PUPCE	Disabled
72	PC5		—	—	V_{DDA}	PUCR/PUPCE	Disabled
73	PC6		—	—	V_{DDA}	PUCR/PUPCE	Disabled
74	PC7		—	—	V_{DDA}	PUCR/PUPCE	Disabled
75	VRH	—	—	—	—	—	—
76	VDDA	—	—	—	—	—	—
77	VSSA	—	—	—	—	—	—
78	PD0	—	—	—	V_{DDX}	PUCR/PUPDE	Disabled
79	PD1	—	—	—	V_{DDX}	PUCR/PUPDE	Disabled
80	PD2	—	—	—	V_{DDX}	PUCR/PUPDE	Disabled
81	PD3	—	—	—	V_{DDX}	PUCR/PUPDE	Disabled
82	PS0	RXD0	—	—	V_{DDX}	PERS/PPSS	Up
83	PS1	TXD0	—	—	V_{DDX}	PERS/PPSS	Up
84	PS2	RXD1	—	—	V_{DDX}	PERS/PPSS	Up
85	PS3	TXD1	—	—	V_{DDX}	PERS/PPSS	Up

[1] Read: Anytime
Write: Anytime

Table 2-73. PIEJ Register Field Descriptions

Field	Description
7-0 PIEJ	**Port J interrupt enable—** This bit enables or disables the edge sensitive pin interrupt on the associated pin. An interrupt can be generated if the pin is operating in input or output mode when in use with the general-purpose or related peripheral function. 1 Interrupt is enabled 0 Interrupt is disabled (interrupt flag masked)

2.4.3.48 Port J Interrupt Flag Register (PIFJ)

Address 0x026F (G1, G2) Access: User read/write[1]

	7	6	5	4	3	2	1	0
R W	PIFJ7	PIFJ6	PIFJ5	PIFJ4	PIFJ3	PIFJ2	PIFJ1	PIFJ0
Reset	0	0	0	0	0	0	0	0

Address 0x026F (G3) Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	0	0	0	0	PIFJ3	PIFJ2	PIFJ1	PIFJ0
W								
Reset	0	0	0	0	0	0	0	0

Figure 2-48. Port J Interrupt Flag Register (PIFJ)

[1] Read: Anytime
Write: Anytime, write 1 to clear

Table 2-74. PIFJ Register Field Descriptions

Field	Description
7-0 PIFJ	**Port J interrupt flag—** This flag asserts after a valid active edge was detected on the related pin (see Section 2.5.4.2, “Pin Interrupts and Wakeup”). This can be a rising or a falling edge based on the state of the polarity select register. An interrupt will occur if the associated interrupt enable bit is set. Writing a logic “1” to the corresponding bit field clears the flag. 1 Active edge on the associated bit has occurred 0 No active edge occurred

2.4.3.64 Port AD Interrupt Flag Register (PIF1AD)

Address 0x027F Access: User read/write[1]

	7	6	5	4	3	2	1	0
R W	PIF1AD7	PIF1AD6	PIF1AD5	PIF1AD4	PIF1AD3	PIF1AD2	PIF1AD1	PIF1AD0
Reset	0	0	0	0	0	0	0	0

Figure 2-63. Port AD Interrupt Flag Register (PIF1AD)

[1] Read: Anytime
Write: Anytime

Table 2-90. PIF1AD Register Field Descriptions

Field	Description
7-0 PIF1AD	**Port AD interrupt flag—** This flag asserts after a valid active edge was detected on the related pin (see Section 2.5.4.2, “Pin Interrupts and Wakeup”). This can be a rising or a falling edge based on the state of the polarity select register. An interrupt will occur if the associated interrupt enable bit is set. Writing a logic “1” to the corresponding bit field clears the flag. 1 Active edge on the associated bit has occurred 0 No active edge occurred

Chapter 3
5V Analog Comparator (ACMPV1)

Revision History

Rev. No. (Item No.)	Date (Submitted By)	Sections Affected	Substantial Change(s)
V00.08	13 Aug 2010		• Added register name to every bitfield reference
V00.09	10 Sep 2010		• Internal updates •
V01.00	18 Oct 2010		• Initial version •

3.1 Introduction

The analog comparator (ACMP) provides a circuit for comparing two analog input voltages. Refer to the device overview section for availability on a specific device.

3.2 Features

The ACMP has the following features:

- Low offset, low long-term offset drift
- Selectable interrupt on rising, falling, or rising and falling edges of comparator output
- Option to output comparator signal on an external pin ACMPO
- Option to trigger timer input capture events

3.3 Block Diagram

The block diagram of the ACMP is shown below.

10.1.3 S12CPMU Block Diagram

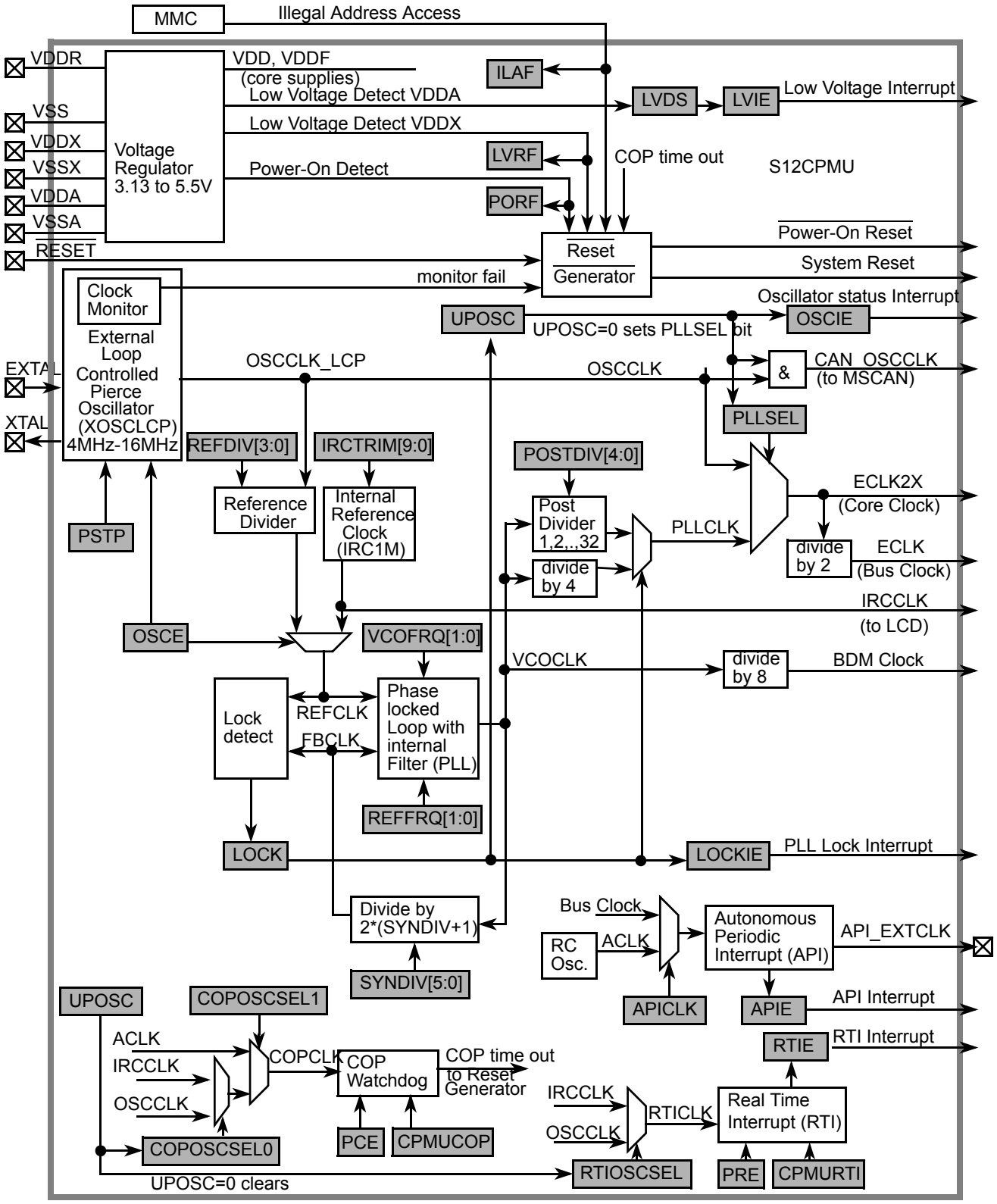

Figure 10-1. Block diagram of S12CPMU

Table 11-11. ATD Behavior in Freeze Mode (Breakpoint)

FRZ1	FRZ0	Behavior in Freeze Mode
0	1	Reserved
1	0	Finish current conversion, then freeze
1	1	Freeze Immediately

11.3.2.5 ATD Control Register 4 (ATDCTL4)

Writes to this register will abort current conversion sequence.

Module Base + 0x0004

Figure 11-7. ATD Control Register 4 (ATDCTL4)

Read: Anytime

Write: Anytime

Table 11-12. ATDCTL4 Field Descriptions

Field	Description
7–5 SMP[2:0]	**Sample Time Select** — These three bits select the length of the sample time in units of ATD conversion clock cycles. Note that the ATD conversion clock period is itself a function of the prescaler value (bits PRS4-0). Table 11-13 lists the available sample time lengths.
4–0 PRS[4:0]	**ATD Clock Prescaler** — These 5 bits are the binary prescaler value PRS. The ATD conversion clock frequency is calculated as follows: $f_{ATDCLK} = \frac{f_{BUS}}{2 \times (PRS + 1)}$ Refer to Device Specification for allowed frequency range of f_{ATDCLK}.

Table 11-13. Sample Time Select

SMP2	SMP1	SMP0	Sample Time in Number of ATD Clock Cycles
0	0	0	4
0	0	1	6
0	1	0	8
0	1	1	10
1	0	0	12
1	0	1	16
1	1	0	20
1	1	1	24

15.4 Functional Description

The ADC10B16C consists of an analog sub-block and a digital sub-block.

15.4.1 Analog Sub-Block

The analog sub-block contains all analog electronics required to perform a single conversion. Separate power supplies VDDA and VSSA allow to isolate noise of other MCU circuitry from the analog sub-block.

15.4.1.1 Sample and Hold Machine

The Sample and Hold Machine controls the storage and charge of the sample capacitor to the voltage level of the analog signal at the selected ADC input channel.

During the sample process the analog input connects directly to the storage node.

The input analog signals are unipolar and must be within the potential range of VSSA to VDDA.

During the hold process the analog input is disconnected from the storage node.

15.4.1.2 Analog Input Multiplexer

The analog input multiplexer connects one of the 16 external analog input channels to the sample and hold machine.

15.4.1.3 Analog-to-Digital (A/D) Machine

The A/D Machine performs analog to digital conversions. The resolution is program selectable to be either 8 or 10 bits. The A/D machine uses a successive approximation architecture. It functions by comparing the sampled and stored analog voltage with a series of binary coded discrete voltages.

By following a binary search algorithm, the A/D machine identifies the discrete voltage that is nearest to the sampled and stored voltage.

When not converting the A/D machine is automatically powered down.

Only analog input signals within the potential range of VRL to VRH (A/D reference potentials) will result in a non-railed digital output code.

15.4.2 Digital Sub-Block

This subsection describes some of the digital features in more detail. See Section 15.3.2, “Register Descriptions” for all details.

15.4.2.1 External Trigger Input

The external trigger feature allows the user to synchronize ATD conversions to an external event rather than relying only on software to trigger the ATD module when a conversion is about to take place. The external trigger signal (out of reset ATD channel 15, configurable in ATDCTL1) is programmable to be

Each channel counter can be read at anytime without affecting the count or the operation of the PWM channel.

Any value written to the counter causes the counter to reset to $00, the counter direction to be set to up, the immediate load of both duty and period registers with values from the buffers, and the output to change according to the polarity bit. When the channel is disabled (PWMEx = 0), the counter stops. When a channel becomes enabled (PWMEx = 1), the associated PWM counter continues from the count in the PWMCNTx register. This allows the waveform to continue where it left off when the channel is re-enabled. When the channel is disabled, writing “0” to the period register will cause the counter to reset on the next selected clock.

NOTE

If the user wants to start a new “clean” PWM waveform without any “history” from the old waveform, the user must write to channel counter (PWMCNTx) prior to enabling the PWM channel (PWMEx = 1).

Generally, writes to the counter are done prior to enabling a channel in order to start from a known state. However, writing a counter can also be done while the PWM channel is enabled (counting). The effect is similar to writing the counter when the channel is disabled, except that the new period is started immediately with the output set according to the polarity bit.

NOTE

Writing to the counter while the channel is enabled can cause an irregular PWM cycle to occur.

The counter is cleared at the end of the effective period (see Section 19.4.2.5, “Left Aligned Outputs” and Section 19.4.2.6, “Center Aligned Outputs” for more details).

Table 19-12. PWM Timer Counter Conditions

Counter Clears ($00)	Counter Counts	Counter Stops
When PWMCNTx register written to any value	When PWM channel is enabled (PWMEx = 1). Counts from last value in PWMCNTx.	When PWM channel is disabled (PWMEx = 0)
Effective period ends		

19.4.2.5 Left Aligned Outputs

The PWM timer provides the choice of two types of outputs, left aligned or center aligned. They are selected with the CAEx bits in the PWMCAE register. If the CAEx bit is cleared (CAEx = 0), the corresponding PWM output will be left aligned.

In left aligned output mode, the 8-bit counter is configured as an up counter only. It compares to two registers, a duty register and a period register as shown in the block diagram in Figure 19-16. When the PWM counter matches the duty register the output flip-flop changes state causing the PWM waveform to also change state. A match between the PWM counter and the period register resets the counter and the output flip-flop, as shown in Figure 19-16, as well as performing a load from the double buffer period and duty register to the associated registers, as described in Section 19.4.2.3, “PWM Period and Duty”. The counter counts from 0 to the value in the period register – 1.

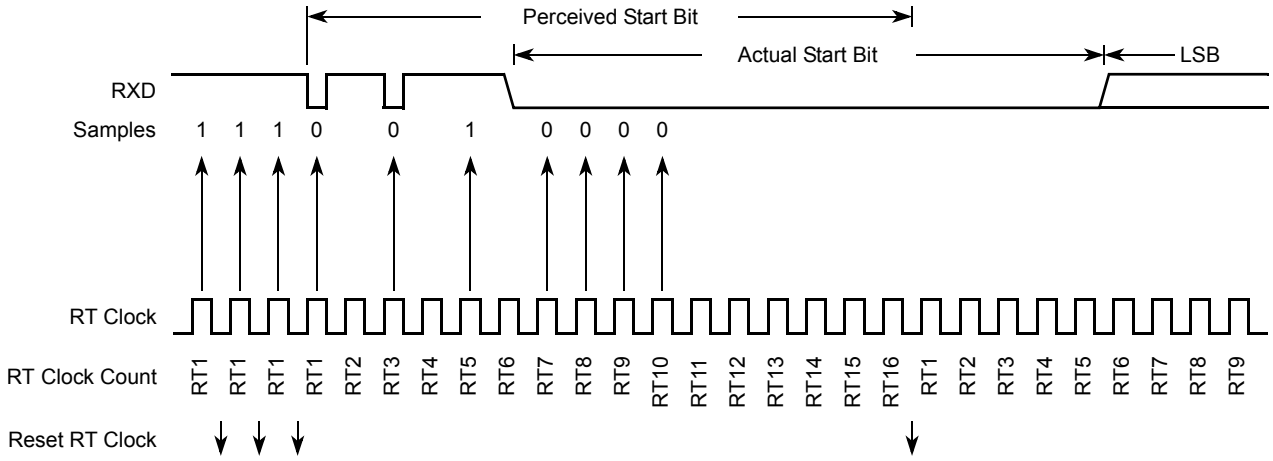

Figure 20-24. Start Bit Search Example 3

Figure 20-25 shows the effect of noise early in the start bit time. Although this noise does not affect proper synchronization with the start bit time, it does set the noise flag.

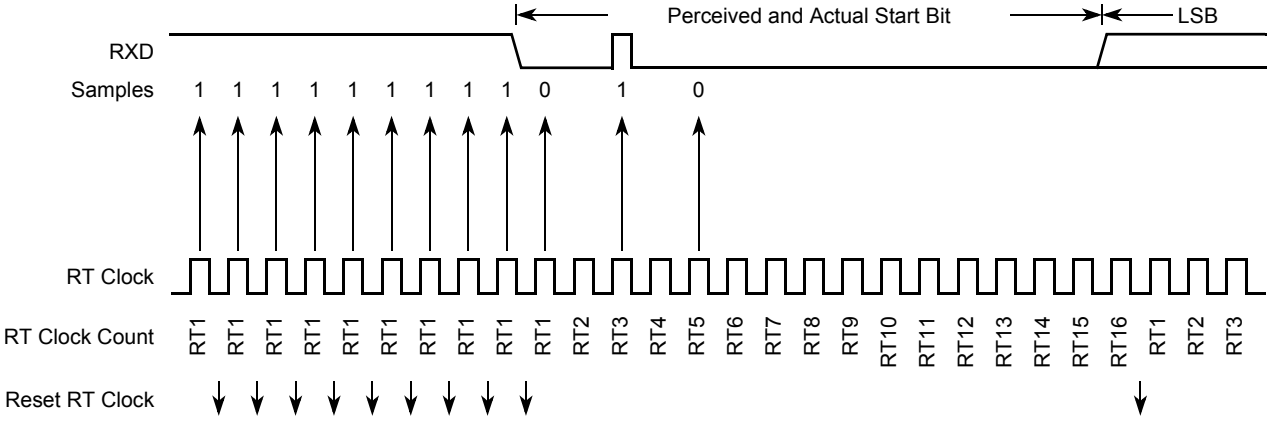

Figure 20-25. Start Bit Search Example 4

Figure 20-26 shows a burst of noise near the beginning of the start bit that resets the RT clock. The sample after the reset is low but is not preceded by three high samples that would qualify as a falling edge. Depending on the timing of the start bit search and on the data, the frame may be missed entirely or it may set the framing error flag.

NOTE

In single-wire operation data from the TXD pin is inverted if RXPOL is set.

20.4.8 Loop Operation

In loop operation the transmitter output goes to the receiver input. The RXD pin is disconnected from the SCI.

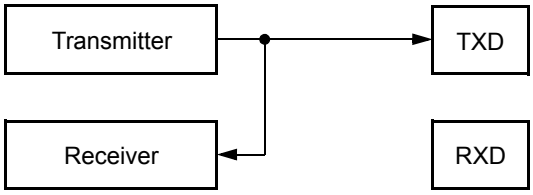

Figure 20-31. Loop Operation (LOOPS = 1, RSRC = 0)

Enable loop operation by setting the LOOPS bit and clearing the RSRC bit in SCI control register 1 (SCICR1). Setting the LOOPS bit disables the path from the RXD pin to the receiver. Clearing the RSRC bit connects the transmitter output to the receiver input. Both the transmitter and receiver must be enabled (TE = 1 and RE = 1).

NOTE

In loop operation data from the transmitter is not recognized by the receiver if RXPOL and TXPOL are not the same.

20.5 Initialization/Application Information

20.5.1 Reset Initialization

See Section 20.3.2, “Register Descriptions”.

20.5.2 Modes of Operation

20.5.2.1 Run Mode

Normal mode of operation.

To initialize a SCI transmission, see Section 20.4.5.2, “Character Transmission”.

20.5.2.2 Wait Mode

SCI operation in wait mode depends on the state of the SCISWAI bit in the SCI control register 1 (SCICR1).

- If SCISWAI is clear, the SCI operates normally when the CPU is in wait mode.
- If SCISWAI is set, SCI clock generation ceases and the SCI module enters a power-conservation state when the CPU is in wait mode. Setting SCISWAI does not affect the state of the receiver enable bit, RE, or the transmitter enable bit, TE.

Table 24-34. Erase Verify P-Flash Section Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x03	Global address [17:16] of a P-Flash block
001	Global address [15:0] of the first phrase to be verified	
010	Number of phrases to be verified	

Upon clearing CCIF to launch the Erase Verify P-Flash Section command, the Memory Controller will verify the selected section of Flash memory is erased. The CCIF flag will set after the Erase Verify P-Flash Section operation has completed. If the section is not erased, it means blank check failed, both MGSTAT bits will be set.

Table 24-35. Erase Verify P-Flash Section Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 010 at command launch
		Set if command not available in current mode (see Table 24-25)
		Set if an invalid global address [17:0] is supplied see Table 24-3)[1]
		Set if a misaligned phrase address is supplied (global address [2:0] != 000)
		Set if the requested section crosses a the P-Flash address boundary
	FPVIOL	None
	MGSTAT1	Set if any errors have been encountered during the read[2] or if blank check failed.
	MGSTAT0	Set if any non-correctable errors have been encountered during the read[2] or if blank check failed.

1 As defined by the memory map for FTMRG32K1.

2 As found in the memory map for FTMRG32K1.

24.4.6.4 Read Once Command

The Read Once command provides read access to a reserved 64 byte field (8 phrases) located in the nonvolatile information register of P-Flash. The Read Once field is programmed using the Program Once command described in Section 24.4.6.6. The Read Once command must not be executed from the Flash block containing the Program Once reserved field to avoid code runaway.

Table 24-36. Read Once Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x04	Not Required
001	Read Once phrase index (0x0000 - 0x0007)	
010	Read Once word 0 value	
011	Read Once word 1 value	
100	Read Once word 2 value	

- Fast sector erase and phrase program operation
- Ability to read the P-Flash memory while programming a word in the EEPROM memory
- Flexible protection scheme to prevent accidental program or erase of P-Flash memory

26.1.2.2 EEPROM Features

- 1.5Kbytes of EEPROM memory composed of one 1.5Kbyte Flash block divided into 384 sectors of 4 bytes
- Single bit fault correction and double bit fault detection within a word during read operations
- Automated program and erase algorithm with verify and generation of ECC parity bits
- Fast sector erase and word program operation
- Protection scheme to prevent accidental program or erase of EEPROM memory
- Ability to program up to four words in a burst sequence

26.1.2.3 Other Flash Module Features

- No external high-voltage power supply required for Flash memory program and erase operations
- Interrupt generation on Flash command completion and Flash error detection
- Security mechanism to prevent unauthorized access to the Flash memory

Table 30-43. Program Once Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 101 at command launch
		Set if command not available in current mode (see Table 30-27)
		Set if an invalid phrase index is supplied
		Set if the requested phrase has already been programmed[1]
	FPVIOL	None
	MGSTAT1	Set if any errors have been encountered during the verify operation
	MGSTAT0	Set if any non-correctable errors have been encountered during the verify operation

1 If a Program Once phrase is initially programmed to 0xFFFF_FFFF_FFFF_FFFF, the Program Once command will be allowed to execute again on that same phrase.

30.4.6.7 Erase All Blocks Command

The Erase All Blocks operation will erase the entire P-Flash and EEPROM memory space.

Table 30-44. Erase All Blocks Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x08	Not required

Upon clearing CCIF to launch the Erase All Blocks command, the Memory Controller will erase the entire Flash memory space and verify that it is erased. If the Memory Controller verifies that the entire Flash memory space was properly erased, security will be released. During the execution of this command (CCIF=0) the user must not write to any Flash module register. The CCIF flag will set after the Erase All Blocks operation has completed.

Table 30-45. Erase All Blocks Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 000 at command launch
		Set if command not available in current mode (see Table 30-27)
	FPVIOL	Set if any area of the P-Flash or EEPROM memory is protected
	MGSTAT1	Set if any errors have been encountered during the verify operation
	MGSTAT0	Set if any non-correctable errors have been encountered during the verify operation

30.4.6.8 Erase Flash Block Command

The Erase Flash Block operation will erase all addresses in a P-Flash or EEPROM block.

31.3.2.9.1 P-Flash Protection Restrictions

The general guideline is that P-Flash protection can only be added and not removed. Table 31-21 specifies all valid transitions between P-Flash protection scenarios. Any attempt to write an invalid scenario to the FPROT register will be ignored. The contents of the FPROT register reflect the active protection scenario. See the FPHS and FPLS bit descriptions for additional restrictions.

Table 31-21. P-Flash Protection Scenario Transitions

From Protection Scenario	To Protection Scenario[1]							
	0	1	2	3	4	5	6	7
0	X	X	X	X				
1		X		X				
2			X	X				
3				X				
4				X	X			
5			X	X	X	X		
6		X		X	X		X	
7	X	X	X	X	X	X	X	X

1 Allowed transitions marked with X, see Figure 31-14 for a definition of the scenarios.

31.3.2.10 EEPROM Protection Register (EEPROT)

The EEPROT register defines which EEPROM sectors are protected against program and erase operations.

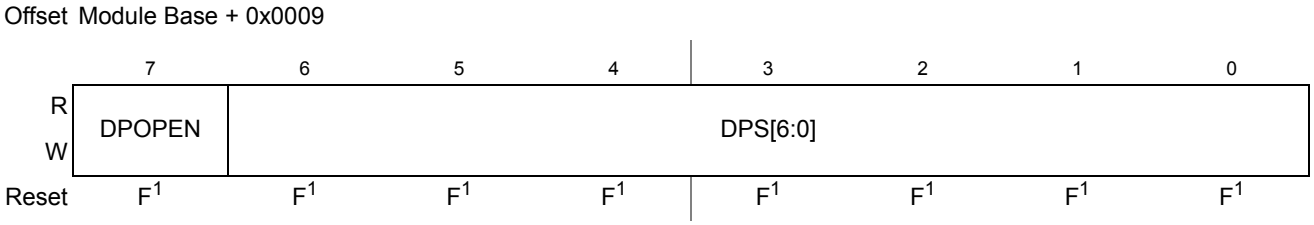

Figure 31-15. EEPROM Protection Register (EEPROT)

1 Loaded from IFR Flash configuration field, during reset sequence.

The (unreserved) bits of the EEPROT register are writable with the restriction that protection can be added but not removed. Writes must increase the DPS value and the DPOPEN bit can only be written from 1 (protection disabled) to 0 (protection enabled). If the DPOPEN bit is set, the state of the DPS bits is irrelevant.

During the reset sequence, fields DPOPEN and DPS of the EEPROT register are loaded with the contents of the EEPROM protection byte in the Flash configuration field at global address 0x3_FF0D located in

in an error (10-bit resolution) of less than 1/2 LSB (2.5 mV) at the maximum leakage current. If device or operating conditions are less than worst case or leakage-induced error is acceptable, larger values of source resistance of up to 10Kohm are allowed.

A.4.2.4 Source Capacitance

When sampling an additional internal capacitor is switched to the input. This can cause a voltage drop due to charge sharing with the external and the pin capacitance. For a maximum sampling error of the input voltage ≤ 1LSB (10-bit resilution), then the external filter capacitor, $C_f \geq 1024 * (C_{INS}–C_{INN})$.

A.4.2.5 Current Injection

There are two cases to consider.

1. A current is injected into the channel being converted. The channel being stressed has conversion values of $3FF (in 10-bit mode) for analog inputs greater than V_{RH} and $000 for values less than V_{RL} unless the current is higher than specified as disruptive condition.
2. Current is injected into pins in the neighborhood of the channel being converted. A portion of this current is picked up by the channel (coupling ratio K), This additional current impacts the accuracy of the conversion depending on the source resistance.

   The additional input voltage error on the converted channel can be calculated as:

   $$V_{ERR} = K * R_S * I_{INJ}$$

   with I_{INJ} being the sum of the currents injected into the two pins adjacent to the converted channel.

Table A-20. ADC Electrical Characteristics

Supply voltage 3.13 V < V_{DDA} < 5.5 V, -40°C < T_J < T_{Jmax}[1]							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	C	Max input source resistance[2]	R_S	—	—	1	KΩ
2	D	Total input capacitance Non sampling Total input capacitance Sampling	C_{INN} C_{INS}	— —	— —	10 16	pF
3	D	Input internal Resistance	R_{INA}	-	5	15	kΩ
4	C	Disruptive analog input current	I_{NA}	-2.5	—	2.5	mA
5	C	Coupling ratio positive current injection	K_p	—	—	1E-4	A/A
6	C	Coupling ratio negative current injection	K_n	—	—	5E-3	A/A

1 see Table A-4

2 1 Refer to A.4.2.3 for further information concerning source resistance

A.4.3 ADC Accuracy

Table A-21 and Table A-26 specifies the ADC conversion performance excluding any errors due to current injection, input capacitance and source resistance.

Appendix D
Package and Die Information

Revision History

Version Number	Revision Date	Description of Changes
Rev 0.01	2-Jan-2009	Initial release
Rev 0.02	25-Jan-2013	• Added D.7, “KGD Information”
Rev 0.03	31-Jan-2013	• Updated , “Bondpad Coordinates”

NOTES:

1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M–1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE AB IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS T, U, AND Z TO BE DETERMINED AT DATUM PLANE AB.
5. DIMENSIONS TO BE DETERMINED AT SEATING PLANE AC.
6. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 PER SIDE. DIMENSIONS DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE AB.
7. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.350.
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076.
9. EXACT SHAPE OF EACH CORNER IS OPTIONAL.

© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	**MECHANICAL OUTLINE**	PRINT VERSION NOT TO SCALE	
TITLE: LQFP, 48 LEAD, 0.50 PITCH (7.0 X 7.0 X 1.4)	DOCUMENT NO: 98ASH00962A		REV: G
	CASE NUMBER: 932-03		14 APR 2005
	STANDARD: JEDEC MS-026-BBC		