Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	12V1
Core Size	16-Bit
Speed	25MHz
Connectivity	CANbus, IrDA, LINbus, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	86
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	3K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3.13V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s9s12g96f0vll

A.1.4 Current Injection . . . 1179
A.1.5 Absolute Maximum Ratings . . . 1179
A.1.6 ESD Protection and Latch-up Immunity . . . 1180
A.1.7 Operating Conditions . . . 1181
A.1.8 Power Dissipation and Thermal Characteristics . . . 1183
A.2 I/O Characteristics . . . 1187
A.3 Supply Currents . . . 1191
A.3.1 Measurement Conditions . . . 1191
A.4 ADC Characteristics . . . 1196
A.4.1 ADC Operating Characteristics . . . 1196
A.4.2 Factors Influencing Accuracy . . . 1197
A.4.3 ADC Accuracy . . . 1198
A.4.4 ADC Temperature Sensor . . . 1208
A.5 ACMP Characteristics . . . 1208
A.6 DAC Characteristics . . . 1210
A.7 NVM . . . 1211
A.7.1 Timing Parameters . . . 1211
A.7.2 NVM Reliability Parameters . . . 1216
A.8 Phase Locked Loop . . . 1217
A.8.1 Jitter Definitions . . . 1217
A.8.2 Electrical Characteristics for the PLL . . . 1219
A.9 Electrical Characteristics for the IRC1M . . . 1219
A.10 Electrical Characteristics for the Oscillator (XOSCLCP) . . . 1221
A.11 Reset Characteristics . . . 1222
A.12 Electrical Specification for Voltage Regulator . . . 1223
A.13 Chip Power-up and Voltage Drops . . . 1225
A.14 MSCAN . . . 1226
A.15 SPI Timing . . . 1227
A.15.1 Master Mode . . . 1227
A.15.2 Slave Mode . . . 1229
A.16 ADC Conversion Result Reference . . . 1231

Appendix B
Detailed Register Address Map

B.1 Detailed Register Map . . . 1233

Appendix C
Ordering and Shipping Information

C.1 Ordering Information . . . 1253

Appendix D
Package and Die Information

D.1 100 LQFP Mechanical Dimensions . . . 1256
D.2 64 LQFP Mechanical Dimensions . . . 1259

- Bus-off recovery by software intervention or automatically
- 16-bit time stamp of transmitted/received messages

1.3.12 Serial Communication Interface Module (SCI)

- Up to three SCI modules
- Full-duplex or single-wire operation
- Standard mark/space non-return-to-zero (NRZ) format
- Selectable IrDA 1.4 return-to-zero-inverted (RZI) format with programmable pulse widths
- 13-bit baud rate selection
- Programmable character length
- Programmable polarity for transmitter and receiver
- Active edge receive wakeup
- Break detect and transmit collision detect supporting LIN 1.3, 2.0, 2.1 and SAE J2602

1.3.13 Serial Peripheral Interface Module (SPI)

- Up to three SPI modules
- Configurable 8- or 16-bit data size
- Full-duplex or single-wire bidirectional
- Double-buffered transmit and receive
- Master or slave mode
- MSB-first or LSB-first shifting
- Serial clock phase and polarity options

1.3.14 Analog-to-Digital Converter Module (ADC)

Up to 16-channel, 10-bit/12-bit[1] analog-to-digital converter

  — 3 us conversion time
  — 8-/10[1]-bit resolution
  — Left or right justified result data
  — Wakeup from low power modes on analog comparison > or <= match
  — Continuous conversion mode
  — External triggers to initiate conversions via GPIO or peripheral outputs such as PWM or TIM
  — Multiple channel scans
  — Precision fixed voltage reference for ADC conversions
  —

- Pins can also be used as digital I/O including wakeup capability

1. 12-bit resolution only available on S12GA192 and S12GA240 devices.

Table 1-20. 48-Pin LQFP Pinout for S12G96 and S12G128

	Function <----lowest-----PRIORITY-----highest---->					Power Supply	Internal Pull Resistor	
Package Pin	Pin	2nd Func.	3rd Func.	4th Func	5th Func		CTRL	Reset State
30	PAD10	KWAD10	AN10			V_{DDA}	PER0AD/PPS0AD	Disabled
31	PAD3	KWAD3	AN3	—	—	V_{DDA}	PER1AD/PPS1AD	Disabled
32	PAD11	KWAD11	AN11	—	—	V_{DDA}	PER0AD/PPS0AD	Disabled
33	PAD4	KWAD4	AN4	—	—	V_{DDA}	PER1AD/PPS1AD	Disabled
34	PAD5	KWAD5	AN5	—	—	V_{DDA}	PER1AD/PPS0AD	Disabled
35	PAD6	KWAD6	AN6	—	—	V_{DDA}	PER1AD/PPS1AD	Disabled
36	PAD7	KWAD7	AN7	—	—	V_{DDA}	PER1AD/PPS1AD	Disabled
37	VDDA	VRH	—	—	—	—	—	—
38	VSSA	—	—	—	—	—	—	—
39	PS0	RXD0	—	—	—	V_{DDX}	PERS/PPSS	Up
40	PS1	TXD0	—	—	—	V_{DDX}	PERS/PPSS	Up
41	PS2	RXD1	—	—	—	V_{DDX}	PERS/PPSS	Up
42	PS3	TXD1	—	—	—	V_{DDX}	PERS/PPSS	Up
43	PS4	MISO0	—	—	—	V_{DDX}	PERS/PPSS	Up
44	PS5	MOSI0	—	—	—	V_{DDX}	PERS/PPSS	Up
45	PS6	SCK0	—	—	—	V_{DDX}	PERS/PPSS	Up
46	PS7	API_EXTCLK	ECLK	$\overline{SS0}$	—	V_{DDX}	PERS/PPSS	Up
47	PM0	RXD2	RXCAN	—	—	V_{DDX}	PERM/PPSM	Disabled
48	PM1	TXD2	TXCAN	—	—	V_{DDX}	PERM/PPSM	Disabled

[1] The regular I/O characteristics (see Section A.2, “I/O Characteristics”) apply if the EXTAL/XTAL function is disabled

Table 1-23. 48-Pin LQFP Pinout for S12GA96 and S12GA128

	Function <----lowest-----PRIORITY-----highest---->					Power Supply	Internal Pull Resistor	
Package Pin	Pin	2nd Func.	3rd Func.	4th Func	5th Func		CTRL	Reset State
30	PAD10	KWAD10	AN10			V_{DDA}	PER0AD/PPS0AD	Disabled
31	PAD3	KWAD3	AN3	—	—	V_{DDA}	PER1AD/PPS1AD	Disabled
32	PAD11	KWAD11	AN11	—	—	V_{DDA}	PER0AD/PPS0AD	Disabled
33	PAD4	KWAD4	AN4	—	—	V_{DDA}	PER1AD/PPS1AD	Disabled
34	PAD5	KWAD5	AN5	—	—	V_{DDA}	PER1AD/PPS0AD	Disabled
35	PAD6	KWAD6	AN6	—	—	V_{DDA}	PER1AD/PPS1AD	Disabled
36	PAD7	KWAD7	AN7	—	—	V_{DDA}	PER1AD/PPS1AD	Disabled
37	VDDA	VRH	—	—	—	—	—	—
38	VSSA	—	—	—	—	—	—	—
39	PS0	RXD0	—	—	—	V_{DDX}	PERS/PPSS	Up
40	PS1	TXD0	—	—	—	V_{DDX}	PERS/PPSS	Up
41	PS2	RXD1	—	—	—	V_{DDX}	PERS/PPSS	Up
42	PS3	TXD1	—	—	—	V_{DDX}	PERS/PPSS	Up
43	PS4	MISO0	—	—	—	V_{DDX}	PERS/PPSS	Up
44	PS5	MOSI0	—	—	—	V_{DDX}	PERS/PPSS	Up
45	PS6	SCK0	—	—	—	V_{DDX}	PERS/PPSS	Up
46	PS7	API_EXTCLK	ECLK	$\overline{SS0}$	—	V_{DDX}	PERS/PPSS	Up
47	PM0	RXD2	RXCAN	—	—	V_{DDX}	PERM/PPSM	Disabled
48	PM1	TXD2	TXCAN	—	—	V_{DDX}	PERM/PPSM	Disabled

[1] The regular I/O characteristics (see Section A.2, “I/O Characteristics”) apply if the EXTAL/XTAL function is disabled

Table 1-28. 100-Pin LQFP Pinout for S12G192 and S12G240

	Function <----lowest-----PRIORITY-----highest---->				Power Supply	Internal Pull Resistor	
Package Pin	Pin	2nd Func.	3rd Func.	4th Func.		CTRL	Reset State
28	PB3	—	—	—	V_{DDX}	PUCR/PUPBE	Disabled
29	PP0	KWP0	ETRIG0	PWM0	V_{DDX}	PERP/PPSP	Disabled
30	PP1	KWP1	ETRIG1	PWM1	V_{DDX}	PERP/PPSP	Disabled
31	PP2	KWP2	ETRIG2	PWM2	V_{DDX}	PERP/PPSP	Disabled
32	PP3	KWP3	ETRIG3	PWM3	V_{DDX}	PERP/PPSP	Disabled
33	PP4	KWP4	PWM4	—	V_{DDX}	PERP/PPSP	Disabled
34	PP5	KWP5	PWM5	—	V_{DDX}	PERP/PPSP	Disabled
35	PP6	KWP6	PWM6	—	V_{DDX}	PERP/PPSP	Disabled
36	PP7	KWP7	PWM7	—	V_{DDX}	PERP/PPSP	Disabled
37	VDDX3	—	—	—	—	—	—
38	VSSX3	—	—	—	—	—	—
39	PT7	IOC7	—	—	V_{DDX}	PERT/PPST	Disabled
40	PT6	IOC6	—	—	V_{DDX}	PERT/PPST	Disabled
41	PT5	IOC5	—	—	V_{DDX}	PERT/PPST	Disabled
42	PT4	IOC4	—	—	V_{DDX}	PERT/PPST	Disabled
43	PT3	IOC3	—	—	V_{DDX}	PERT/PPST	Disabled
44	PT2	IOC2	—	—	V_{DDX}	PERT/PPST	Disabled
45	PT1	IOC1	—	—	V_{DDX}	PERT/PPST	Disabled
46	PT0	IOC0	—	—	V_{DDX}	PERT/PPST	Disabled
47	PB4	$\overline{\text{IRQ}}$	—	—	V_{DDX}	PUCR/PUPBE	Disabled
48	PB5	$\overline{\text{XIRQ}}$	—	—	V_{DDX}	PUCR/PUPBE	Disabled
49	PB6	—	—	—	V_{DDX}	PUCR/PUPBE	Disabled
50	PB7	—	—	—	V_{DDX}	PUCR/PUPBE	Disabled
51	PC0	—	—	—	V_{DDA}	PUCR/PUPCE	Disabled
52	PC1	—	—	—	V_{DDA}	PUCR/PUPCE	Disabled
53	PC2	—	—	—	V_{DDA}	PUCR/PUPCE	Disabled
54	PC3	—	—	—	V_{DDA}	PUCR/PUPCE	Disabled
55	PAD0	KWAD0	AN0	—	V_{DDA}	PER1AD/PPS1AD	Disabled
56	PAD8	KWAD8	AN8	—	V_{DDA}	PER0AD/PPS0AD	Disabled

Table 2-21. Block Register Map (G3) (continued)

Global Address Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x027C PIE0AD	R	0	0	0	0	PIE0AD3	PIE0AD2	PIE0AD1	PIE0AD0
	W								
0x027D PIE1AD	R	PIE1AD7	PIE1AD6	PIE1AD5	PIE1AD4	PIE1AD3	PIE1AD2	PIE1AD1	PIE1AD0
	W								
0x027E PIF0AD	R	0	0	0	0	PIF0AD3	PIF0AD2	PIF0AD1	PIF0AD0
	W								
0x027F PIF1AD	R	PIF1AD7	PIF1AD6	PIF1AD5	PIF1AD4	PIF1AD3	PIF1AD2	PIF1AD1	PIF1AD0
	W								

= Unimplemented or Reserved

2.4.3 Register Descriptions

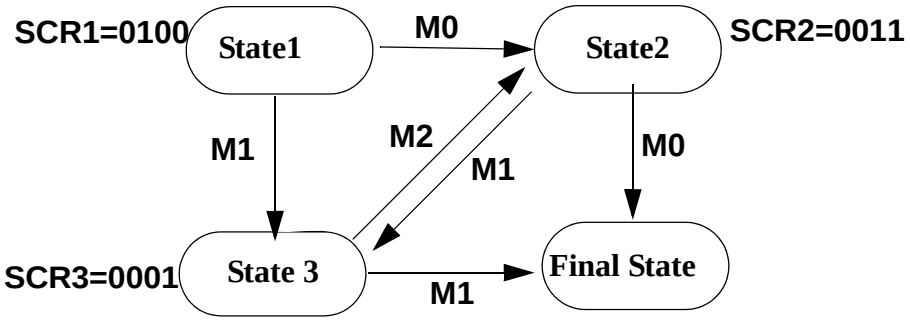
This section describes the details of all configuration registers. Every register has the same functionality in all groups if not specified separately. Refer to the register figures for reserved locations. If not stated differently, writing to reserved bits has not effect and read returns zero.

NOTE

- All register read accesses are synchronous to internal clocks
- General-purpose data output availability depends on prioritization; input data registers always reflect the pin status independent of the use
- Pull-device availability, pull-device polarity, wired-or mode, key-wakeup functionality are independent of the prioritization unless noted differently in section Section 2.3, “PIM Routing - Functional description”.

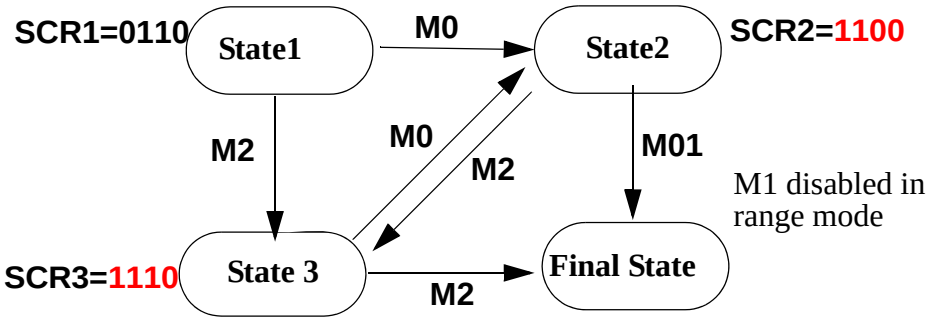
event B cause a trigger. Similarly 2 consecutive occurrences of event B without an intermediate event A cause a trigger. This is possible by using CompA and CompC to match on the same address as shown.

Figure 8-32. Scenario 4a



This scenario is currently not possible using 2 comparators only. S12SDBGV2 makes it possible with 2 comparators, State 3 allowing a M0 to return to state 2, whilst a M2 leads to final state as shown.

Figure 8-33. Scenario 4b (with 2 comparators)



The advantage of using only 2 channels is that now range comparisons can be included (channel0)

This however violates the S12SDBGV1 specification, which states that a match leading to final state always has priority in case of a simultaneous match, whilst priority is also given to the lowest channel number. For S12SDBG the corresponding CPU priority decoder is removed to support this, such that on simultaneous taghits, taghits pointing to final state have highest priority. If no taghit points to final state then the lowest channel number has priority. Thus with the above encoding from State3, the CPU and DBG would break on a simultaneous M0/M2.

This method requires that:

- The application software previously programmed into the microcontroller has been designed to have the capability to erase and program the Flash options/security byte, or security is first disabled using the backdoor key method, allowing BDM to be used to issue commands to erase and program the Flash options/security byte.
- The Flash sector containing the Flash options/security byte is not protected.

9.1.7 Complete Memory Erase (Special Modes)

The microcontroller can be unsecured in special modes by erasing the entire EEPROM and Flash memory contents.

When a secure microcontroller is reset into special single chip mode (SS), the BDM firmware verifies whether the EEPROM and Flash memory are erased. If any EEPROM or Flash memory address is not erased, only BDM hardware commands are enabled. BDM hardware commands can then be used to write to the EEPROM and Flash registers to mass erase the EEPROM and all Flash memory blocks.

When next reset into special single chip mode, the BDM firmware will again verify whether all EEPROM and Flash memory are erased, and this being the case, will enable all BDM commands, allowing the Flash options/security byte to be programmed to the unsecured value. The security bits SEC[1:0] in the Flash security register will indicate the unsecure state following the next reset.

0x02FA

	7	6	5	4	3	2	1	0
R	OSCE	Reserved	OSCPINS_EN	Reserved]				
W								
Reset	0	0	0	0	0	0	0	0

Figure 10-27. S12CPMU Oscillator Register (CPMUOSC)

Read: Anytime

Write: Anytime if PROT=0 (CPMUPROT register) and PLLSEL=1 (CPMUCLKS register). Else write has no effect.

NOTE.

Write to this register clears the LOCK and UPOSC status bits.

Table 10-24. CPMUOSC Field Descriptions

Field	Description
7 OSCE	**Oscillator Enable Bit** — This bit enables the external oscillator (XOSCLCP). The UPOSC status bit in the CPMUFLG register indicates when the oscillation is stable and OSCCLK can be selected as Bus Clock or source of the COP or RTI. A loss of oscillation will lead to a clock monitor reset. 0 External oscillator is disabled. REFCLK for PLL is IRCCLK. 1 External oscillator is enabled.Clock monitor is enabled.External oscillator is qualified by PLLCLK REFCLK for PLL is the external oscillator clock divided by REFDIV. **Note:** When starting up the external oscillator (either by programming OSCE bit to 1 or on exit from Full Stop Mode with OSCE bit already 1) the software must wait for a minimum time equivalent to the startup-time of the external oscillator t_{UPOSC} before entering Pseudo Stop Mode.
6 Reserved	Do not alter this bit from its reset value. It is for Manufacturer use only and can change the PLL behavior.
5 OSCPINS_EN	Oscillator Pins EXTAL and XTAL Enable Bit If OSCE=1 this read-only bit is set. It can only be cleared with the next reset. Enabling the external oscillator reserves the EXTAL and XTAL pins exclusively for oscillator application. 0 EXTAL and XTAL pins are not reserved for oscillator. 1 EXTAL and XTAL pins exclusively reserved for oscillator.
4-0 Reserved	Do not alter these bits from their reset value. It is for Manufacturer use only and can change the PLL behavior.

10.3.2.20 S12CPMU Protection Register (CPMUPROT)

This register protects the following clock configuration registers from accidental overwrite:

Chapter 11
Analog-to-Digital Converter (ADC10B8CV2)

Revision History

Version Number	Revision Date	Effective Date	Author	Description of Changes
V02.00	13 May 2009	13 May 2009		Initial version copied from V01.05, changed unused Bits in ATDDIEN to read logic 1
V02.01	17 Dec 2009	17 Dec 2009		Updated Table 11-15 Analog Input Channel Select Coding - description of internal channels. Updated register ATDDR (left/right justified result) description in section 11.3.2.12.1/11-424 and 11.3.2.12.2/11-425 and added Table 11-21 to improve feature description.
V02.02	09 Feb 2010	09 Feb 2010		Fixed typo in Table 11-9 - conversion result for 3mV and 10bit resolution
V02.03	26 Feb 2010	26 Feb 2010		Corrected Table 11-15 Analog Input Channel Select Coding - description of internal channels.
V02.04	14 Apr 2010	14 Apr 2010		Corrected typos to be in-line with SoC level pin naming conventions for VDDA, VSSA, VRL and VRH.
V02.05	25 Aug 2010	25 Aug 2010		Removed feature of conversion during STOP and general wording clean up done in Section 11.4, “Functional Description
V02.06	09 Sep 2010	09 Sep 2010		Update of internal only information.
V02.07	11 Feb 2011	11 Feb 2011		Connectivity Information regarding internal channel_6 added to Table 11-15.
V02.08	22. Jun 2012	22. Jun 2012		Updated register wirte access information in section 11.3.2.9/11-422
V02.09	29. Jun 2012	29 Jun 2012		Removed IP name in block diagram Figure 11-1
V02.10	02 Oct 2012	02 Oct 2012		Added user information to avoid maybe false external trigger events when enabling the external trigger mode (Section 11.4.2.1, “External Trigger Input).

11.1 Introduction

The ADC10B8C is a 8-channel, 10-bit, multiplexed input successive approximation analog-to-digital converter. Refer to device electrical specifications for ATD accuracy.

14.5 Resets

At reset the ADC12B12C is in a power down state. The reset state of each individual bit is listed within the Register Description section (see Section 14.3.2, “Register Descriptions”) which details the registers and their bit-field.

14.6 Interrupts

The interrupts requested by the ADC12B12C are listed in Table 14-24. Refer to MCU specification for related vector address and priority.

Table 14-24. ATD Interrupt Vectors

Interrupt Source	CCR Mask	Local Enable
Sequence Complete Interrupt	I bit	ASCIE in ATDCTL2
Compare Interrupt	I bit	ACMPIE in ATDCTL2

See Section 14.3.2, “Register Descriptions” for further details.

Table 15-16. ATDSTAT0 Field Descriptions (continued)

Field	Description
3–0 CC[3:0]	**Conversion Counter** — These 4 read-only bits are the binary value of the conversion counter. The conversion counter points to the result register that will receive the result of the current conversion. E.g. CC3=0, CC2=1, CC1=1, CC0=0 indicates that the result of the current conversion will be in ATD Result Register 6. If in non-FIFO mode (FIFO=0) the conversion counter is initialized to zero at the beginning and end of the conversion sequence. If in FIFO mode (FIFO=1) the register counter is not initialized. The conversion counter wraps around when its maximum value is reached. Aborting a conversion or starting a new conversion clears the conversion counter even if FIFO=1.

15.3.2.8 ATD Compare Enable Register (ATDCMPE)

Writes to this register will abort current conversion sequence.

Read: Anytime

Write: Anytime

Module Base + 0x0008

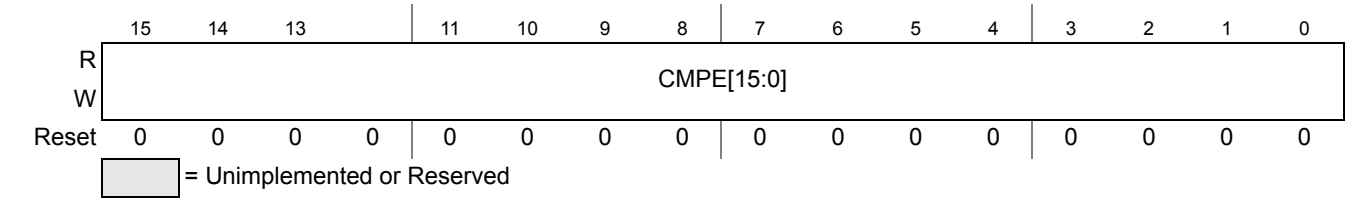


Figure 15-10. ATD Compare Enable Register (ATDCMPE)

Table 15-17. ATDCMPE Field Descriptions

Field	Description
15–0 CMPE[15:0]	**Compare Enable for Conversion Number *n* (*n*= 15, 14, 13, 12, 11, 10, 9, 8, 7, 6, 5, 4, 3, 2, 1, 0) of a Sequence (*n conversion number, NOT channel number!)*** — These bits enable automatic compare of conversion results individually for conversions of a sequence. The sense of each comparison is determined by the CMPHT[*n*] bit in the ATDCMPHT register. For each conversion number with CMPE[*n*]=1 do the following: 1) Write compare value to ATDDR*n* result register 2) Write compare operator with CMPHT[*n*] in ATDCPMHT register CCF[*n*] in ATDSTAT2 register will flag individual success of any comparison. 0 No automatic compare 1 Automatic compare of results for conversion *n* of a sequence is enabled.

19.4 Functional Description

19.4.1 PWM Clock Select

There are four available clocks: clock A, clock B, clock SA (scaled A), and clock SB (scaled B). These four clocks are based on the bus clock.

Clock A and B can be software selected to be 1, 1/2, 1/4, 1/8,..., 1/64, 1/128 times the bus clock. Clock SA uses clock A as an input and divides it further with a reloadable counter. Similarly, clock SB uses clock B as an input and divides it further with a reloadable counter. The rates available for clock SA are software selectable to be clock A divided by 2, 4, 6, 8,..., or 512 in increments of divide by 2. Similar rates are available for clock SB. Each PWM channel has the capability of selecting one of four clocks, clock A, Clock B, clock SA or clock SB.

The block diagram in Figure 19-15 shows the four different clocks and how the scaled clocks are created.

19.4.1.1 Prescale

The input clock to the PWM prescaler is the bus clock. It can be disabled whenever the part is in freeze mode by setting the PFRZ bit in the PWMCTL register. If this bit is set, whenever the MCU is in freeze mode (freeze mode signal active) the input clock to the prescaler is disabled. This is useful for emulation in order to freeze the PWM. The input clock can also be disabled when all available PWM channels are disabled (PWMEx-0 = 0). This is useful for reducing power by disabling the prescale counter.

Clock A and clock B are scaled values of the input clock. The value is software selectable for both clock A and clock B and has options of 1, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, or 1/128 times the bus clock. The value selected for clock A is determined by the PCKA2, PCKA1, PCKA0 bits in the PWMPRCLK register. The value selected for clock B is determined by the PCKB2, PCKB1, PCKB0 bits also in the PWMPRCLK register.

19.4.1.2 Clock Scale

The scaled A clock uses clock A as an input and divides it further with a user programmable value and then divides this by 2. The scaled B clock uses clock B as an input and divides it further with a user programmable value and then divides this by 2. The rates available for clock SA are software selectable to be clock A divided by 2, 4, 6, 8,..., or 512 in increments of divide by 2. Similar rates are available for clock SB.

Table 22-5. TTOV Field Descriptions

Note: Writing to unavailable bits has no effect. Reading from unavailable bits return a zero.

Field	Description
5:0 TOV[5:0]	**Toggle On Overflow Bits** — TOVx toggles output compare pin on overflow. This feature only takes effect when in output compare mode. When set, it takes precedence over forced output compare 0 Toggle output compare pin on overflow feature disabled. 1 Toggle output compare pin on overflow feature enabled.

22.3.2.6 Timer Control Register 1/Timer Control Register 2 (TCTL1/TCTL2)

Module Base + 0x0008

	7	6	5	4	3	2	1	0
R W	RESERVED	RESERVED	RESERVED	RESERVED	OM5	OL5	OM4	OL4
Reset	0	0	0	0	0	0	0	0

Figure 22-10. Timer Control Register 1 (TCTL1)

Module Base + 0x0009

	7	6	5	4	3	2	1	0
R W	OM3	OL3	OM2	OL2	OM1	OL1	OM0	OL0
Reset	0	0	0	0	0	0	0	0

Figure 22-11. Timer Control Register 2 (TCTL2)

Read: Anytime

Write: Anytime

Table 22-6. TCTL1/TCTL2 Field Descriptions

Note: Writing to unavailable bits has no effect. Reading from unavailable bits return a zero

Field	Description
5:0 OMx	**Output Mode** — These six pairs of control bits are encoded to specify the output action to be taken as a result of a successful OCx compare. When either OMx or OLx is 1, the pin associated with OCx becomes an output tied to OCx. **Note:** For an output line to be driven by an OCx the OCPDx must be cleared.
5:0 OLx	**Output Level** — These sixpairs of control bits are encoded to specify the output action to be taken as a result of a successful OCx compare. When either OMx or OLx is 1, the pin associated with OCx becomes an output tied to OCx. **Note:** For an output line to be driven by an OCx the OCPDx must be cleared.

Table 24-52. Set User Margin Level Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x0D	Flash block selection code [1:0]. See Table 24-32
001	Margin level setting.	

Upon clearing CCIF to launch the Set User Margin Level command, the Memory Controller will set the user margin level for the targeted block and then set the CCIF flag.

NOTE

When the EEPROM block is targeted, the EEPROM user margin levels are applied only to the EEPROM reads. However, when the P-Flash block is targeted, the P-Flash user margin levels are applied to both P-Flash and EEPROM reads. It is not possible to apply user margin levels to the P-Flash block only.

Valid margin level settings for the Set User Margin Level command are defined in Table 24-53.

Table 24-53. Valid Set User Margin Level Settings

CCOB (CCOBIX=001)	Level Description
0x0000	Return to Normal Level
0x0001	User Margin-1 Level[1]
0x0002	User Margin-0 Level[2]

1 Read margin to the erased state

2 Read margin to the programmed state

Table 24-54. Set User Margin Level Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 001 at command launch
		Set if command not available in current mode (see Table 24-25)
		Set if an invalid FlashBlockSelectionCode[1:0] is supplied (See Table 24-32)
		Set if an invalid margin level setting is supplied
	FPVIOL	None
	MGSTAT1	None
	MGSTAT0	None

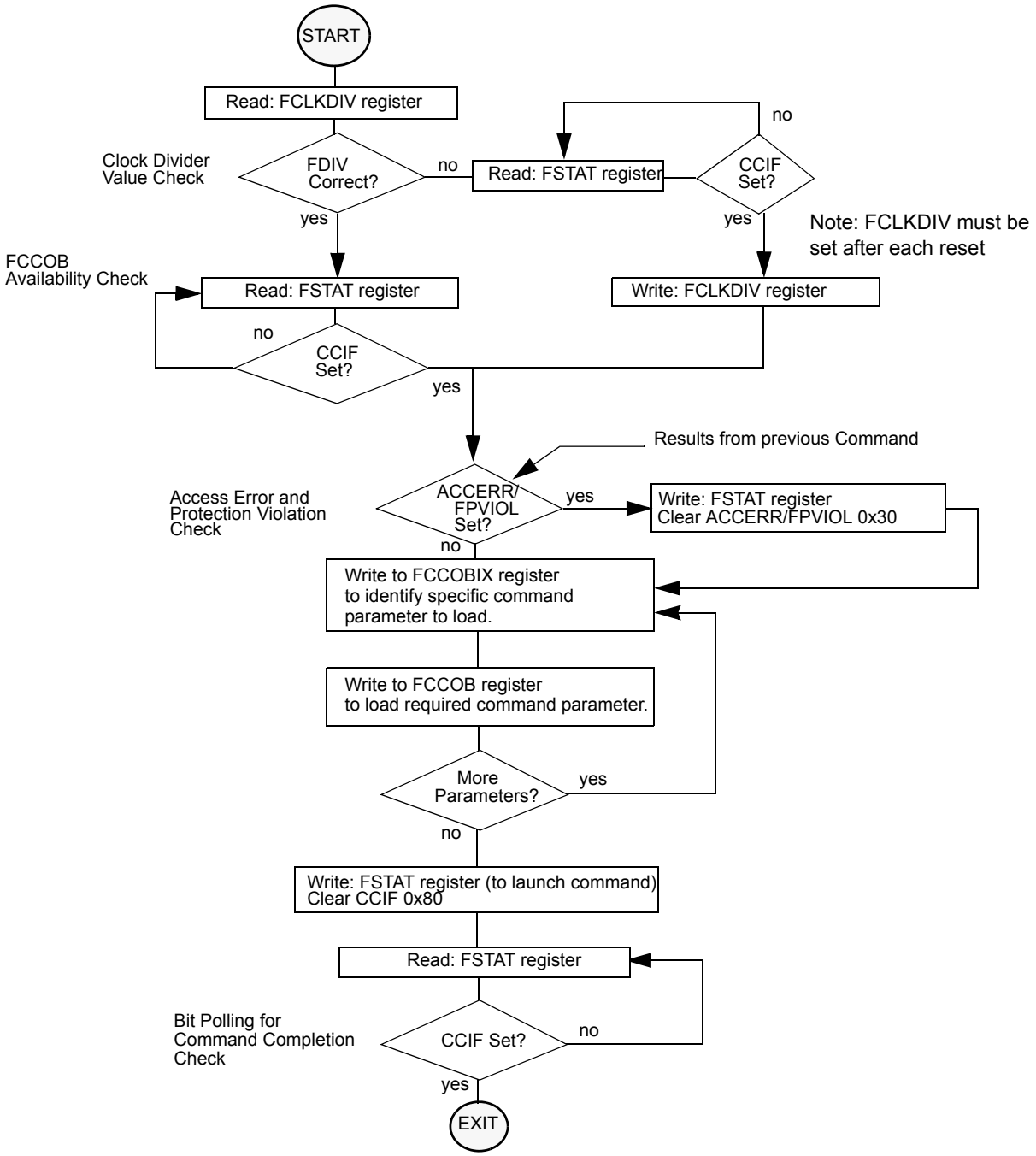


Figure 29-26. Generic Flash Command Write Sequence Flowchart

Table 29-43. Program Once Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 101 at command launch
		Set if command not available in current mode (see Table 29-27)
		Set if an invalid phrase index is supplied
		Set if the requested phrase has already been programmed[1]
	FPVIOL	None
	MGSTAT1	Set if any errors have been encountered during the verify operation
	MGSTAT0	Set if any non-correctable errors have been encountered during the verify operation

1 If a Program Once phrase is initially programmed to 0xFFFF_FFFF_FFFF_FFFF, the Program Once command will be allowed to execute again on that same phrase.

29.4.6.7 Erase All Blocks Command

The Erase All Blocks operation will erase the entire P-Flash and EEPROM memory space.

Table 29-44. Erase All Blocks Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x08	Not required

Upon clearing CCIF to launch the Erase All Blocks command, the Memory Controller will erase the entire Flash memory space and verify that it is erased. If the Memory Controller verifies that the entire Flash memory space was properly erased, security will be released. During the execution of this command (CCIF=0) the user must not write to any Flash module register. The CCIF flag will set after the Erase All Blocks operation has completed.

Table 29-45. Erase All Blocks Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 000 at command launch
		Set if command not available in current mode (see Table 29-27)
	FPVIOL	Set if any area of the P-Flash or EEPROM memory is protected
	MGSTAT1	Set if any errors have been encountered during the verify operation
	MGSTAT0	Set if any non-correctable errors have been encountered during the verify operation

29.4.6.8 Erase Flash Block Command

The Erase Flash Block operation will erase all addresses in a P-Flash or EEPROM block.

Table 31-17. FPROT Field Descriptions (continued)

Field	Description
2 FPLDIS	**Flash Protection Lower Address Range Disable** — The FPLDIS bit determines whether there is a protected/unprotected area in a specific region of the P-Flash memory beginning with global address 0x3_8000. 0 Protection/Unprotection enabled 1 Protection/Unprotection disabled
1–0 FPLS[1:0]	**Flash Protection Lower Address Size** — The FPLS bits determine the size of the protected/unprotected area in P-Flash memory as shown in Table 31-20. The FPLS bits can only be written to while the FPLDIS bit is set.

Table 31-18. P-Flash Protection Function

FPOPEN	FPHDIS	FPLDIS	Function[1]
1	1	1	No P-Flash Protection
1	1	0	Protected Low Range
1	0	1	Protected High Range
1	0	0	Protected High and Low Ranges
0	1	1	Full P-Flash Memory Protected
0	1	0	Unprotected Low Range
0	0	1	Unprotected High Range
0	0	0	Unprotected High and Low Ranges

1 For range sizes, refer to Table 31-19 and Table 31-20.

Table 31-19. P-Flash Protection Higher Address Range

FPHS[1:0]	Global Address Range	Protected Size
00	0x3_F800–0x3_FFFF	2 Kbytes
01	0x3_F000–0x3_FFFF	4 Kbytes
10	0x3_E000–0x3_FFFF	8 Kbytes
11	0x3_C000–0x3_FFFF	16 Kbytes

Table 31-20. P-Flash Protection Lower Address Range

FPLS[1:0]	Global Address Range	Protected Size
00	0x3_8000–0x3_83FF	1 Kbyte
01	0x3_8000–0x3_87FF	2 Kbytes
10	0x3_8000–0x3_8FFF	4 Kbytes
11	0x3_8000–0x3_9FFF	8 Kbytes

All possible P-Flash protection scenarios are shown in Figure 31-14 . Although the protection scheme is loaded from the Flash memory at global address 0x3_FF0C during the reset sequence, it can be changed by the user. The P-Flash protection scheme can be used by applications requiring reprogramming in single chip mode while providing as much protection as possible if reprogramming is not required.

Table 31-24. FCCOB - NVM Command Mode (Typical Usage)

CCOBIX[2:0]	Byte	FCCOB Parameter Fields (NVM Command Mode)
010	HI	Data 0 [15:8]
	LO	Data 0 [7:0]
011	HI	Data 1 [15:8]
	LO	Data 1 [7:0]
100	HI	Data 2 [15:8]
	LO	Data 2 [7:0]
101	HI	Data 3 [15:8]
	LO	Data 3 [7:0]

31.3.2.12 Flash Reserved1 Register (FRSV1)

This Flash register is reserved for factory testing.

Offset Module Base + 0x000C

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 31-18. Flash Reserved1 Register (FRSV1)

All bits in the FRSV1 register read 0 and are not writable.

31.3.2.13 Flash Reserved2 Register (FRSV2)

This Flash register is reserved for factory testing.

Offset Module Base + 0x000D

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 31-19. Flash Reserved2 Register (FRSV2)

All bits in the FRSV2 register read 0 and are not writable.

31.3.2.14 Flash Reserved3 Register (FRSV3)

This Flash register is reserved for factory testing.

- VERNUM: Version number. The first version is number 0b_0001 with both 0b_0000 and 0b_1111 meaning ‘none’.

31.4.3 Internal NVM resource (NVMRES)

IFR is an internal NVM resource readable by CPU , when NVMRES is active. The IFR fields are shown in Table 31-5.

The NVMRES global address map is shown in Table 31-6.

For FTMRG240K2 the NVMRES address area is shared with 16K space of P-Flash area, as shown in Figure 31-2.

31.4.4 Flash Command Operations

Flash command operations are used to modify Flash memory contents.

The next sections describe:

- How to write the FCLKDIV register that is used to generate a time base (FCLK) derived from BUSCLK for Flash program and erase command operations
- The command write sequence used to set Flash command parameters and launch execution
- Valid Flash commands available for execution, according to MCU functional mode and MCU security state.

31.4.4.1 Writing the FCLKDIV Register

Prior to issuing any Flash program or erase command after a reset, the user is required to write the FCLKDIV register to divide BUSCLK down to a target FCLK of 1 MHz. Table 31-8 shows recommended values for the FDIV field based on BUSCLK frequency.

NOTE

Programming or erasing the Flash memory cannot be performed if the bus clock runs at less than 0.8 MHz. Setting FDIV too high can destroy the Flash memory due to overstress. Setting FDIV too low can result in incomplete programming or erasure of the Flash memory cells.

When the FCLKDIV register is written, the FDIVLD bit is set automatically. If the FDIVLD bit is 0, the FCLKDIV register has not been written since the last reset. If the FCLKDIV register has not been written, any Flash program or erase command loaded during a command write sequence will not execute and the ACCERR bit in the FSTAT register will set.

31.4.4.2 Command Write Sequence

The Memory Controller will launch all valid Flash commands entered using a command write sequence.

Before launching a command, the ACCERR and FPVIOL bits in the FSTAT register must be clear (see Section 31.3.2.7) and the CCIF flag should be tested to determine the status of the current command write