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Details

Product Status	Active
Core Processor	12V1
Core Size	16-Bit
Speed	25MHz
Connectivity	CANbus, IrDA, LINbus, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	40
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3.13V ~ 5.5V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s9s12ga128f0mlfr

Table 1-14. 64-Pin LQFP Pinout for S12GN48

Package Pin	Function <---lowest---PRIORITY---highest--->					Power Supply	Internal Pull Resistor	
	Pin	2nd Func.	3rd Func.	4th Func	5th Func		CTRL	Reset State
1	PJ6	KWJ6	—	—	—	V _{DDX}	PERJ/PPSJ	Up
2	PJ5	KWJ5	—	—	—	V _{DDX}	PERJ/PPSJ	Up
3	PJ4	KWJ4	—	—	—	V _{DDX}	PERJ/PPSJ	Up
4	RESET	—	—	—	—	V _{DDX}	PULLUP	
5	VDDX	—	—	—	—	—	—	—
6	VDDR	—	—	—	—	—	—	—
7	VSSX	—	—	—	—	—	—	—
8	PE0 ¹	EXTAL	—	—	—	V _{DDX}	PUCR/PDPEE	Down
9	VSS	—	—	—	—	—	—	—
10	PE1 ¹	XTAL	—	—	—	V _{DDX}	PUCR/PDPEE	Down
11	TEST	—	—	—	—	N.A.	$\overline{\text{RESET}}$ pin	Down
12	PJ0	KWJ0	MISO1	—	—	V _{DDX}	PERJ/PPSJ	Up
13	PJ1	KWJ1	MOSI1	—	—	V _{DDX}	PERJ/PPSJ	Up
14	PJ2	KWJ2	SCK1	—	—	V _{DDX}	PERJ/PPSJ	Up
15	PJ3	KWJ3	$\overline{\text{SS1}}$	—	—	V _{DDX}	PERJ/PPSJ	Up
16	BKGD	MODC	—	—	—	V _{DDX}	PUCR/BKPUE	Up
17	PP0	KWP0	ETRIG0	API_EXTC LK	PWM0	V _{DDX}	PERP/PPSP	Disabled
18	PP1	KWP1	ETRIG1	ECLKX2	PWM1	V _{DDX}	PERP/PPSP	Disabled
19	PP2	KWP2	ETRIG2	PWM2	—	V _{DDX}	PERP/PPSP	Disabled
20	PP3	KWP3	ETRIG3	PWM3	—	V _{DDX}	PERP/PPSP	Disabled
21	PP4	KWP4	PWM4	—	—	V _{DDX}	PERP/PPSP	Disabled
22	PP5	KWP5	PWM5	—	—	V _{DDX}	PERP/PPSP	Disabled
23	PP6	KWP6	—	—	—	V _{DDX}	PERP/PPSP	Disabled
24	PP7	KWP7	—	—	—	V _{DDX}	PERP/PPSP	Disabled
25	PT7	—	—	—	—	V _{DDX}	PERT/PPST	Disabled
26	PT6	—	—	—	—	V _{DDX}	PERT/PPST	Disabled
27	PT5	IOC5	—	—	—	V _{DDX}	PERT/PPST	Disabled

NOTE

If an attempt is made to activate BDM before being enabled, the CPU resumes normal instruction execution after a brief delay. If BDM is not enabled, any hardware BACKGROUND commands issued are ignored by the BDM and the CPU is not delayed.

In active BDM, the BDM registers and standard BDM firmware lookup table are mapped to addresses 0x3_FF00 to 0x3_FFFF. BDM registers are mapped to addresses 0x3_FF00 to 0x3_FF0B. The BDM uses these registers which are readable anytime by the BDM. However, these registers are not readable by user programs.

When BDM is activated while CPU executes code overlapping with BDM firmware space the saved program counter (PC) will be auto incremented by one from the BDM firmware, no matter what caused the entry into BDM active mode (BGND instruction, BACKGROUND command or breakpoints). In such a case the PC must be set to the next valid address via a WRITE_PC command before executing the GO command.

7.4.3 BDM Hardware Commands

Hardware commands are used to read and write target system memory locations and to enter active background debug mode. Target system memory includes all memory that is accessible by the CPU such as on-chip RAM, Flash, I/O and control registers.

Hardware commands are executed with minimal or no CPU intervention and do not require the system to be in active BDM for execution, although, they can still be executed in this mode. When executing a hardware command, the BDM sub-block waits for a free bus cycle so that the background access does not disturb the running application program. If a free cycle is not found within 128 clock cycles, the CPU is momentarily frozen so that the BDM can steal a cycle. When the BDM finds a free cycle, the operation does not intrude on normal CPU operation provided that it can be completed in a single cycle. However, if an operation requires multiple cycles the CPU is frozen until the operation is complete, even though the BDM found a free cycle.

The BDM hardware commands are listed in [Table 7-5](#).

The READ_BD and WRITE_BD commands allow access to the BDM register locations. These locations are not normally in the system memory map but share addresses with the application in memory. To distinguish between physical memory locations that share the same address, BDM memory resources are enabled just for the READ_BD and WRITE_BD access cycle. This allows the BDM to access BDM locations unobtrusively, even if the addresses conflict with the application memory map.

Table 7-5. Hardware Commands

Command	Opcode (hex)	Data	Description
BACKGROUND	90	None	Enter background mode if BDM is enabled. If enabled, an ACK will be issued when the part enters active background mode.
ACK_ENABLE	D5	None	Enable Handshake. Issues an ACK pulse after the command is executed.
ACK_DISABLE	D6	None	Disable Handshake. This command does not issue an ACK pulse.

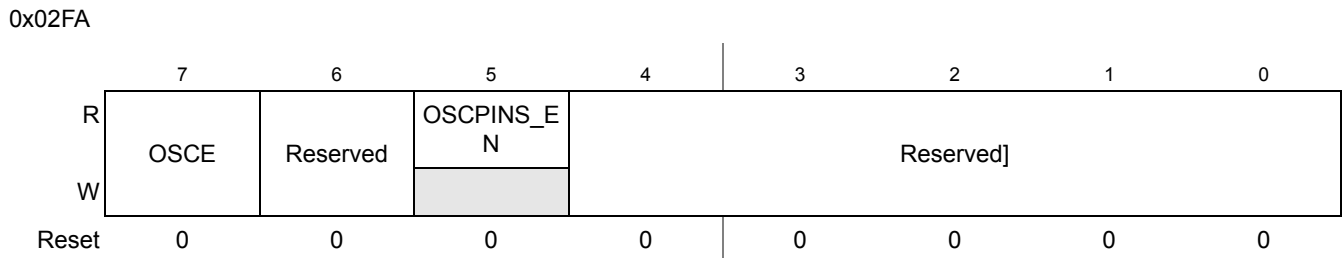


Figure 10-27. S12CPMU Oscillator Register (CPMUOSC)

Read: Anytime

Write: Anytime if PROT=0 (CPMUPROT register) and PLLSEL=1 (CPMUCLKS register). Else write has no effect.

NOTE.

Write to this register clears the LOCK and UPOSC status bits.

Table 10-24. CPMUOSC Field Descriptions

Field	Description
7 OSCE	<p>Oscillator Enable Bit — This bit enables the external oscillator (XOSCLCP). The UPOSC status bit in the CPMUFLG register indicates when the oscillation is stable and OSCCLK can be selected as Bus Clock or source of the COP or RTI. A loss of oscillation will lead to a clock monitor reset.</p> <p>0 External oscillator is disabled. REFCLK for PLL is IRCCLK.</p> <p>1 External oscillator is enabled. Clock monitor is enabled. External oscillator is qualified by PLLCLK REFCLK for PLL is the external oscillator clock divided by REFDIV.</p> <p>Note: When starting up the external oscillator (either by programming OSCE bit to 1 or on exit from Full Stop Mode with OSCE bit already 1) the software must wait for a minimum time equivalent to the startup-time of the external oscillator t_{UPOSC} before entering Pseudo Stop Mode.</p>
6 Reserved	Do not alter this bit from its reset value. It is for Manufacturer use only and can change the PLL behavior.
5 OSCPINS_EN	<p>Oscillator Pins EXTAL and XTAL Enable Bit</p> <p>If OSCE=1 this read-only bit is set. It can only be cleared with the next reset.</p> <p>Enabling the external oscillator reserves the EXTAL and XTAL pins exclusively for oscillator application.</p> <p>0 EXTAL and XTAL pins are not reserved for oscillator.</p> <p>1 EXTAL and XTAL pins exclusively reserved for oscillator.</p>
4-0 Reserved	Do not alter these bits from their reset value. It is for Manufacturer use only and can change the PLL behavior.

10.3.2.20 S12CPMU Protection Register (CPMUPROT)

This register protects the following clock configuration registers from accidental overwrite:

Table 12-15. Analog Input Channel Select Coding

SC	CD	CC	CB	CA	Analog Input Channel
1	0	0	0	0	Internal_6,
	0	0	0	1	Internal_7
	0	0	1	0	Internal_0
	0	0	1	1	Internal_1
	0	1	0	0	VRH
	0	1	0	1	VRL
	0	1	1	0	(VRH+VRL) / 2
	0	1	1	1	Reserved
	1	0	0	0	Internal_2
	1	0	0	1	Internal_3
	1	0	1	0	Internal_4
	1	0	1	1	Internal_5
	1	1	X	X	Reserved

Table 16-14. ATDCTL5 Field Descriptions (continued)

Field	Description
4 MULT	<p>Multi-Channel Sample Mode — When MULT is 0, the ATD sequence controller samples only from the specified analog input channel for an entire conversion sequence. The analog channel is selected by channel selection code (control bits CD/CC/CB/CA located in ATDCTL5). When MULT is 1, the ATD sequence controller samples across channels. The number of channels sampled is determined by the sequence length value (S8C, S4C, S2C, S1C). The first analog channel examined is determined by channel selection code (CD, CC, CB, CA control bits); subsequent channels sampled in the sequence are determined by incrementing the channel selection code or wrapping around to AN0 (channel 0).</p> <p>0 Sample only one channel 1 Sample across several channels</p>
3–0 CD, CC, CB, CA	<p>Analog Input Channel Select Code — These bits select the analog input channel(s). Table 16-15 lists the coding used to select the various analog input channels.</p> <p>In the case of single channel conversions (MULT=0), this selection code specifies the channel to be examined.</p> <p>In the case of multiple channel conversions (MULT=1), this selection code specifies the first channel to be examined in the conversion sequence. Subsequent channels are determined by incrementing the channel selection code or wrapping around to AN0 (after converting the channel defined by the Wrap Around Channel Select Bits WRAP3-0 in ATDCTL0). When starting with a channel number higher than the one defined by WRAP3-0 the first wrap around will be AN16 to AN0.</p>

Table 16-15. Analog Input Channel Select Coding

SC	CD	CC	CB	CA	Analog Input Channel
0	0	0	0	0	AN0
	0	0	0	1	AN1
	0	0	1	0	AN2
	0	0	1	1	AN3
	0	1	0	0	AN4
	0	1	0	1	AN5
	0	1	1	0	AN6
	0	1	1	1	AN7
	1	0	0	0	AN8
	1	0	0	1	AN9
	1	0	1	0	AN10
	1	0	1	1	AN11
	1	1	0	0	AN12
	1	1	0	1	AN13
	1	1	1	0	AN14
1	1	1	1	AN15	

17.3.4 AMPM Input Pin

This analog pin is used as input for the operational amplifier negative input pin, if the according mode is selected, see register bit DACM[2:0].

17.4 Memory Map and Register Definition

This sections provides the detailed information of all registers for the DAC_8B5V module.

17.4.1 Register Summary

Figure 17-2 shows the summary of all implemented registers inside the DAC_8B5V module.

NOTE

Register Address = Module Base Address + Address Offset, where the Module Base Address is defined at the MCU level and the Address Offset is defined at the module level.

Address Offset Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0000 DACCTL	R			0	0	0	DACM[2:0]		
	W	FVR	DRIVE						
0x0001 Reserved	R	0	0	0	0	0	0	0	0
	W								
0x0002 DACVOL	R	VOLTAGE[7:0]							
	W								
0x0003 - 0x0006 Reserved	R	0	0	0	0	0	0	0	0
	W								
0x0007 Reserved	R								
	W	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
0x0007 DACDEBUG	R								
	W	0	BUF_EN	DAC_EN	S3	S2n	S2p	S1n	S1p


 = Unimplemented

Figure 17-2. DAC_8B5V Register Summaryfv_dac_8b5v_RESERVED

18.3.2.17 MSCAN Identifier Acceptance Registers (CANIDAR0-7)

On reception, each message is written into the background receive buffer. The CPU is only signalled to read the message if it passes the criteria in the identifier acceptance and identifier mask registers (accepted); otherwise, the message is overwritten by the next message (dropped).

The acceptance registers of the MSCAN are applied on the IDR0–IDR3 registers (see [Section 18.3.3.1, “Identifier Registers \(IDR0–IDR3\)”](#)) of incoming messages in a bit by bit manner (see [Section 18.4.3, “Identifier Acceptance Filter”](#)).

For extended identifiers, all four acceptance and mask registers are applied. For standard identifiers, only the first two (CANIDAR0/1, CANIDMR0/1) are applied.

Module Base + 0x0010 to Module Base + 0x0013

Access: User read/write¹

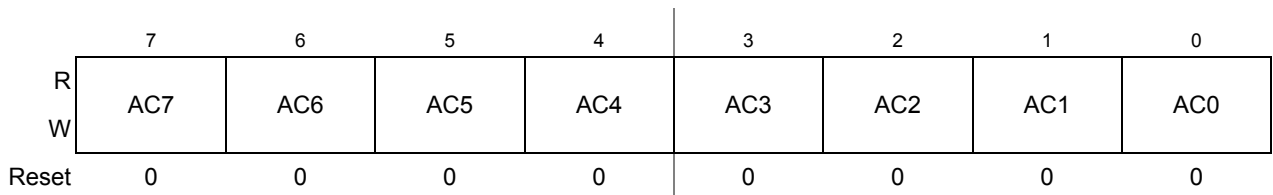


Figure 18-20. MSCAN Identifier Acceptance Registers (First Bank) — CANIDAR0–CANIDAR3

- ¹ Read: Anytime
Write: Anytime in initialization mode (INITRQ = 1 and INITAK = 1)

Table 18-22. CANIDAR0–CANIDAR3 Register Field Descriptions

Field	Description
7-0 AC[7:0]	Acceptance Code Bits — AC[7:0] comprise a user-defined sequence of bits with which the corresponding bits of the related identifier register (IDRn) of the receive message buffer are compared. The result of this comparison is then masked with the corresponding identifier mask register.

Module Base + 0x0018 to Module Base + 0x001B

Access: User read/write¹

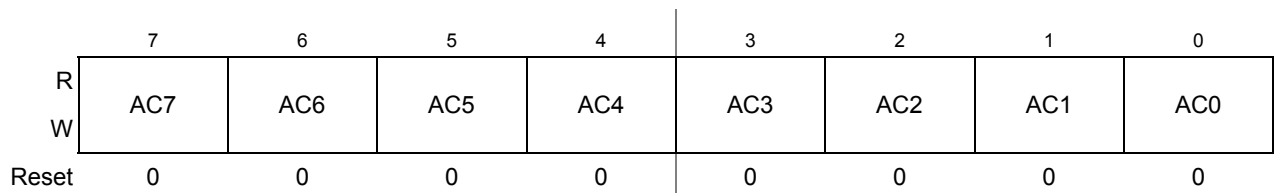


Figure 18-21. MSCAN Identifier Acceptance Registers (Second Bank) — CANIDAR4–CANIDAR7

- ¹ Read: Anytime
Write: Anytime in initialization mode (INITRQ = 1 and INITAK = 1)

Trying to alter data in any protected area in the P-Flash memory will result in a protection violation error and the FPVIOL bit will be set in the FSTAT register. The block erase of a P-Flash block is not possible if any of the P-Flash sectors contained in the same P-Flash block are protected.

Table 24-17. FPROT Field Descriptions

Field	Description
7 FPOPEN	Flash Protection Operation Enable — The FPOPEN bit determines the protection function for program or erase operations as shown in Table 24-18 for the P-Flash block. 0 When FPOPEN is clear, the FPHDIS bit defines an unprotected address range as specified by the FPHS bits 1 When FPOPEN is set, the FPHDIS bit enables protection for the address range specified by the FPHS bits
6 RNV[6]	Reserved Nonvolatile Bit — The RNV bit should remain in the erased state for future enhancements.
5 FPHDIS	Flash Protection Higher Address Range Disable — The FPHDIS bit determines whether there is a protected/unprotected area in a specific region of the P-Flash memory ending with global address 0x3_FFFF. 0 Protection/Unprotection enabled 1 Protection/Unprotection disabled
4–3 FPHS[1:0]	Flash Protection Higher Address Size — The FPHS bits determine the size of the protected/unprotected area in P-Flash memory as shown in Table 24-19 . The FPHS bits can only be written to while the FPHDIS bit is set.
2–0 RNV[2:0]	Reserved Nonvolatile Bits — These RNV bits should remain in the erased state.

Table 24-18. P-Flash Protection Function

FPOPEN	FPHDIS	Function ¹
1	1	No P-Flash Protection
1	0	Protected High Range
0	1	Full P-Flash Memory Protected
0	0	Unprotected High Range

¹ For range sizes, refer to [Table 24-19](#).

Table 24-19. P-Flash Protection Higher Address Range

FPHS[1:0]	Global Address Range	Protected Size
00	0x3_F800–0x3_FFFF	2 Kbytes
01	0x3_F000–0x3_FFFF	4 Kbytes
10	0x3_E000–0x3_FFFF	8 Kbytes
11	0x3_C000–0x3_FFFF	16 Kbytes

Although the protection scheme is loaded from the Flash memory at global address 0x3_FF0C during the reset sequence, it can be changed by the user. The P-Flash protection scheme can be used by applications requiring reprogramming in single chip mode while providing as much protection as possible if reprogramming is not required.

24.3.2.16 Flash Option Register (FOPT)

The FOPT register is the Flash option register.

Offset Module Base + 0x0010

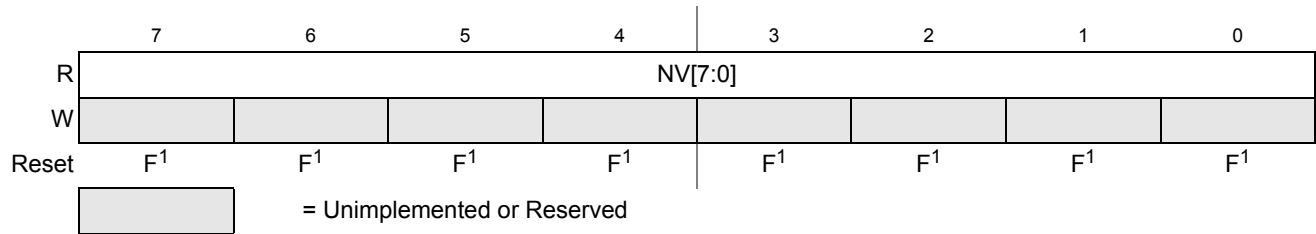


Figure 24-21. Flash Option Register (FOPT)

¹ Loaded from IFR Flash configuration field, during reset sequence.

All bits in the FOPT register are readable but are not writable.

During the reset sequence, the FOPT register is loaded from the Flash nonvolatile byte in the Flash configuration field at global address 0x3_FF0E located in P-Flash memory (see [Table 24-4](#)) as indicated by reset condition F in [Figure 24-21](#). If a double bit fault is detected while reading the P-Flash phrase containing the Flash nonvolatile byte during the reset sequence, all bits in the FOPT register will be set.

Table 24-23. FOPT Field Descriptions

Field	Description
7–0 NV[7:0]	Nonvolatile Bits — The NV[7:0] bits are available as nonvolatile bits. Refer to the device user guide for proper use of the NV bits.

24.3.2.17 Flash Reserved5 Register (FRSV5)

This Flash register is reserved for factory testing.

Offset Module Base + 0x0011

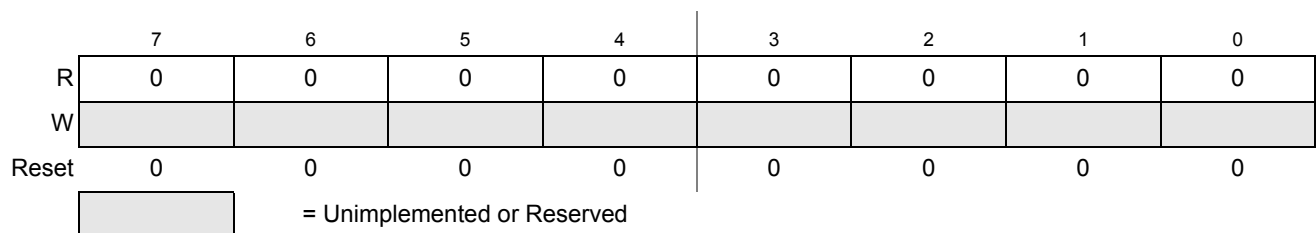


Figure 24-22. Flash Reserved5 Register (FRSV5)

All bits in the FR5V register read 0 and are not writable.

24.3.2.18 Flash Reserved6 Register (FRSV6)

This Flash register is reserved for factory testing.

25.3.2.5 Flash Configuration Register (FCNFG)

The FCNFG register enables the Flash command complete interrupt and forces ECC faults on Flash array read access from the CPU.

Offset Module Base + 0x0004



Figure 25-9. Flash Configuration Register (FCNFG)

CCIE, IGNSF, DFD, and FSFD bits are readable and writable while remaining bits read 0 and are not writable.

Table 25-13. FCNFG Field Descriptions

Field	Description
7 CCIE	Command Complete Interrupt Enable — The CCIE bit controls interrupt generation when a Flash command has completed. 0 Command complete interrupt disabled 1 An interrupt will be requested whenever the CCIF flag in the FSTAT register is set (see Section 25.3.2.7)
4 IGNSF	Ignore Single Bit Fault — The IGNSF controls single bit fault reporting in the FERSTAT register (see Section 25.3.2.8). 0 All single bit faults detected during array reads are reported 1 Single bit faults detected during array reads are not reported and the single bit fault interrupt will not be generated
1 DFD	Force Double Bit Fault Detect — The DFD bit allows the user to simulate a double bit fault during Flash array read operations and check the associated interrupt routine. The DFD bit is cleared by writing a 0 to DFD. 0 Flash array read operations will set the DFDIF flag in the FERSTAT register only if a double bit fault is detected 1 Any Flash array read operation will force the DFDIF flag in the FERSTAT register to be set (see Section 25.3.2.7) and an interrupt will be generated as long as the DFDIE interrupt enable in the FERCNFG register is set (see Section 25.3.2.6)
0 FSFD	Force Single Bit Fault Detect — The FSFD bit allows the user to simulate a single bit fault during Flash array read operations and check the associated interrupt routine. The FSFD bit is cleared by writing a 0 to FSFD. 0 Flash array read operations will set the SFDIF flag in the FERSTAT register only if a single bit fault is detected 1 Flash array read operation will force the SFDIF flag in the FERSTAT register to be set (see Section 25.3.2.7) and an interrupt will be generated as long as the SFDIE interrupt enable in the FERCNFG register is set (see Section 25.3.2.6)

25.3.2.6 Flash Error Configuration Register (FERCNFG)

The FERCNFG register enables the Flash error interrupts for the FERSTAT flags.

Offset Module Base + 0x0005

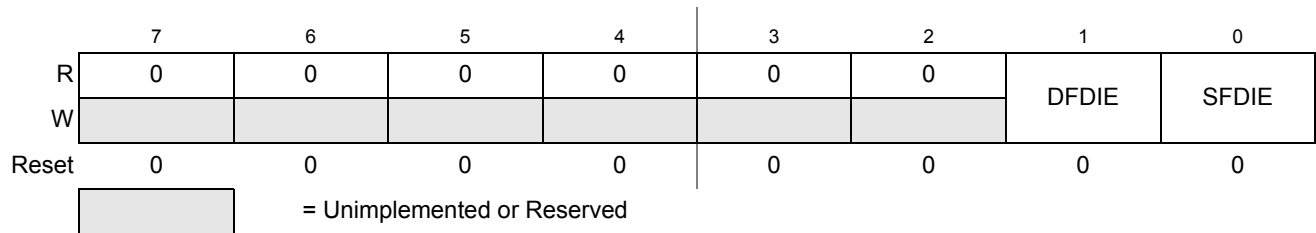


Figure 27-10. Flash Error Configuration Register (FERCNFG)

All assigned bits in the FERCNFG register are readable and writable.

Table 27-14. FERCNFG Field Descriptions

Field	Description
1 DFDIE	Double Bit Fault Detect Interrupt Enable — The DFDIE bit controls interrupt generation when a double bit fault is detected during a Flash block read operation. 0 DFDIF interrupt disabled 1 An interrupt will be requested whenever the DFDIF flag is set (see Section 27.3.2.8)
0 SFDIE	Single Bit Fault Detect Interrupt Enable — The SFDIE bit controls interrupt generation when a single bit fault is detected during a Flash block read operation. 0 SFDIF interrupt disabled whenever the SFDIF flag is set (see Section 27.3.2.8) 1 An interrupt will be requested whenever the SFDIF flag is set (see Section 27.3.2.8)

27.3.2.7 Flash Status Register (FSTAT)

The FSTAT register reports the operational status of the Flash module.

Offset Module Base + 0x0006

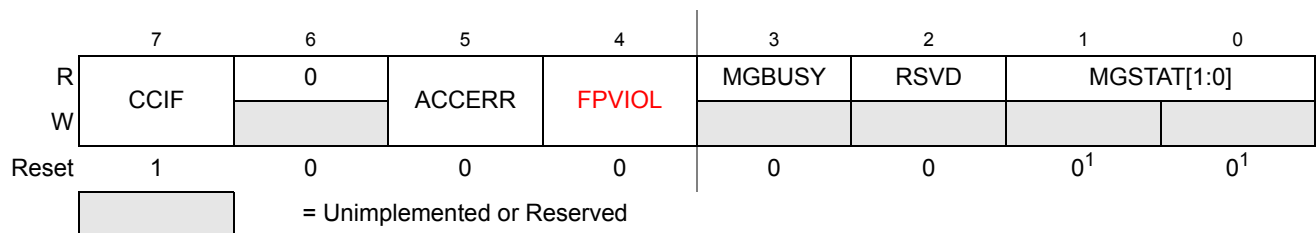


Figure 27-11. Flash Status Register (FSTAT)

¹ Reset value can deviate from the value shown if a double bit fault is detected during the reset sequence (see [Section 27.6](#)).

CCIF, ACCERR, and FPVIOL bits are readable and writable, MGBUSY and MGSTAT bits are readable but not writable, while remaining bits read 0 and are not writable.

Trying to alter data in any protected area in the P-Flash memory will result in a protection violation error and the FPVIOL bit will be set in the FSTAT register. The block erase of a P-Flash block is not possible if any of the P-Flash sectors contained in the same P-Flash block are protected.

Table 27-17. FPROT Field Descriptions

Field	Description
7 FPOPEN	Flash Protection Operation Enable — The FPOPEN bit determines the protection function for program or erase operations as shown in Table 27-18 for the P-Flash block. 0 When FPOPEN is clear, the FPHDIS and FPLDIS bits define unprotected address ranges as specified by the corresponding FPHS and FPLS bits 1 When FPOPEN is set, the FPHDIS and FPLDIS bits enable protection for the address range specified by the corresponding FPHS and FPLS bits
6 RNV[6]	Reserved Nonvolatile Bit — The RNV bit should remain in the erased state for future enhancements.
5 FPHDIS	Flash Protection Higher Address Range Disable — The FPHDIS bit determines whether there is a protected/unprotected area in a specific region of the P-Flash memory ending with global address 0x3_FFFF. 0 Protection/Unprotection enabled 1 Protection/Unprotection disabled
4–3 FPHS[1:0]	Flash Protection Higher Address Size — The FPHS bits determine the size of the protected/unprotected area in P-Flash memory as shown in Table 27-19 . The FPHS bits can only be written to while the FPHDIS bit is set.
2 FPLDIS	Flash Protection Lower Address Range Disable — The FPLDIS bit determines whether there is a protected/unprotected area in a specific region of the P-Flash memory beginning with global address 0x3_8000. 0 Protection/Unprotection enabled 1 Protection/Unprotection disabled
1–0 FPLS[1:0]	Flash Protection Lower Address Size — The FPLS bits determine the size of the protected/unprotected area in P-Flash memory as shown in Table 27-20 . The FPLS bits can only be written to while the FPLDIS bit is set.

Table 27-18. P-Flash Protection Function

FPOPEN	FPHDIS	FPLDIS	Function ¹
1	1	1	No P-Flash Protection
1	1	0	Protected Low Range
1	0	1	Protected High Range
1	0	0	Protected High and Low Ranges
0	1	1	Full P-Flash Memory Protected
0	1	0	Unprotected Low Range
0	0	1	Unprotected High Range
0	0	0	Unprotected High and Low Ranges

¹ For range sizes, refer to [Table 27-19](#) and [Table 27-20](#).

8. Reset the MCU

27.5.3 Mode and Security Effects on Flash Command Availability

The availability of Flash module commands depends on the MCU operating mode and security state as shown in [Table 27-27](#).

27.6 Initialization

On each system reset the flash module executes an initialization sequence which establishes initial values for the Flash Block Configuration Parameters, the FPROT and EEPROT protection registers, and the FOPT and FSEC registers. The initialization routine reverts to built-in default values that leave the module in a fully protected and secured state if errors are encountered during execution of the reset sequence. If a double bit fault is detected during the reset sequence, both MGSTAT bits in the FSTAT register will be set.

CCIF is cleared throughout the initialization sequence. The Flash module holds off all CPU access for a portion of the initialization sequence. Flash reads are allowed once the hold is removed. Completion of the initialization sequence is marked by setting CCIF high which enables user commands.

If a reset occurs while any Flash command is in progress, that command will be immediately aborted. The state of the word being programmed or the sector/block being erased is not guaranteed.

Table 28-54. Set User Margin Level Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x0D	Flash block selection code [1:0]. See Table 28-34
001	Margin level setting.	

Upon clearing CCIF to launch the Set User Margin Level command, the Memory Controller will set the user margin level for the targeted block and then set the CCIF flag.

NOTE

When the EEPROM block is targeted, the EEPROM user margin levels are applied only to the EEPROM reads. However, when the P-Flash block is targeted, the P-Flash user margin levels are applied to both P-Flash and EEPROM reads. It is not possible to apply user margin levels to the P-Flash block only.

Valid margin level settings for the Set User Margin Level command are defined in [Table 28-55](#).

Table 28-55. Valid Set User Margin Level Settings

CCOB (CCOBIX=001)	Level Description
0x0000	Return to Normal Level
0x0001	User Margin-1 Level ¹
0x0002	User Margin-0 Level ²

¹ Read margin to the erased state

² Read margin to the programmed state

Table 28-56. Set User Margin Level Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 001 at command launch
		Set if command not available in current mode (see Table 28-27)
		Set if an invalid FlashBlockSelectionCode[1:0] is supplied (See Table 28-34)
		Set if an invalid margin level setting is supplied
	FPVIOL	None
	MGSTAT1	None
	MGSTAT0	None

Table 29-14. FERCNFG Field Descriptions

Field	Description
1 DFDIE	Double Bit Fault Detect Interrupt Enable — The DFDIE bit controls interrupt generation when a double bit fault is detected during a Flash block read operation. 0 DFDIF interrupt disabled 1 An interrupt will be requested whenever the DFDIF flag is set (see Section 29.3.2.8)
0 SFDIE	Single Bit Fault Detect Interrupt Enable — The SFDIE bit controls interrupt generation when a single bit fault is detected during a Flash block read operation. 0 SFDIF interrupt disabled whenever the SFDIF flag is set (see Section 29.3.2.8) 1 An interrupt will be requested whenever the SFDIF flag is set (see Section 29.3.2.8)

29.3.2.7 Flash Status Register (FSTAT)

The FSTAT register reports the operational status of the Flash module.

Offset Module Base + 0x0006

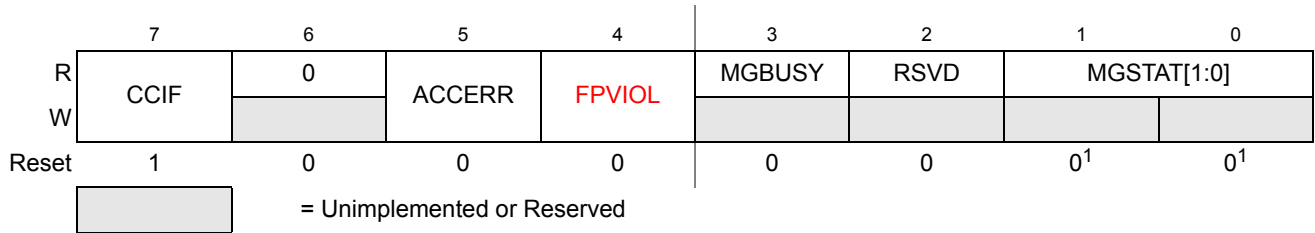


Figure 29-11. Flash Status Register (FSTAT)

¹ Reset value can deviate from the value shown if a double bit fault is detected during the reset sequence (see [Section 29.6](#)).

CCIF, ACCERR, and FPVIOL bits are readable and writable, MGBUSY and MGSTAT bits are readable but not writable, while remaining bits read 0 and are not writable.

Table 29-15. FSTAT Field Descriptions

Field	Description
7 CCIF	Command Complete Interrupt Flag — The CCIF flag indicates that a Flash command has completed. The CCIF flag is cleared by writing a 1 to CCIF to launch a command and CCIF will stay low until command completion or command violation. 0 Flash command in progress 1 Flash command has completed
5 ACCERR	Flash Access Error Flag — The ACCERR bit indicates an illegal access has occurred to the Flash memory caused by either a violation of the command write sequence (see Section 29.4.4.2) or issuing an illegal Flash command. While ACCERR is set, the CCIF flag cannot be cleared to launch a command. The ACCERR bit is cleared by writing a 1 to ACCERR. Writing a 0 to the ACCERR bit has no effect on ACCERR. 0 No access error detected 1 Access error detected
4 FPVIOL	Flash Protection Violation Flag — The FPVIOL bit indicates an attempt was made to program or erase an address in a protected area of P-Flash or EEPROM memory during a command write sequence. The FPVIOL bit is cleared by writing a 1 to FPVIOL. Writing a 0 to the FPVIOL bit has no effect on FPVIOL. While FPVIOL is set, it is not possible to launch a command or start a command write sequence. 0 No protection violation detected 1 Protection violation detected

[Table 30-4](#)). The Verify Backdoor Access Key command must not be executed from the Flash block containing the backdoor comparison key to avoid code runaway.

Table 30-52. Verify Backdoor Access Key Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x0C	Not required
001	Key 0	
010	Key 1	
011	Key 2	
100	Key 3	

Upon clearing CCIF to launch the Verify Backdoor Access Key command, the Memory Controller will check the FSEC KEYEN bits to verify that this command is enabled. If not enabled, the Memory Controller sets the ACCERR bit in the FSTAT register and terminates. If the command is enabled, the Memory Controller compares the key provided in FCCOB to the backdoor comparison key in the Flash configuration field with Key 0 compared to 0x3_FF00, etc. If the backdoor keys match, security will be released. If the backdoor keys do not match, security is not released and all future attempts to execute the Verify Backdoor Access Key command are aborted (set ACCERR) until a reset occurs. The CCIF flag is set after the Verify Backdoor Access Key operation has completed.

Table 30-53. Verify Backdoor Access Key Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 100 at command launch
		Set if an incorrect backdoor key is supplied
		Set if backdoor key access has not been enabled (KEYEN[1:0] != 10, see Section 30.3.2.2)
		Set if the backdoor key has mismatched since the last reset
	FPVIOL	None
	MGSTAT1	None
	MGSTAT0	None

30.4.6.12 Set User Margin Level Command

The Set User Margin Level command causes the Memory Controller to set the margin level for future read operations of the P-Flash or EEPROM block.

Table 30-54. Set User Margin Level Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x0D	Flash block selection code [1:0]. See Table 30-34
001	Margin level setting.	

Table 30-64. Erase EEPROM Sector Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x12	Global address [17:16] to identify EEPROM block
001	Global address [15:0] anywhere within the sector to be erased. See Section 30.1.2.2 for EEPROM sector size.	

Upon clearing CCIF to launch the Erase EEPROM Sector command, the Memory Controller will erase the selected Flash sector and verify that it is erased. The CCIF flag will set after the Erase EEPROM Sector operation has completed.

Table 30-65. Erase EEPROM Sector Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 001 at command launch
		Set if command not available in current mode (see Table 30-27)
		Set if an invalid global address [17:0] is supplied (see Table 30-3)
		Set if a misaligned word address is supplied (global address [0] != 0)
	FPVIOL	Set if the selected area of the EEPROM memory is protected
	MGSTAT1	Set if any errors have been encountered during the verify operation
	MGSTAT0	Set if any non-correctable errors have been encountered during the verify operation

30.4.7 Interrupts

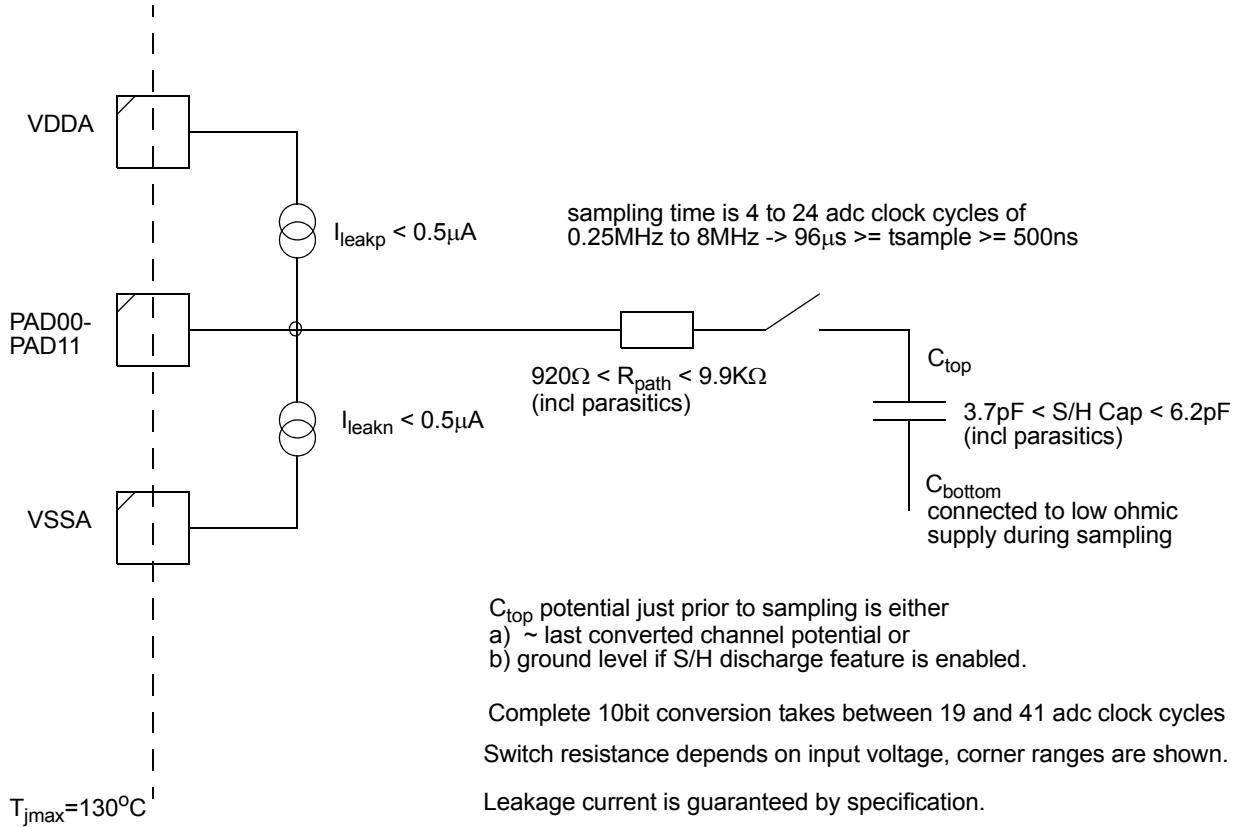
The Flash module can generate an interrupt when a Flash command operation has completed or when a Flash command operation has detected an ECC fault.

Table 30-66. Flash Interrupt Sources

Interrupt Source	Interrupt Flag	Local Enable	Global (CCR) Mask
Flash Command Complete	CCIF (FSTAT register)	CCIE (FCNFG register)	I Bit
ECC Double Bit Fault on Flash Read	DFDIF (FERSTAT register)	DFDIE (FERCNFG register)	I Bit
ECC Single Bit Fault on Flash Read	SFDIF (FERSTAT register)	SFDIE (FERCNFG register)	I Bit

A.4.3.2 ADC Analog Input Parasitics

Figure A-2. ADC Analog Input Parasitics



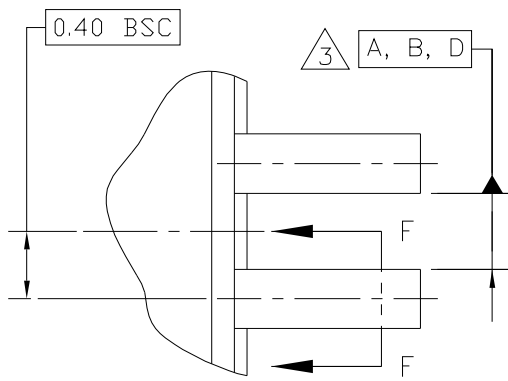
A.4.4 ADC Temperature Sensor

Table A-30. ADC Temperature Sensor

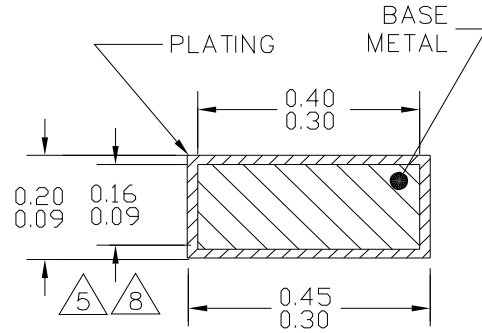
Num	C	Rating	Symbol	Min	Typ	Max	Unit
1	T	Temperature Sensor Slope	dV_{TS}	-4.0	-3.8	-3.6	mV/°C

A.5 ACMP Characteristics

This section describes the electrical characteristics of the analog comparator.

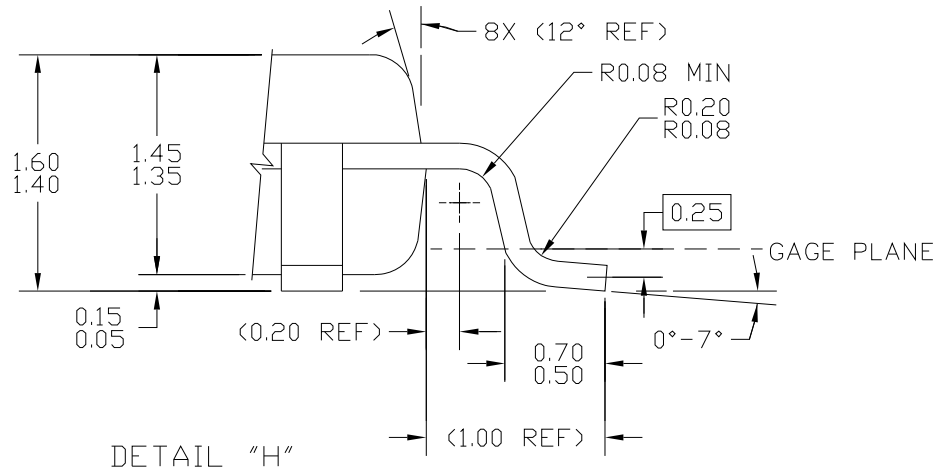


DETAIL G



M 0.2 M C A-B D

SECTION F-F
ROTATED 90°CW
32 PLACES



DETAIL "H"

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	CASE NUMBER: 873A-03	19 MAY 2005	
	STANDARD: JEDEC MS-026 BBA		