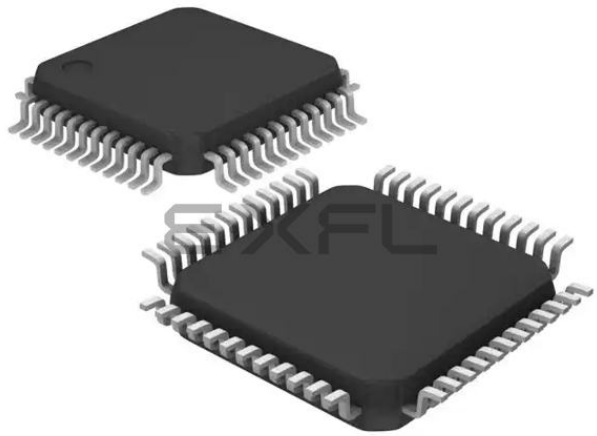

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Details	
Product Status	Active
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Connectivity	CANbus, IrDA, LINbus, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	40
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Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	11K x 8
Voltage - Supply (Vcc/Vdd)	3.13V ~ 5.5V
Data Converters	A/D 16x12b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s9s12ga240f0vlf

Chapter 21
Serial Peripheral Interface (S12SPIV5)

Table 1-5. Assigned Part ID Numbers

Device	Mask Set Number	Part ID
MC9S12GNA16	0N48A	0xF380
	0N57V	0xF380
MC9S12GN16	0N48A[3]	0xF380[3]
	0N57V[3]	0xF380[3]
	1N48A[4]	0xF381[4]
	1N57V[4]	0xF381[4]

1 Only available in 48-pin LQFP and 64-pin LQFP
2 Only available in 32-pin LQFP
3 Only available in 48-pin LQFP and 48-pin QFN
4 Only available in 20-pin TSSOP and 32-pin LQFP

1.7 Signal Description and Device Pinouts

This section describes signals that connect off-chip. It includes a pinout diagram, a table of signal properties, and detailed discussion of signals. It is built from the signal description sections of the individual IP blocks on the device.

1.7.1 Pin Assignment Overview

Table 1-6 provides a summary of which ports are available for each package option.

Table 1-6. Port Availability by Package Option

Port	20 TSSOP	32 LQFP	48 LQFP 48 QFN	64 LQFP	100 LQFP	KGD (Die)
Port AD/ADC Channels	6	8	12	16	16	16
Port A pins	0	0	0	0	8	8
Port B pins	0	0	0	0	8	8
Port C pins	0	0	0	0	8	8
Port D pins	0	0	0	0	8	8
Port E pins	2	2	2	2	2	2
Port J	0	0	4	8	8	8
Port M	0	2	2	4	4	4
Port P	0	4	6	8	8	8
Port S	4	6	8	8	8	8
Port T	2	4	6	8	8	8

Table 1-9. 32-Pin LQFP OPinout for S12GN16 and S12GN32

	Function <----lowest-----PRIORITY-----highest---->					Power Supply	Internal Pull Resistor	
Package Pin	Pin	2nd Func.	3rd Func.	4th Func	5th Func		CTRL	Reset State
32	PM1	—	—	—	—	V_{DDX}	PERM/PPSM	Disabled

1 The regular I/O characteristics (see Section A.2, “I/O Characteristics”) apply if the EXTAL/XTAL function is disabled

1.8.1.3 Pinout 48-Pin LQFP/QFN

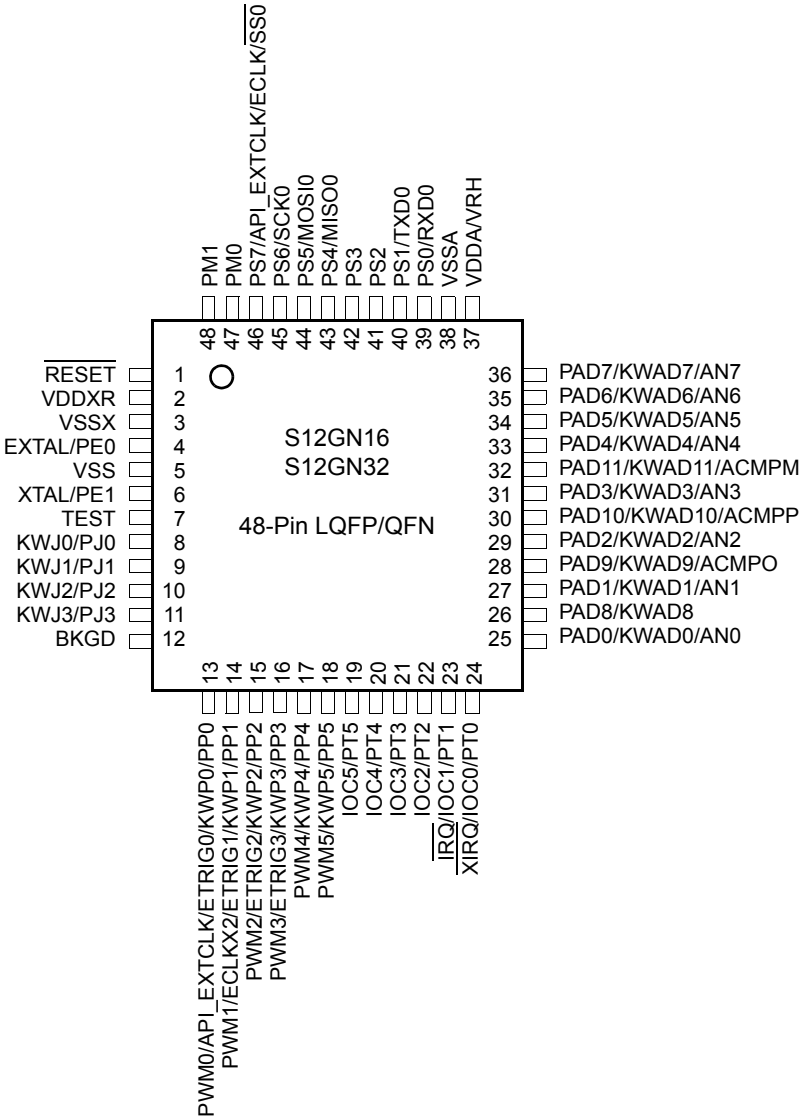


Figure 1-5. 48-Pin LQFP/QFN Pinout for S12GN16 and S12GN32

Table 1-17. 64-Pin LQFP Pinout for S12G48 and S12G64

	Function <----lowest-----PRIORITY-----highest---->					Power Supply	Internal Pull Resistor	
Package Pin	Pin	2nd Func.	3rd Func.	4th Func	5th Func		CTRL	Reset State
28	PT4	IOC4	—	—	—	V_{DDX}	PERT/PPST	Disabled
29	PT3	IOC3	—	—	—	V_{DDX}	PERT/PPST	Disabled
30	PT2	IOC2	—	—	—	V_{DDX}	PERT/PPST	Disabled
31	PT1	IOC1	$\overline{IRQ}$	—	—	V_{DDX}	PERT/PPST	Disabled
32	PT0	IOC0	$\overline{XIRQ}$	—	—	V_{DDX}	PERT/PPST	Disabled
33	PAD0	KWAD0	AN0	—	—	V_{DDA}	PER1AD/PPS1AD	Disabled
34	PAD8	KWAD8	AN8	—	—	V_{DDA}	PER0AD/PPS0AD	Disabled
35	PAD1	KWAD1	AN1	—	—	V_{DDA}	PER1AD/PPS1AD	Disabled
36	PAD9	KWAD9	AN9	ACMPO	—	V_{DDA}	PER0ADPPS0AD	Disabled
37	PAD2	KWAD2	AN2	—	—	V_{DDA}	PER1AD/PPS1AD	Disabled
38	PAD10	KWAD10	AN10	ACMPP		V_{DDA}	PER0AD/PPS0AD	Disabled
39	PAD3	KWAD3	AN3	—	—	V_{DDA}	PER1AD/PPS1AD	Disabled
40	PAD11	KWAD11	AN11	ACMPM		V_{DDA}	PER0AD/PPS0AD	Disabled
41	PAD4	KWAD4	AN4	—	—	V_{DDA}	PER1AD/PPS1AD	Disabled
42	PAD12	KWAD12	—	—	—	V_{DDA}	PER0AD/PPS0AD	Disabled
43	PAD5	KWAD5	AN5	—	—	V_{DDA}	PER1AD/PPS1AD	Disabled
44	PAD13	KWAD13	—	—	—	V_{DDA}	PER0AD/PPS0AD	Disabled
45	PAD6	KWAD6	AN6	—	—	V_{DDA}	PER1AD/PPS1AD	Disabled
46	PAD14	KWAD14	—	—	—	V_{DDA}	PER0AD/PPS0AD	Disabled
47	PAD7	KWAD7	AN7	—	—	V_{DDA}	PER1AD/PPS1AD	Disabled
48	PAD15	KWAD15	—	—	—	V_{DDA}	PER0AD/PPS0AD	Disabled
49	VRH	—	—	—	—	—	—	—
50	VDDA	—	—	—	—	—	—	—
51	VSSA	—	—	—	—	—	—	—
52	PS0	RXD0	—	—	—	V_{DDX}	PERS/PPSS	Up
53	PS1	TXD0	—	—	—	V_{DDX}	PERS/PPSS	Up
54	PS2	RXD1	—	—	—	V_{DDX}	PERS/PPSS	Up
55	PS3	TXD1	—	—	—	V_{DDX}	PERS/PPSS	Up
56	PS4	MISO0	—	—	—	V_{DDX}	PERS/PPSS	Up

Table 1-22. 100-Pin LQFP Pinout for S12G96 and S12G128

	Function <----lowest-----PRIORITY-----highest---->				Power Supply	Internal Pull Resistor	
Package Pin	Pin	2nd Func.	3rd Func.	4th Func.		CTRL	Reset State
1	PJ6	KWJ6	SCK2	—	V_{DDX}	PERJ/PPSJ	Up
2	PJ5	KWJ5	MOSI2	—	V_{DDX}	PERJ/PPSJ	Up
3	PJ4	KWJ4	MISO2	—	V_{DDX}	PERJ/PPSJ	Up
4	PA0	—	—	—	V_{DDX}	PUCR/PUPAE	Disabled
5	PA1	—	—	—	V_{DDX}	PUCR/PUPAE	Disabled
6	PA2	—	—	—	V_{DDX}	PUCR/PUPAE	Disabled
7	PA3	—	—	—	V_{DDX}	PUCR/PUPAE	Disabled
8	RESET	—	—	—	V_{DDX}	PULLUP	
9	VDDX1	—	—	—	—	—	—
10	VDDR	—	—	—	—	—	—
11	VSSX1	—	—	—	—	—	—
12	PE0[1]	EXTAL	—	—	V_{DDX}	PUCR/PDPEE	Down
13	VSS	—	—	—	—	—	—
14	PE1[1]	XTAL	—	—	V_{DDX}	PUCR/PDPEE	Down
15	TEST	—	—	—	N.A.	$\overline{\text{RESET}}$ pin	Down
16	PA4	—	—	—	V_{DDX}	PUCR/PUPAE	Disabled
17	PA5	—	—	—	V_{DDX}	PUCR/PUPAE	Disabled
18	PA6	—	—	—	V_{DDX}	PUCR/PUPAE	Disabled
19	PA7	—	—	—	V_{DDX}	PUCR/PUPAE	Disabled
20	PJ0	KWJ0	MISO1	—	V_{DDX}	PERJ/PPSJ	Up
21	PJ1	KWJ1	MOSI1	—	V_{DDX}	PERJ/PPSJ	Up
22	PJ2	KWJ2	SCK1	—	V_{DDX}	PERJ/PPSJ	Up
23	PJ3	KWJ3	$\overline{\text{SS1}}$	—	V_{DDX}	PERJ/PPSJ	Up
24	BKGD	MODC	—	—	V_{DDX}	PUCR/BKPUE	Up
25	PB0	ECLK	—	—	V_{DDX}	PUCR/PUPBE	Disabled
26	PB1	API_EXTCLK	—	—	V_{DDX}	PUCR/PUPBE	Disabled
27	PB2	ECLKX2	—	—	V_{DDX}	PUCR/PUPBE	Disabled

A standard port pin has the following minimum features:

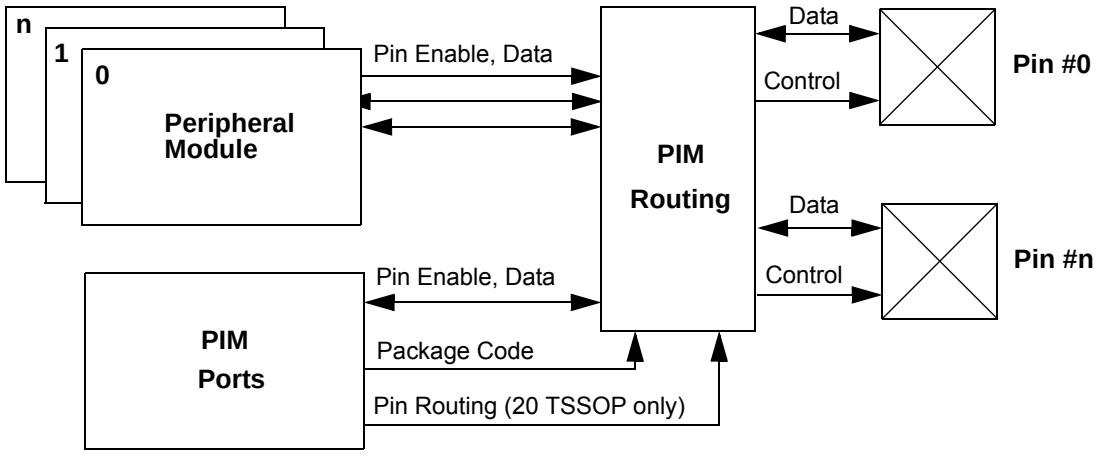
- Input/output selection
- 3.15 V - 5 V digital and analog input
- Input with selectable pullup or pulldown device

Optional features supported on dedicated pins:

- Open drain for wired-or connections
- Key-wakeup feature: External pin interrupt with glitch filtering, which can also be used for wakeup from stop mode.

2.1.4 Block Diagram

Figure 2-1. Block Diagram



2.2 PIM Routing - External Signal Description

This section lists and describes the signals that do connect off-chip.

Table 2-3 shows the availability of I/O port pins for each group in the largest offered package option.

Table 2-3. Port Pin Availability (in largest package) per Device

Port	Device Group		
	G1 (100 pin)	G2 (64 pin)	G3 (48 pin)
A	7-0	-	-
B	7-0	-	-
C	7-0	-	-
D	7-0	-	-
E	1-0	1-0	1-0

Table 2-4. Signals and Priorities

Legend	
?	Signal available on pin
?	Routing option on pin
?	Routing reset location
	Not available on pin

Port	Pin	Signal	Signals per Device and Package (signal priority on pin from top to bottom)																				I/O	Description
			GA240 / GA192	G240 / G192	G128 / GA128 / G96 / GA96	GA240 / GA192	G240 / G192	G128 / GA128 / G96 / GA96	G64 / GA64 / G48 / GA48	GN48	GA240 / GA192	G240 / G192	G128 / GA128 / G96 / GA96	G64 / GA64 / G48 / GA48	GN48	GN32 / GNA32	GN16 / GNA16	G64 / G48	GN48	GN32	GN16	GN32	GN16		
			100			64					48							32				20			
AD	PAD7	ACMPM																?	?	?	?			I	ACMP inverting input (-)
		AN7	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?			I	ADC analog
		[PT1AD7]/ KWAD7	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?			I/O	GPIO with interrupt
	PAD6	ACMPP																?	?	?	?			I	ACMP non-inv. input (+)
		AN6	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?			I	ADC analog
		[PT1AD6]/ KWAD6	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?			I/O	GPIO with interrupt
	PAD5	ACMPO																?	?	?	?			O	ACMP unsync. dig. out
		ACMPM																				?	?	I	ACMP inverting input (-)
		AN5	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	I	ADC analog
		TXD0																				?	?	I/O	SCI transmit
		IOC3																				?	?	I/O	Timer channel
		PWM3																				?	?	O	PWM channel
		ETRIG3																				?	?	I	ADC external trigger
		[PT1AD5]/ KWAD5	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	I/O	GPIO with interrupt
	PAD4	ACMPP																				?	?	I	ACMP non-inv. input (+)
		AN4	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	I	ADC analog
		RXD0																				?	?	I	SCI receive
		IOC2																				?	?	I/O	Timer channel
		PWM2																				?	?	O	PWM channel
		ETRIG2																				?	?	I	ADC external trigger
		[PT1AD4]/ KWAD4	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	I/O	GPIO with interrupt
	PAD3	ACMPO																				?	?	O	ACMP unsync. dig. out
		AN3	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	I	ADC analog
		[PT1AD3]/ KWAD3	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	I/O	GPIO with interrupt
	PAD2-PAD0	AN2-AN0	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	I	ADC analog
		[PT1AD2: PT1AD0]/ KWAD2-KWAD0	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	I/O	GPIO with interrupt

Table 2-40. PTS Register Field Descriptions

Field	Description
7-0 PTS	**Port S general-purpose input/output data**—Data Register When not used with an alternative signal, the associated pin can be used as general-purpose I/O. In general-purpose output mode the port data register bit value is driven to the pin. If the associated data direction bit is set to 1, a read returns the value of the port data register bit, otherwise the buffered pin input state is read.

2.4.3.21 Port S Input Register (PTIS)

Address 0x0249 Access: User read only[1]

	7	6	5	4	3	2	1	0
R	PTIS7	PTIS6	PTIS5	PTIS4	PTIS3	PTIS2	PTIS1	PTIS0
W								
Reset	0	0	0	0	0	0	0	0

Figure 2-22. Port S Input Register (PTIS)

[1] Read: Anytime
Write:Never

Table 2-41. PTIS Register Field Descriptions

Field	Description
7-0 PTIS	**Port S input data—** A read always returns the buffered input state of the associated pin. It can be used to detect overload or short circuit conditions on output pins.

2.4.3.22 Port S Data Direction Register (DDRS)

Address 0x024A Access: User read/write[1]

	7	6	5	4	3	2	1	0
R W	DDRS7	DDRS6	DDRS5	DDRS4	DDRS3	DDRS2	DDRS1	DDRS0
Reset	0	0	0	0	0	0	0	0

Figure 2-23. Port S Data Direction Register (DDRS)

[1] Read: Anytime
Write: Anytime

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x003B	CPMURTI	R	RTDEC	RTR6	RTR5	RTR4	RTR3	RTR2	RTR1	RTR0
		W								
0x003C	CPMUCOP	R	WCOP	RSBCK	0	0	0	CR2	CR1	CR0
		W			WRTMASK					
0x003D	RESERVEDCPMUTEST0	R	0	0	0	0	0	0	0	0
		W								
0x003E	RESERVEDCPMUTEST1	R	0	0	0	0	0	0	0	0
		W								
0x003F	CPMU ARMCOP	R	0	0	0	0	0	0	0	0
		W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x02F0	RESERVED	R	0	0	0	0	0	0	0	0
		W								
0x02F1	CPMU LVCTL	R	0	0	0	0	0	LVDS	LVIE	LVIF
		W								
0x02F2	CPMU APICTL	R	APICLK	0	0	APIES	APIEA	APIFE	APIE	APIF
		W								
0x02F3	CPMUACLKTR	R	ACLKTR5	ACLKTR4	ACLKTR3	ACLKTR2	ACLKTR1	ACLKTR0	0	0
		W								
0x02F4	CPMUAPIRH	R	APIR15	APIR14	APIR13	APIR12	APIR11	APIR10	APIR9	APIR8
		W								
0x02F5	CPMUAPIRL	R	APIR7	APIR6	APIR5	APIR4	APIR3	APIR2	APIR1	APIR0
		W								
0x02F6	RESERVEDCPMUTEST3	R	0	0	0	0	0	0	0	0
		W								
0x02F7	RESERVED	R	0	0	0	0	0	0	0	0
		W								
0x02F8	CPMU IRCTRIMH	R	TCTRIM[4:0]					0	IRCTRIM[9:8]	
		W								
0x02F9	CPMU IRCTRIML	R	IRCTRIM[7:0]							
		W								
0x02FA	CPMUOSC	R	OSCE	Reserved	OSCPINS_EN	Reserved				
		W								
0x02FB	CPMUPROT	R	0	0	0	0	0	0	0	PROT
		W								
0x02FC	RESERVEDCPMUTEST2	R	0	0	0	0	0	0	0	0
		W								

= Unimplemented or Reserved

Figure 10-3. CPMU Register Summary

15.3.2.12.2 Right Justified Result Data (DJM=1)

Module Base +
0x0010 = ATDDR0, 0x0012 = ATDDR1, 0x0014 = ATDDR2, 0x0016 = ATDDR3
0x0018 = ATDDR4, 0x001A = ATDDR5, 0x001C = ATDDR6, 0x001E = ATDDR7
0x0020 = ATDDR8, 0x0022 = ATDDR9, 0x0024 = ATDDR10, 0x0026 = ATDDR11
0x0028 = ATDDR12, 0x002A = ATDDR13, 0x002C = ATDDR14, 0x002E = ATDDR15

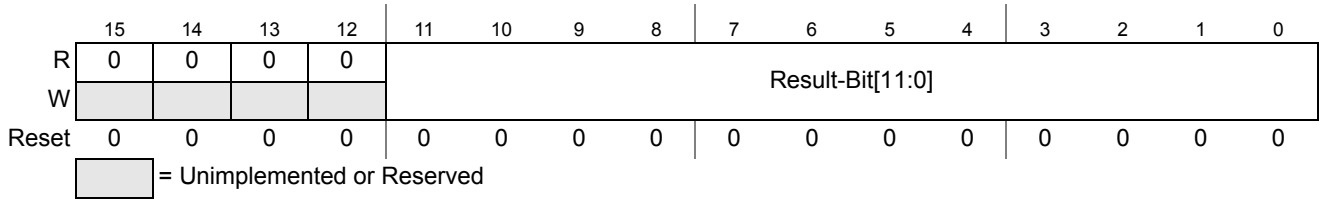


Figure 15-15. Right justified ATD conversion result register (ATDDR*n*)

Table 15-22 shows how depending on the A/D resolution the conversion result is transferred to the ATD result registers for right justified data. Compare is always done using all 12 bits of both the conversion result and the compare value in ATDDRn.

Table 15-22. Conversion result mapping to ATDDRn

A/D resolution	DJM	conversion result mapping to ATDDR*n*
8-bit data	1	Result-Bit[7:0] = result, Result-Bit[11:8]=0000
10-bit data	1	Result-Bit[9:0] = result, Result-Bit[11:10]=00

Each channel counter can be read at anytime without affecting the count or the operation of the PWM channel.

Any value written to the counter causes the counter to reset to $00, the counter direction to be set to up, the immediate load of both duty and period registers with values from the buffers, and the output to change according to the polarity bit. When the channel is disabled (PWMEx = 0), the counter stops. When a channel becomes enabled (PWMEx = 1), the associated PWM counter continues from the count in the PWMCNTx register. This allows the waveform to continue where it left off when the channel is re-enabled. When the channel is disabled, writing “0” to the period register will cause the counter to reset on the next selected clock.

NOTE

If the user wants to start a new “clean” PWM waveform without any “history” from the old waveform, the user must write to channel counter (PWMCNTx) prior to enabling the PWM channel (PWMEx = 1).

Generally, writes to the counter are done prior to enabling a channel in order to start from a known state. However, writing a counter can also be done while the PWM channel is enabled (counting). The effect is similar to writing the counter when the channel is disabled, except that the new period is started immediately with the output set according to the polarity bit.

NOTE

Writing to the counter while the channel is enabled can cause an irregular PWM cycle to occur.

The counter is cleared at the end of the effective period (see Section 19.4.2.5, “Left Aligned Outputs” and Section 19.4.2.6, “Center Aligned Outputs” for more details).

Table 19-12. PWM Timer Counter Conditions

Counter Clears ($00)	Counter Counts	Counter Stops
When PWMCNTx register written to any value	When PWM channel is enabled (PWMEx = 1). Counts from last value in PWMCNTx.	When PWM channel is disabled (PWMEx = 0)
Effective period ends		

19.4.2.5 Left Aligned Outputs

The PWM timer provides the choice of two types of outputs, left aligned or center aligned. They are selected with the CAEx bits in the PWMCAE register. If the CAEx bit is cleared (CAEx = 0), the corresponding PWM output will be left aligned.

In left aligned output mode, the 8-bit counter is configured as an up counter only. It compares to two registers, a duty register and a period register as shown in the block diagram in Figure 19-16. When the PWM counter matches the duty register the output flip-flop changes state causing the PWM waveform to also change state. A match between the PWM counter and the period register resets the counter and the output flip-flop, as shown in Figure 19-16, as well as performing a load from the double buffer period and duty register to the associated registers, as described in Section 19.4.2.3, “PWM Period and Duty”. The counter counts from 0 to the value in the period register – 1.

Offset Module Base + 0x0005

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	DFDIE	SFDIE
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 26-10. Flash Error Configuration Register (FERCNFG)

All assigned bits in the FERCNFG register are readable and writable.

Table 26-14. FERCNFG Field Descriptions

Field	Description
1 DFDIE	**Double Bit Fault Detect Interrupt Enable** — The DFDIE bit controls interrupt generation when a double bit fault is detected during a Flash block read operation. 0 DFDIF interrupt disabled 1 An interrupt will be requested whenever the DFDIF flag is set (see Section 26.3.2.8)
0 SFDIE	**Single Bit Fault Detect Interrupt Enable** — The SFDIE bit controls interrupt generation when a single bit fault is detected during a Flash block read operation. 0 SFDIF interrupt disabled whenever the SFDIF flag is set (see Section 26.3.2.8) 1 An interrupt will be requested whenever the SFDIF flag is set (see Section 26.3.2.8)

26.3.2.7 Flash Status Register (FSTAT)

The FSTAT register reports the operational status of the Flash module.

Offset Module Base + 0x0006

	7	6	5	4	3	2	1	0
R	CCIF	0	ACCERR	FPVIOL	MGBUSY	RSVD	MGSTAT[1:0]	
W								
Reset	1	0	0	0	0	0	0[1]	0[1]

= Unimplemented or Reserved

Figure 26-11. Flash Status Register (FSTAT)

[1] Reset value can deviate from the value shown if a double bit fault is detected during the reset sequence (see Section 26.6).

CCIF, ACCERR, and FPVIOL bits are readable and writable, MGBUSY and MGSTAT bits are readable but not writable, while remaining bits read 0 and are not writable.

The FPROT register, described in Section 29.3.2.9, can be set to protect regions in the Flash memory from accidental program or erase. Three separate memory regions, one growing upward from global address 0x3_8000 in the Flash memory (called the lower region), one growing downward from global address 0x3_FFFF in the Flash memory (called the higher region), and the remaining addresses in the Flash memory, can be activated for protection. The Flash memory addresses covered by these protectable regions are shown in the P-Flash memory map. The higher address region is mainly targeted to hold the boot loader code since it covers the vector space. Default protection settings as well as security information that allows the MCU to restrict access to the Flash module are stored in the Flash configuration field as described in Table 29-4.

Table 29-4. Flash Configuration Field

Global Address	Size (Bytes)	Description
0x3_FF00-0x3_FF07	8	Backdoor Comparison Key Refer to Section 29.4.6.11, “Verify Backdoor Access Key Command,” and Section 29.5.1, “Unsecuring the MCU using Backdoor Key Access”
0x3_FF08-0x3_FF0B[1]	4	Reserved
0x3_FF0C[1]	1	P-Flash Protection byte. Refer to Section 29.3.2.9, “P-Flash Protection Register (FPROT)”
0x3_FF0D[1]	1	EEPROM Protection byte. Refer to Section 29.3.2.10, “EEPROM Protection Register (DFPROT)”
0x3_FF0E[1]	1	Flash Nonvolatile byte Refer to Section 29.3.2.16, “Flash Option Register (FOPT)”
0x3_FF0F[1]	1	Flash Security byte Refer to Section 29.3.2.2, “Flash Security Register (FSEC)”

1 0x3FF08-0x3_FF0F form a Flash phrase and must be programmed in a single command write sequence. Each byte in the 0x3_FF08 - 0x3_FF0B reserved field should be programmed to 0xFF.

Table 30-14. FERCNFG Field Descriptions

Field	Description
1 DFDIE	**Double Bit Fault Detect Interrupt Enable** — The DFDIE bit controls interrupt generation when a double bit fault is detected during a Flash block read operation. 0 DFDIF interrupt disabled 1 An interrupt will be requested whenever the DFDIF flag is set (see Section 30.3.2.8)
0 SFDIE	**Single Bit Fault Detect Interrupt Enable** — The SFDIE bit controls interrupt generation when a single bit fault is detected during a Flash block read operation. 0 SFDIF interrupt disabled whenever the SFDIF flag is set (see Section 30.3.2.8) 1 An interrupt will be requested whenever the SFDIF flag is set (see Section 30.3.2.8)

30.3.2.7 Flash Status Register (FSTAT)

The FSTAT register reports the operational status of the Flash module.

Offset Module Base + 0x0006

	7	6	5	4	3	2	1	0
R	CCIF	0	ACCERR	FPVIOL	MGBUSY	RSVD	MGSTAT[1:0]	
W								
Reset	1	0	0	0	0	0	0[1]	0[1]

= Unimplemented or Reserved

Figure 30-11. Flash Status Register (FSTAT)

[1] Reset value can deviate from the value shown if a double bit fault is detected during the reset sequence (see Section 30.6).

CCIF, ACCERR, and FPVIOL bits are readable and writable, MGBUSY and MGSTAT bits are readable but not writable, while remaining bits read 0 and are not writable.

Table 30-15. FSTAT Field Descriptions

Field	Description
7 CCIF	**Command Complete Interrupt Flag** — The CCIF flag indicates that a Flash command has completed. The CCIF flag is cleared by writing a 1 to CCIF to launch a command and CCIF will stay low until command completion or command violation. 0 Flash command in progress 1 Flash command has completed
5 ACCERR	**Flash Access Error Flag** — The ACCERR bit indicates an illegal access has occurred to the Flash memory caused by either a violation of the command write sequence (see Section 30.4.4.2) or issuing an illegal Flash command. While ACCERR is set, the CCIF flag cannot be cleared to launch a command. The ACCERR bit is cleared by writing a 1 to ACCERR. Writing a 0 to the ACCERR bit has no effect on ACCERR. 0 No access error detected 1 Access error detected
4 FPVIOL	**Flash Protection Violation Flag** —The FPVIOL bit indicates an attempt was made to program or erase an address in a protected area of P-Flash or EEPROM memory during a command write sequence. The FPVIOL bit is cleared by writing a 1 to FPVIOL. Writing a 0 to the FPVIOL bit has no effect on FPVIOL. While FPVIOL is set, it is not possible to launch a command or start a command write sequence. 0 No protection violation detected 1 Protection violation detected

Table 30-4). The Verify Backdoor Access Key command must not be executed from the Flash block containing the backdoor comparison key to avoid code runaway.

Table 30-52. Verify Backdoor Access Key Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x0C	Not required
001	Key 0	
010	Key 1	
011	Key 2	
100	Key 3	

Upon clearing CCIF to launch the Verify Backdoor Access Key command, the Memory Controller will check the FSEC KEYEN bits to verify that this command is enabled. If not enabled, the Memory Controller sets the ACCERR bit in the FSTAT register and terminates. If the command is enabled, the Memory Controller compares the key provided in FCCOB to the backdoor comparison key in the Flash configuration field with Key 0 compared to 0x3_FF00, etc. If the backdoor keys match, security will be released. If the backdoor keys do not match, security is not released and all future attempts to execute the Verify Backdoor Access Key command are aborted (set ACCERR) until a reset occurs. The CCIF flag is set after the Verify Backdoor Access Key operation has completed.

Table 30-53. Verify Backdoor Access Key Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 100 at command launch
		Set if an incorrect backdoor key is supplied
		Set if backdoor key access has not been enabled (KEYEN[1:0] != 10, see Section 30.3.2.2)
		Set if the backdoor key has mismatched since the last reset
	FPVIOL	None
	MGSTAT1	None
	MGSTAT0	None

30.4.6.12 Set User Margin Level Command

The Set User Margin Level command causes the Memory Controller to set the margin level for future read operations of the P-Flash or EEPROM block.

Table 30-54. Set User Margin Level Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x0D	Flash block selection code [1:0]. See Table 30-34
001	Margin level setting.	

Table A-16. Run and Wait Current Characteristics (Junction Temperature From +150°C To +160°C)

Conditions are: V_{DDR}=5.5V, T_A=150°C, see Table A-13. and Table A-14.							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
S12GN16, S12GN32							
1	M	IDD Run Current (code execution from RAM)	I_{DDRr}		12.7		mA
2	C	IDD Run Current (code execution from flash)	I_{DDRf}		13.2		mA
3	M	IDD Wait Current	I_{DDW}		7.4		mA

Table A-23. ADC Conversion Performance 5V range (Junction Temperature From –40°C To +150°C)

S12GN16, S12GN32, S12GN48, S12G48, S12G64, S12G96, S12G128, S12G192, and S12G240								
Supply voltage 4.5V < V_{DDA} < 5.5 V, -40°C < T_J < 150°C, V_{REF} = V_{RH} - V_{RL} = V_{DDA}, f_{ADCCLK} = 8.0MHz The values are tested to be valid with no port AD output drivers switching simultaneous with conversions.								
Num	**C**	**Rating[1]**		**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	P	Resolution	10-Bit	LSB		5		mV
2	P	Differential Nonlinearity	10-Bit	DNL	-1	±0.5	1	counts
3	P	Integral Nonlinearity	10-Bit	INL	-2	±1	2	counts
4	P	Absolute Error[2]	10-Bit[3] 10-Bit[4]	AE	-3 -4	±2 ±2	3 4	counts
5	C	Resolution	8-Bit	LSB		20		mV
6	C	Differential Nonlinearity	8-Bit	DNL	-0.5	±0.3	0.5	counts
7	C	Integral Nonlinearity	8-Bit	INL	-1	±0.5	1	counts
8	C	Absolute Error[2]	8-Bit	AE	-1.5	±1	1.5	counts

1 The 8-bit mode operation is structurally tested in production test. Absolute values are tested in 10-bit mode.

2 These values include the quantization error which is inherently 1/2 count for any A/D converter.

3 LQFP 48 and bigger

4 LQFP 32 and smaller

In Table A-52 the timing characteristics for slave mode are listed.

Table A-52. SPI Slave Mode Timing Characteristics

Conditions are 4.5 V < V_{DD35} < 5.5 V junction temperature from –40°C to T_{Jmax}.							
Num	**C**	**Characteristic**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	D	SCK Frequency	f_{sck}	DC	—	1/4	f_{bus}
1	D	SCK Period	t_{sck}	4	—	∞	t_{bus}
2	D	Enable Lead Time	t_L	4	—	—	t_{bus}
3	D	Enable Trail Time	t_T	4	—	—	t_{bus}
4	D	Clock (SCK) High or Low Time	t_{wsck}	4	—	—	t_{bus}
5	D	Data Setup Time (Inputs)	t_{su}	8	—	—	ns
6	D	Data Hold Time (Inputs)	t_{hi}	8	—	—	ns
7	D	Slave Access Time (time to data active)	t_a	—	—	20	ns
8	D	Slave MISO Disable Time	t_{dis}	—	—	22	ns
9	D	Data Valid after SCK Edge	t_{vsck}	—	—	$28 + 0.5 \cdot t_{bus}$ [1]	ns
10	D	Data Valid after $\overline{SS}$ fall	t_{vss}	—	—	$28 + 0.5 \cdot t_{bus}$ [1]	ns
11	D	Data Hold Time (Outputs)	t_{ho}	20	—	—	ns
12	D	Rise and Fall Time Inputs	t_{rfi}	—	—	9	ns
13	D	Rise and Fall Time Outputs	t_{rfo}	—	—	9	ns

[1] $0.5t_{bus}$ added due to internal synchronization delay

A.16 ADC Conversion Result Reference

The reference voltage V_{DDF} is measured under the conditions shown in Table A-53. The value stored in the IFR is the average of eight consecutive conversions at T_j=150 °C and eight consecutive conversions at T_j=-40 °C.

Table A-53. Measurement Conditions

Description	Symbol	Value	Unit
Regulator supply voltage	V_{DDR}	5	V
I/O supply voltage	V_{DDX}	5	V
Analog supply voltage	V_{DDA}	5	V
ADC reference voltage	V_{RH}	5	V
ADC clock	f_{ADCCLK}	2	MHz
ADC sample time	t_{SMP}	4	ADC clock cycles
Bus frequency	f_{bus}	24	MHz
Junction temperature	T_j	150 and -40	°C
Code execution		from RAM	