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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | 12V1 |
| Core Size | 16-Bit |
| Speed | 25MHz |
| Connectivity | CANbus, IrDA, LINbus, SCI, SPI |
| Peripherals | LVD, POR, PWM, WDT |
| Number of I/O | 86 |
| Program Memory Size | 240KB (240K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 4K x 8 |
| RAM Size | 11K x 8 |
| Voltage - Supply (Vcc/Vdd) | 3.13V ~ 5.5V |
| Data Converters | A/D 16x12b; D/A 2x8b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-LQFP |
| Supplier Device Package | 100-LQFP (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/s9s12ga240f0vll |

**Table 1-24. 64-Pin LQFP Pinout for S12GA96 and S12GA128**

| | Function <----lowest-----PRIORITY-----highest----> | | | | | Power Supply | Internal Pull Resistor | |
|---|---|---|---|---|---|---|---|---|
| Package Pin | Pin | 2nd Func. | 3rd Func. | 4th Func | 5th Func | | CTRL | Reset State |
| 1 | PJ6 | KWJ6 | SCK2 | — | — | $V_{DDX}$ | PERJ/PPSJ | Up |
| 2 | PJ5 | KWJ5 | MOSI2 | — | — | $V_{DDX}$ | PERJ/PPSJ | Up |
| 3 | PJ4 | KWJ4 | MISO2 | — | — | $V_{DDX}$ | PERJ/PPSJ | Up |
| 4 | RESET | — | — | — | — | $V_{DDX}$ | PULLUP | |
| 5 | VDDX | — | — | — | — | — | — | — |
| 6 | VDDR | — | — | — | — | — | — | — |
| 7 | VSSX | — | — | — | — | — | — | — |
| 8 | PE0[1] | EXTAL | — | — | — | $V_{DDX}$ | PUCR/PDPEE | Down |
| 9 | VSS | — | — | — | — | — | — | — |
| 10 | PE1[1] | XTAL | — | — | — | $V_{DDX}$ | PUCR/PDPEE | Down |
| 11 | TEST | — | — | — | — | N.A. | $\overline{\text{RESET}}$ pin | Down |
| 12 | PJ0 | KWJ0 | MISO1 | — | — | $V_{DDX}$ | PERJ/PPSJ | Up |
| 13 | PJ1 | KWJ1 | MOSI1 | — | — | $V_{DDX}$ | PERJ/PPSJ | Up |
| 14 | PJ2 | KWJ2 | SCK1 | — | — | $V_{DDX}$ | PERJ/PPSJ | Up |
| 15 | PJ3 | KWJ3 | $\overline{\text{SS1}}$ | — | — | $V_{DDX}$ | PERJ/PPSJ | Up |
| 16 | BKGD | MODC | — | — | — | $V_{DDX}$ | PUCR/BKPUE | Up |
| 17 | PP0 | KWP0 | ETRIG0 | API_EXTCLK | PWM0 | $V_{DDX}$ | PERP/PPSP | Disabled |
| 18 | PP1 | KWP1 | ETRIG1 | ECLKX2 | PWM1 | $V_{DDX}$ | PERP/PPSP | Disabled |
| 19 | PP2 | KWP2 | ETRIG2 | PWM2 | — | $V_{DDX}$ | PERP/PPSP | Disabled |
| 20 | PP3 | KWP3 | ETRIG3 | PWM3 | — | $V_{DDX}$ | PERP/PPSP | Disabled |
| 21 | PP4 | KWP4 | PWM4 | — | — | $V_{DDX}$ | PERP/PPSP | Disabled |
| 22 | PP5 | KWP5 | PWM5 | — | — | $V_{DDX}$ | PERP/PPSP | Disabled |
| 23 | PP6 | KWP6 | PWM6 | — | — | $V_{DDX}$ | PERP/PPSP | Disabled |
| 24 | PP7 | KWP7 | PWM7 | — | — | $V_{DDX}$ | PERP/PPSP | Disabled |
| 25 | PT7 | IOC7 | — | — | — | $V_{DDX}$ | PERT/PPST | Disabled |
| 26 | PT6 | IOC6 | — | — | — | $V_{DDX}$ | PERT/PPST | Disabled |
| 27 | PT5 | IOC5 | — | — | — | $V_{DDX}$ | PERT/PPST | Disabled |

**Table 1-32. KGD Option for S12GA192 and S12GA240**

| | Function <----lowest-----PRIORITY-----highest----> | | | | Power Supply | Internal Pull Resistor | |
|---|---|---|---|---|---|---|---|
| Wire Bond Die Pad | Pin | 2nd Func. | 3rd Func. | 4th Func. | | CTRL | Reset State |
| 27 | PB2 | ECLKX2 | — | — | $V_{DDX}$ | PUCR/PUPBE | Disabled |
| 28 | PB3 | — | — | — | $V_{DDX}$ | PUCR/PUPBE | Disabled |
| 29 | PP0 | KWP0 | ETRIG0 | PWM0 | $V_{DDX}$ | PERP/PPSP | Disabled |
| 30 | PP1 | KWP1 | ETRIG1 | PWM1 | $V_{DDX}$ | PERP/PPSP | Disabled |
| 31 | PP2 | KWP2 | ETRIG2 | PWM2 | $V_{DDX}$ | PERP/PPSP | Disabled |
| 32 | PP3 | KWP3 | ETRIG3 | PWM3 | $V_{DDX}$ | PERP/PPSP | Disabled |
| 33 | PP4 | KWP4 | PWM4 | — | $V_{DDX}$ | PERP/PPSP | Disabled |
| 34 | PP5 | KWP5 | PWM5 | — | $V_{DDX}$ | PERP/PPSP | Disabled |
| 35 | PP6 | KWP6 | PWM6 | — | $V_{DDX}$ | PERP/PPSP | Disabled |
| 36 | PP7 | KWP7 | PWM7 | — | $V_{DDX}$ | PERP/PPSP | Disabled |
| 37 | VDDX3 | — | — | — | — | — | — |
| 38 | VSSX3 | — | — | — | — | — | — |
| 39 | PT7 | IOC7 | — | — | $V_{DDX}$ | PERT/PPST | Disabled |
| 40 | PT6 | IOC6 | — | — | $V_{DDX}$ | PERT/PPST | Disabled |
| 41 | PT5 | IOC5 | — | — | $V_{DDX}$ | PERT/PPST | Disabled |
| 42 | PT4 | IOC4 | — | — | $V_{DDX}$ | PERT/PPST | Disabled |
| 43 | PT3 | IOC3 | — | — | $V_{DDX}$ | PERT/PPST | Disabled |
| 44 | PT2 | IOC2 | — | — | $V_{DDX}$ | PERT/PPST | Disabled |
| 45 | PT1 | IOC1 | — | — | $V_{DDX}$ | PERT/PPST | Disabled |
| 46 | PT0 | IOC0 | — | — | $V_{DDX}$ | PERT/PPST | Disabled |
| 47 | PB4 | $\overline{\text{IRQ}}$ | — | — | $V_{DDX}$ | PUCR/PUPBE | Disabled |
| 48 | PB5 | $\overline{\text{XIRQ}}$ | — | — | $V_{DDX}$ | PUCR/PUPBE | Disabled |
| 49 | PB6 | — | — | — | $V_{DDX}$ | PUCR/PUPBE | Disabled |
| 50 | PB7 | — | — | — | $V_{DDX}$ | PUCR/PUPBE | Disabled |
| 51 | PC0 | — | — | — | $V_{DDA}$ | PUCR/PUPCE | Disabled |
| 52 | PC1 | — | — | — | $V_{DDA}$ | PUCR/PUPCE | Disabled |
| 53 | PC2 | — | — | — | $V_{DDA}$ | PUCR/PUPCE | Disabled |
| 54 | PC3 | — | — | — | $V_{DDA}$ | PUCR/PUPCE | Disabled |
| 55 | PAD0 | KWAD0 | AN0 | — | $V_{DDA}$ | PER1AD/PPS1AD | Disabled |

**Table 2-40. PTS Register Field Descriptions**

| Field | Description |
|---|---|
| 7-0<br>PTS | **Port S general-purpose input/output data**—Data Register<br>When not used with an alternative signal, the associated pin can be used as general-purpose I/O. In general-purpose output mode the port data register bit value is driven to the pin.<br>If the associated data direction bit is set to 1, a read returns the value of the port data register bit, otherwise the buffered pin input state is read. |

## 2.4.3.21 Port S Input Register (PTIS)

Address 0x0249 Access: User read only[1]

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R | PTIS7 | PTIS6 | PTIS5 | PTIS4 | PTIS3 | PTIS2 | PTIS1 | PTIS0 |
| W | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Figure 2-22. Port S Input Register (PTIS)**

[1] Read: Anytime
Write:Never

**Table 2-41. PTIS Register Field Descriptions**

| Field | Description |
|---|---|
| 7-0<br>PTIS | **Port S input data—**<br>A read always returns the buffered input state of the associated pin. It can be used to detect overload or short circuit conditions on output pins. |

## 2.4.3.22 Port S Data Direction Register (DDRS)

Address 0x024A Access: User read/write[1]

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R<br>W | DDRS7 | DDRS6 | DDRS5 | DDRS4 | DDRS3 | DDRS2 | DDRS1 | DDRS0 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Figure 2-23. Port S Data Direction Register (DDRS)**

[1] Read: Anytime
Write: Anytime

**Table 2-64. PERP Register Field Descriptions**

| Field | Description |
|---|---|
| 7-0<br>PERP | **Port P pull device enable**—Enable pull device on input pin<br>This bit controls whether a pull device on the associated port input pin is active. If a pin is used as output this bit has no effect. The polarity is selected by the related polarity select register bit.<br><br>1 Pull device enabled<br>0 Pull device disabled |

## 2.4.3.38 Port P Polarity Select Register (PPSP)

Address 0x025D (G1, G2) Access: User read/write[1]

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R<br>W | PPSP7 | PPSP6 | PPSP5 | PPSP4 | PPSP3 | PPSP2 | PPSP1 | PPSP0 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Address 0x025D (G3) Access: User read/write[1]

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R | 0 | 0 | PPSP5 | PPSP4 | PPSP3 | PPSP2 | PPSP1 | PPSP0 |
| W | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Figure 2-39. Port P Polarity Select Register (PPSP)**

[1] Read: Anytime
Write: Anytime

**Table 2-65. PPSP Register Field Descriptions**

| Field | Description |
|---|---|
| 7-0<br>PPSP | **Port P pull device select**—Configure pull device and pin interrupt edge polarity on input pin<br>This bit selects a pullup or a pulldown device if enabled on the associated port input pin.<br>This bit also selects the polarity of the active pin interrupt edge.<br><br>1 Pulldown device selected; rising edge selected<br>0 Pullup device selected; falling edge selected |

Figure 10-2 shows a block diagram of the XOSCLCP.

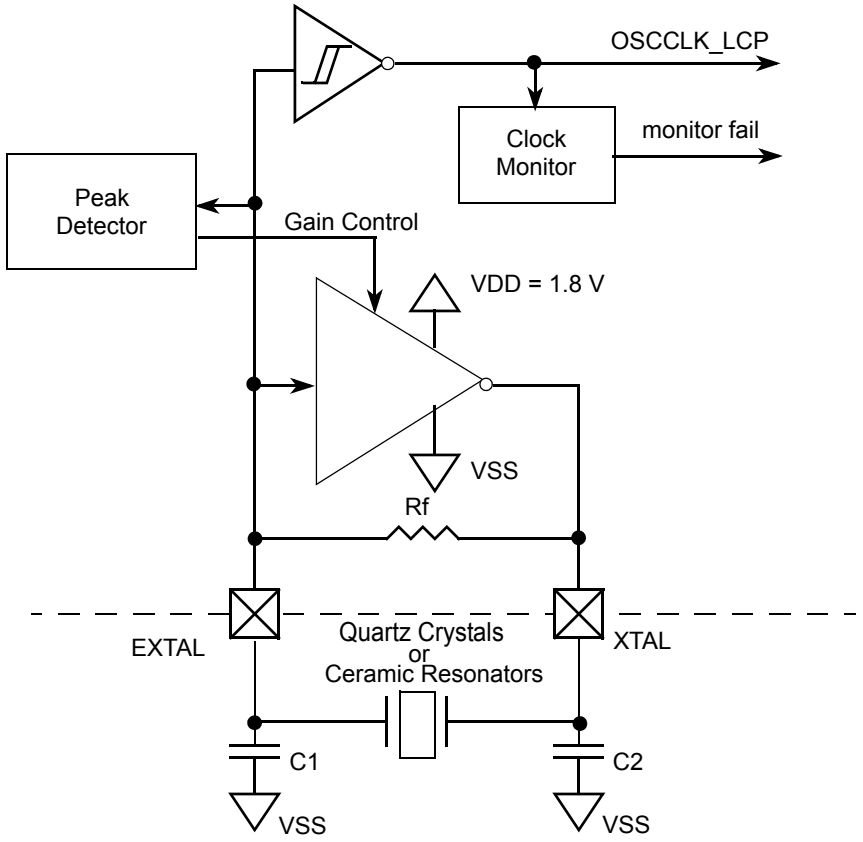



**Figure 10-2. XOSCLCP Block Diagram**

## 10.2 Signal Description

This section lists and describes the signals that connect off chip.

### 10.2.1 $\overline{\text{RESET}}$

Pin $\overline{\text{RESET}}$ is an active-low bidirectional pin. As an input it initializes the MCU asynchronously to a known start-up state. As an open-drain output it indicates that an MCU-internal reset has been triggered.

### 10.2.2 EXTAL and XTAL

These pins provide the interface for a crystal to control the internal clock generator circuitry. EXTAL is the input to the crystal oscillator amplifier. XTAL is the output of the crystal oscillator amplifier. If XOSCLCP is enabled, the MCU internal OSCCLK_LCP is derived from the EXTAL input frequency. If OSCE=0, the EXTAL pin is pulled down by an internal resistor of approximately 200 kΩ and the XTAL pin is pulled down by an internal resistor of approximately 700 kΩ.

**Table 12-13. Sample Time Select**

| SMP2 | SMP1 | SMP0 | Sample Time in Number of ATD Clock Cycles |
|---|---|---|---|
| 1 | 1 | 1 | 24 |

### 12.3.2.6 ATD Control Register 5 (ATDCTL5)

Writes to this register will abort current conversion sequence and start a new conversion sequence. If the external trigger function is enabled (ETRIGE=1) an initial write to ATDCTL5 is required to allow starting of a conversion sequence which will then occur on each trigger event. Start of conversion means the beginning of the sampling phase.

Module Base + 0x0005

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R | 0 | SC | SCAN | MULT | CD | CC | CB | CA |
| W | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

= Unimplemented or Reserved

**Figure 12-8. ATD Control Register 5 (ATDCTL5)**

Read: Anytime

Write: Anytime

**Table 12-14. ATDCTL5 Field Descriptions**

| Field | Description |
|---|---|
| 6<br>SC | **Special Channel Conversion Bit** — If this bit is set, then special channel conversion can be selected using CD, CC, CB and CA of ATDCTL5. Table 12-15 lists the coding.<br>0 Special channel conversions disabled<br>1 Special channel conversions enabled |
| 5<br>SCAN | **Continuous Conversion Sequence Mode** — This bit selects whether conversion sequences are performed continuously or only once. If the external trigger function is enabled (ETRIGE=1) setting this bit has no effect, thus the external trigger always starts a single conversion sequence.<br>0 Single conversion sequence<br>1 Continuous conversion sequences (scan mode) |

**Table 14-16. ATDSTAT0 Field Descriptions (continued)**

| Field | Description |
|---|---|
| 3–0<br>CC[3:0] | **Conversion Counter** — These 4 read-only bits are the binary value of the conversion counter. The conversion counter points to the result register that will receive the result of the current conversion. E.g. CC3=0, CC2=1, CC1=1, CC0=0 indicates that the result of the current conversion will be in ATD Result Register 6. If in non-FIFO mode (FIFO=0) the conversion counter is initialized to zero at the beginning and end of the conversion sequence. If in FIFO mode (FIFO=1) the register counter is not initialized. The conversion counter wraps around when its maximum value is reached.<br>Aborting a conversion or starting a new conversion clears the conversion counter even if FIFO=1. |

## 14.3.2.8 ATD Compare Enable Register (ATDCMPE)

Writes to this register will abort current conversion sequence.

Read: Anytime

Write: Anytime

Module Base + 0x0008

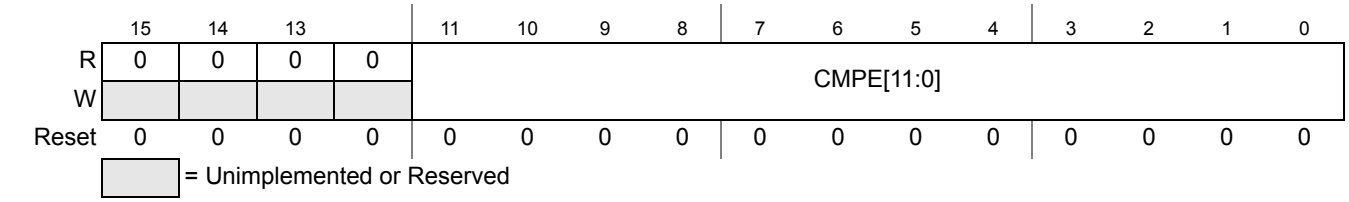



**Figure 14-10. ATD Compare Enable Register (ATDCMPE)**

**Table 14-17. ATDCMPE Field Descriptions**

| Field | Description |
|---|---|
| 11–0<br>CMPE[11:0] | **Compare Enable for Conversion Number *n* (*n*= 11, 10, 9, 8, 7, 6, 5, 4, 3, 2, 1, 0) of a Sequence (*n conversion number, NOT channel number!)*** — These bits enable automatic compare of conversion results individually for conversions of a sequence. The sense of each comparison is determined by the CMPHT[*n*] bit in the ATDCMPHT register.<br>For each conversion number with CMPE[*n*]=1 do the following:<br>1) Write compare value to ATDDR*n* result register<br>2) Write compare operator with CMPHT[*n*] in ATDCPMHT register<br>CCF[*n*] in ATDSTAT2 register will flag individual success of any comparison.<br>0 No automatic compare<br>1 Automatic compare of results for conversion *n* of a sequence is enabled. |

### 14.3.2.10 ATD Input Enable Register (ATDDIEN)

Module Base + 0x000C

| | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R | 1 | 1 | 1 | 1 | IEN[11:0] | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

= Unimplemented or Reserved

**Figure 14-12. ATD Input Enable Register (ATDDIEN)**

Read: Anytime

Write: Anytime

**Table 14-19. ATDDIEN Field Descriptions**

| Field | Description |
|---|---|
| 11–0<br>IEN[11:0] | **ATD Digital Input Enable on channel *x* (*x*= 11, 10, 9, 8, 7, 6, 5, 4, 3, 2, 1, 0)** — This bit controls the digital input buffer from the analog input pin (AN*x*) to the digital data register.<br>0 Disable digital input buffer to AN*x* pin<br>1 Enable digital input buffer on AN*x* pin.<br>**Note:** Setting this bit will enable the corresponding digital input buffer continuously. If this bit is set while simultaneously using it as an analog port, there is potentially increased power consumption because the digital input buffer maybe in the linear region. |

### 14.3.2.11 ATD Compare Higher Than Register (ATDCMPHT)

Writes to this register will abort current conversion sequence.

Read: Anytime

Write: Anytime

Module Base + 0x000E

| | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R | 0 | 0 | 0 | 0 | CMPHT[11:0] | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

= Unimplemented or Reserved

**Figure 14-13. ATD Compare Higher Than Register (ATDCMPHT)**

**Table 14-20. ATDCMPHT Field Descriptions**

| Field | Description |
|---|---|
| 11–0<br>CMPHT[11:0] | **Compare Operation Higher Than Enable for conversion number *n* (*n*= 11, 10, 9, 8, 7, 6, 5, 4, 3, 2, 1, 0) of a Sequence (*n conversion number, NOT channel number!)*** — This bit selects the operator for comparison of conversion results.<br>0 If result of conversion *n* is **lower or same than** compare value in ATDDR*n*, this is flagged in ATDSTAT2<br>1 If result of conversion *n* is **higher than** compare value in ATDDR*n*, this is flagged in ATDSTAT2 |

## 15.1 Introduction

The ADC10B16C is a 16-channel, 10-bit, multiplexed input successive approximation analog-to-digital converter. Refer to device electrical specifications for ATD accuracy.

### 15.1.1 Features

- 8-, 10-bit resolution.
- Automatic return to low power after conversion sequence
- Automatic compare with interrupt for higher than or less/equal than programmable value
- Programmable sample time.
- Left/right justified result data.
- External trigger control.
- Sequence complete interrupt.
- Analog input multiplexer for 8 analog input channels.
- Special conversions for VRH, VRL, (VRL+VRH)/2.
- 1-to-16 conversion sequence lengths.
- Continuous conversion mode.
- Multiple channel scans.
- Configurable external trigger functionality on any AD channel or any of four additional trigger inputs. The four additional trigger inputs can be chip external or internal. Refer to device specification for availability and connectivity.
- Configurable location for channel wrap around (when converting multiple channels in a sequence).

Module Base + 0x00006

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R<br>W | PCLKAB7 | PCLKAB6 | PCLKAB5 | PCLKAB4 | PCLKAB3 | PCLKAB2 | PCLKAB1 | PCLKAB0 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Figure 19-9. PWM Clock Select Register (PWMCLKAB)**

Read: Anytime

Write: Anytime

**NOTE**

Register bits PCLKAB0 to PCLKAB7 can be written anytime. If a clock select is changed while a PWM signal is being generated, a truncated or stretched pulse can occur during the transition.

**Table 19-11. PWMCLK Field Descriptions**

**Note:** Bits related to available channels have functional significance. Writing to unavailable bits has no effect. Read from unavailable bits return a zero

| Field | Description |
|---|---|
| 7<br>PCLKAB7 | Pulse Width Channel 7 Clock A/B Select<br>0 Clock B or SB is the clock source for PWM channel 7, as shown in Table 19-6.<br>1 Clock A or SA is the clock source for PWM channel 7, as shown in Table 19-6. |
| 6<br>PCLKAB6 | Pulse Width Channel 6 Clock A/B Select<br>0 Clock B or SB is the clock source for PWM channel 6, as shown in Table 19-6.<br>1 Clock A or SA is the clock source for PWM channel 6, as shown in Table 19-6. |
| 5<br>PCLKAB5 | Pulse Width Channel 5 Clock A/B Select<br>0 Clock A or SA is the clock source for PWM channel 5, as shown in Table 19-5.<br>1 Clock B or SB is the clock source for PWM channel 5, as shown in Table 19-5. |
| 4<br>PCLKAB4 | Pulse Width Channel 4 Clock A/B Select<br>0 Clock A or SA is the clock source for PWM channel 4, as shown in Table 19-5.<br>1 Clock B or SB is the clock source for PWM channel 4, as shown in Table 19-5. |
| 3<br>PCLKAB3 | Pulse Width Channel 3 Clock A/B Select<br>0 Clock B or SB is the clock source for PWM channel 3, as shown in Table 19-6.<br>1 Clock A or SA is the clock source for PWM channel 3, as shown in Table 19-6. |
| 2<br>PCLKAB2 | Pulse Width Channel 2 Clock A/B Select<br>0 Clock B or SB is the clock source for PWM channel 2, as shown in Table 19-6.<br>1 Clock A or SA is the clock source for PWM channel 2, as shown in Table 19-6. |
| 1<br>PCLKAB1 | Pulse Width Channel 1 Clock A/B Select<br>0 Clock A or SA is the clock source for PWM channel 1, as shown in Table 19-5.<br>1 Clock B or SB is the clock source for PWM channel 1, as shown in Table 19-5. |
| 0<br>PCLKAB0 | Pulse Width Channel 0 Clock A/B Select<br>0 Clock A or SA is the clock source for PWM channel 0, as shown in Table 19-5.<br>1 Clock B or SB is the clock source for PWM channel 0, as shown in Table 19-5. |

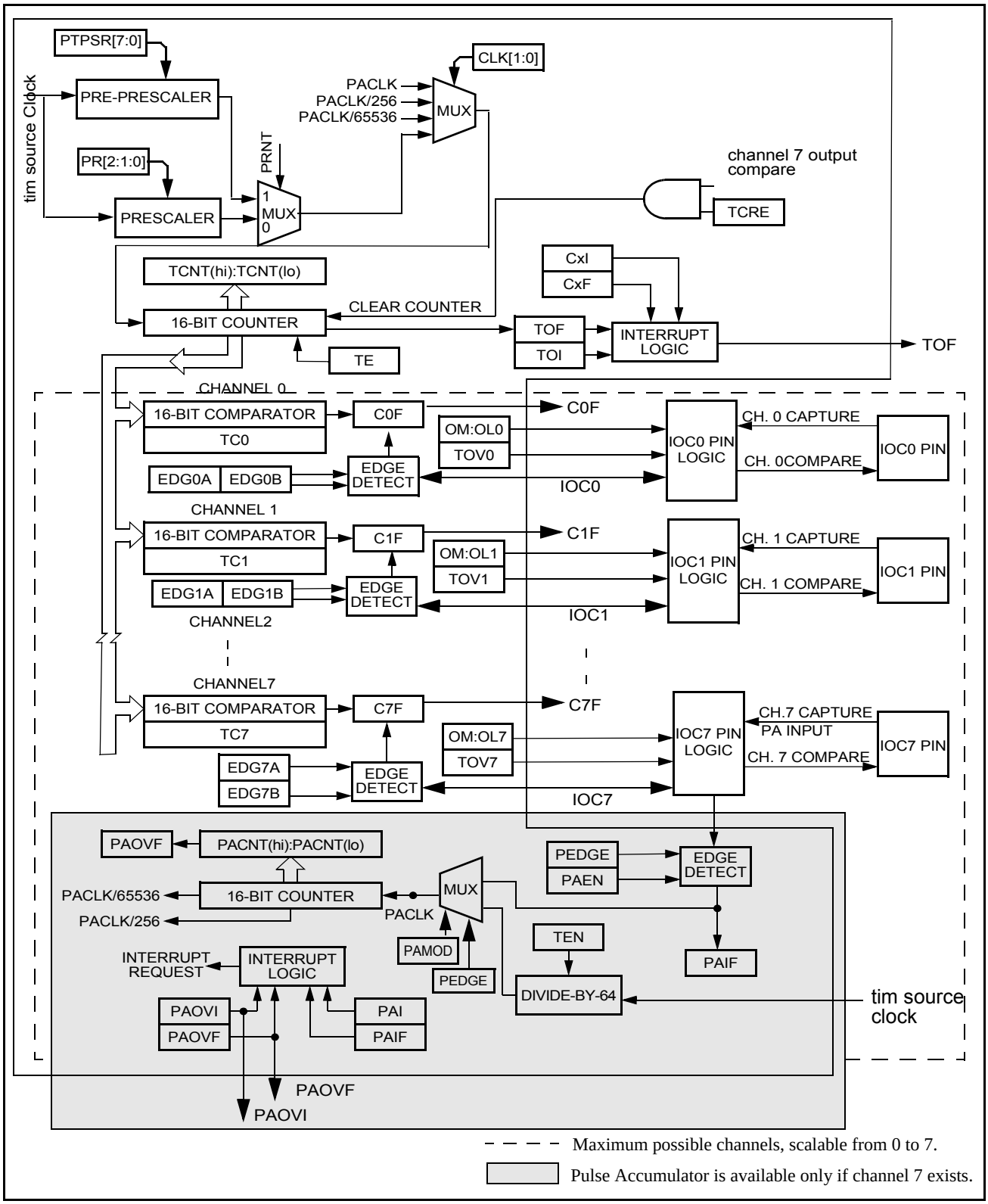



**Figure 23-30. Detailed Timer Block Diagram**

**Table 25-16. FERSTAT Field Descriptions**

| Field | Description |
|---|---|
| 1<br>DFDIF | **Double Bit Fault Detect Interrupt Flag** — The setting of the DFDIF flag indicates that a double bit fault was detected in the stored parity and data bits during a Flash array read operation or that a Flash array read operation returning invalid data was attempted on a Flash block that was under a Flash command operation.[1] The DFDIF flag is cleared by writing a 1 to DFDIF. Writing a 0 to DFDIF has no effect on DFDIF.[2]<br>0 No double bit fault detected<br>1 Double bit fault detected or a Flash array read operation returning invalid data was attempted while command running |
| 0<br>SFDIF | **Single Bit Fault Detect Interrupt Flag** — With the IGNSF bit in the FCNFG register clear, the SFDIF flag indicates that a single bit fault was detected in the stored parity and data bits during a Flash array read operation or that a Flash array read operation returning invalid data was attempted on a Flash block that was under a Flash command operation.[1] The SFDIF flag is cleared by writing a 1 to SFDIF. Writing a 0 to SFDIF has no effect on SFDIF.<br>0 No single bit fault detected<br>1 Single bit fault detected and corrected or a Flash array read operation returning invalid data was attempted while command running |

1 The single bit fault and double bit fault flags are mutually exclusive for parity errors (an ECC fault occurrence can be either single fault or double fault but never both). A simultaneous access collision (Flash array read operation returning invalid data attempted while command running) is indicated when both SFDIF and DFDIF flags are high.

2 There is a one cycle delay in storing the ECC DFDIF and SFDIF fault flags in this register. At least one NOP is required after a flash memory read before checking FERSTAT for the occurrence of ECC errors.

### 25.3.2.9 P-Flash Protection Register (FPROT)

The FPROT register defines which P-Flash sectors are protected against program and erase operations.

Offset Module Base + 0x0008

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R | FPOPEN | RNV6 | FPHDIS | FPHS[1:0] | | FPLDIS | FPLS[1:0] | |
| W | | | | | | | | |
| Reset | F[1] | F[1] | F[1] | F[1] | F[1] | F[1] | F[1] | F[1] |

= Unimplemented or Reserved

**Figure 25-13. Flash Protection Register (FPROT)**

1 Loaded from IFR Flash configuration field, during reset sequence.

The (unreserved) bits of the FPROT register are writable with the restriction that the size of the protected region can only be increased (see Section 25.3.2.9.1, “P-Flash Protection Restrictions,” and Table 25-21).

During the reset sequence, the FPROT register is loaded with the contents of the P-Flash protection byte in the Flash configuration field at global address 0x3_FF0C located in P-Flash memory (see Table 25-4) as indicated by reset condition ‘F’ in Figure 25-13. To change the P-Flash protection that will be loaded during the reset sequence, the upper sector of the P-Flash memory must be unprotected, then the P-Flash protection byte must be reprogrammed. If a double bit fault is detected while reading the P-Flash phrase containing the P-Flash protection byte during the reset sequence, the FPOPEN bit will be cleared and remaining bits in the FPROT register will be set to leave the P-Flash memory fully protected.

### 26.4.8 Wait Mode

The Flash module is not affected if the MCU enters wait mode. The Flash module can recover the MCU from wait via the CCIF interrupt (see Section 26.4.7, “Interrupts”).

### 26.4.9 Stop Mode

If a Flash command is active (CCIF = 0) when the MCU requests stop mode, the current Flash operation will be completed before the MCU is allowed to enter stop mode.

## 26.5 Security

The Flash module provides security information to the MCU. The Flash security state is defined by the SEC bits of the FSEC register (see Table 26-11). During reset, the Flash module initializes the FSEC register using data read from the security byte of the Flash configuration field at global address 0x3_FF0F. The security state out of reset can be permanently changed by programming the security byte assuming that the MCU is starting from a mode where the necessary P-Flash erase and program commands are available and that the upper region of the P-Flash is unprotected. If the Flash security byte is successfully programmed, its new value will take affect after the next MCU reset.

The following subsections describe these security-related subjects:

- Unsecuring the MCU using Backdoor Key Access
- Unsecuring the MCU in Special Single Chip Mode using BDM
- Mode and Security Effects on Flash Command Availability

### 26.5.1 Unsecuring the MCU using Backdoor Key Access

The MCU may be unsecured by using the backdoor key access feature which requires knowledge of the contents of the backdoor keys (four 16-bit words programmed at addresses 0x3_FF00-0x3_FF07). If the KEYEN[1:0] bits are in the enabled state (see Section 26.3.2.2), the Verify Backdoor Access Key command (see Section 26.4.6.11) allows the user to present four prospective keys for comparison to the keys stored in the Flash memory via the Memory Controller. If the keys presented in the Verify Backdoor Access Key command match the backdoor keys stored in the Flash memory, the SEC bits in the FSEC register (see Table 26-11) will be changed to unsecure the MCU. Key values of 0x0000 and 0xFFFF are not permitted as backdoor keys. While the Verify Backdoor Access Key command is active, P-Flash memory and EEPROM memory will not be available for read access and will return invalid data.

### 28.3.2.5 Flash Configuration Register (FCNFG)

The FCNFG register enables the Flash command complete interrupt and forces ECC faults on Flash array read access from the CPU.

Offset Module Base + 0x0004

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R | CCIE | 0 | 0 | IGNSF | 0 | 0 | FDFD | FSFD |
| W | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

= Unimplemented or Reserved

**Figure 28-9. Flash Configuration Register (FCNFG)**

CCIE, IGNSF, FDFD, and FSFD bits are readable and writable while remaining bits read 0 and are not writable.

**Table 28-13. FCNFG Field Descriptions**

| Field | Description |
|---|---|
| 7<br>CCIE | **Command Complete Interrupt Enable** — The CCIE bit controls interrupt generation when a Flash command has completed.<br>0 Command complete interrupt disabled<br>1 An interrupt will be requested whenever the CCIF flag in the FSTAT register is set (see Section 28.3.2.7) |
| 4<br>IGNSF | **Ignore Single Bit Fault** — The IGNSF controls single bit fault reporting in the FERSTAT register (see Section 28.3.2.8).<br>0 All single bit faults detected during array reads are reported<br>1 Single bit faults detected during array reads are not reported and the single bit fault interrupt will not be generated |
| 1<br>FDFD | **Force Double Bit Fault Detect** — The FDFD bit allows the user to simulate a double bit fault during Flash array read operations and check the associated interrupt routine. The FDFD bit is cleared by writing a 0 to FDFD.<br>0 Flash array read operations will set the DFDIF flag in the FERSTAT register only if a double bit fault is detected<br>1 Any Flash array read operation will force the DFDIF flag in the FERSTAT register to be set (see Section 28.3.2.7) and an interrupt will be generated as long as the DFDIE interrupt enable in the FERCNFG register is set (see Section 28.3.2.6) |
| 0<br>FSFD | **Force Single Bit Fault Detect** — The FSFD bit allows the user to simulate a single bit fault during Flash array read operations and check the associated interrupt routine. The FSFD bit is cleared by writing a 0 to FSFD.<br>0 Flash array read operations will set the SFDIF flag in the FERSTAT register only if a single bit fault is detected<br>1 Flash array read operation will force the SFDIF flag in the FERSTAT register to be set (see Section 28.3.2.7) and an interrupt will be generated as long as the SFDIE interrupt enable in the FERCNFG register is set (see Section 28.3.2.6) |

### 28.3.2.6 Flash Error Configuration Register (FERCNFG)

The FERCNFG register enables the Flash error interrupts for the FERSTAT flags.

# Chapter 30
# 192 KByte Flash Module (S12FTMRG192K2V1)

**Table 30-1. Revision History**

| Revision Number | Revision Date | Sections Affected | Description of Changes |
|---|---|---|---|
| V01.06 | 23 Jun 2010 | 30.4.6.2/30-1107<br>30.4.6.12/30-1114<br>30.4.6.13/30-1115 | Updated description of the commands RD1BLK, MLOADU and MLOADF |
| V01.07 | 20 aug 2010 | 30.4.6.2/30-1107<br>30.4.6.12/30-1114<br>30.4.6.13/30-1115 | Updated description of the commands RD1BLK, MLOADU and MLOADF |
| Rev.1.27 | 31 Jan 2011 | 30.3.2.9/30-1090 | Updated description of protection on Section 30.3.2.9 |

## 30.1 Introduction

The FTMRG192K2 module implements the following:

- 192Kbytes of P-Flash (Program Flash) memory
- 4Kbytes of EEPROM memory

The Flash memory is ideal for single-supply applications allowing for field reprogramming without requiring external high voltage sources for program or erase operations. The Flash module includes a memory controller that executes commands to modify Flash memory contents. The user interface to the memory controller consists of the indexed Flash Common Command Object (FCCOB) register which is written to with the command, global address, data, and any required command parameters. The memory controller must complete the execution of a command before the FCCOB register can be written to with a new command.

**CAUTION**

A Flash word or phrase must be in the erased state before being programmed. Cumulative programming of bits within a Flash word or phrase is not allowed.

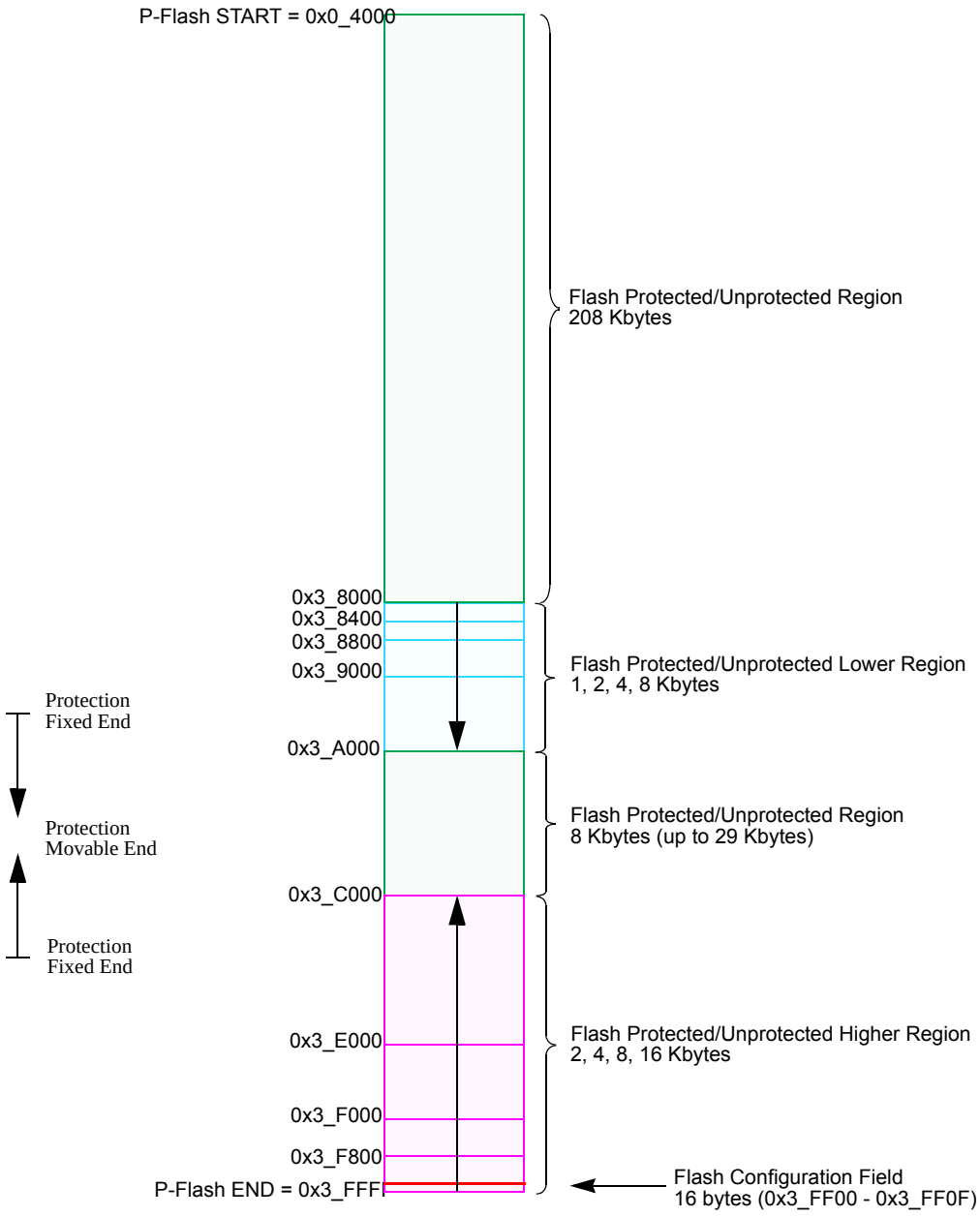



**Figure 31-2. P-Flash Memory Map**

**Table 31-5. Program IFR Fields**

| Global Address | Size (Bytes) | Field Description |
|---|---|---|
| 0x0_4000 – 0x0_4007 | 8 | Reserved |
| 0x0_4008 – 0x0_40B5 | 174 | Reserved |
| 0x0_40B6 – 0x0_40B7 | 2 | Version ID[1] |

**Table 31-36. Erase Verify P-Flash Section Command FCCOB Requirements**

| CCOBIX[2:0] | FCCOB Parameters | |
|---|---|---|
| 000 | 0x03 | Global address [17:16] of a P-Flash block |
| 001 | Global address [15:0] of the first phrase to be verified | |
| 010 | Number of phrases to be verified | |

Upon clearing CCIF to launch the Erase Verify P-Flash Section command, the Memory Controller will verify the selected section of Flash memory is erased. The CCIF flag will set after the Erase Verify P-Flash Section operation has completed. If the section is not erased, it means blank check failed, both MGSTAT bits will be set.

**Table 31-37. Erase Verify P-Flash Section Command Error Handling**

| Register | Error Bit | Error Condition |
|---|---|---|
| FSTAT | ACCERR | Set if CCOBIX[2:0] != 010 at command launch |
| | | Set if command not available in current mode (see Table 31-27) |
| | | Set if an invalid global address [17:0] is supplied see Table 31-3) |
| | | Set if a misaligned phrase address is supplied (global address [2:0] != 000) |
| | | Set if the requested section crosses a the P-Flash address boundary |
| | FPVIOL | None |
| | MGSTAT1 | Set if any errors have been encountered during the read or if blank check failed. |
| | MGSTAT0 | Set if any non-correctable errors have been encountered during the read or if blank check failed. |

### 31.4.6.4 Read Once Command

The Read Once command provides read access to a reserved 64 byte field (8 phrases) located in the nonvolatile information register of P-Flash. The Read Once field is programmed using the Program Once command described in Section 31.4.6.6. The Read Once command must not be executed from the Flash block containing the Program Once reserved field to avoid code runaway.

**Table 31-38. Read Once Command FCCOB Requirements**

| CCOBIX[2:0] | FCCOB Parameters | |
|---|---|---|
| 000 | 0x04 | Not Required |
| 001 | Read Once phrase index (0x0000 - 0x0007) | |
| 010 | Read Once word 0 value | |
| 011 | Read Once word 1 value | |
| 100 | Read Once word 2 value | |
| 101 | Read Once word 3 value | |

| Version Number | Revision Date | Description of Changes |
|---|---|---|
| Rev 0.49 | 5-Jun-2013 | • Updated Section A.1.1, “Parameter Classification”<br>• Applied new M-parameter tag in Table A-7, Table A-9, Table A-11, Table A-16, Table A-22, Table A-24, Table A-26, Table A-28, Table A-32, Table A-43, Table A-45, and Table A-48<br>• Updated Table A-39 (Num 2b, 6b) |
| Rev 0.50 | 15-Jul-2013 | • Updated Section A.7, “NVM” (format and timing parameters) |
| Rev 0.51 | 23-Oct-2017 | • Updated mask set condition in Table A-44 (Num 7a, 7b, 8a, 8b)<br>• Updated mask set condition in Table A-45 (Num 7a, 7b, 8a, 8b) |

# A.1 General

This supplement contains the most accurate electrical information for the MC9S12G microcontroller available at the time of publication.

This introduction is intended to give an overview on several common topics like power supply, current injection etc.

## A.1.1 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding the following classification is used and the parameters are tagged accordingly in the tables where appropriate.

**NOTE**

This classification is shown in the column labeled “C” in the parameter tables where appropriate.

P: Those parameters are guaranteed during production testing on each individual device.

M: These parameters are characterized at 160°C and tested in production at an ambient temperature of 150°C with appropriate guardbanding to guarantee operation at 160°C.

C: Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.

T: Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.

D: Those parameters are derived mainly from simulations.

## A.1.2 Power Supply

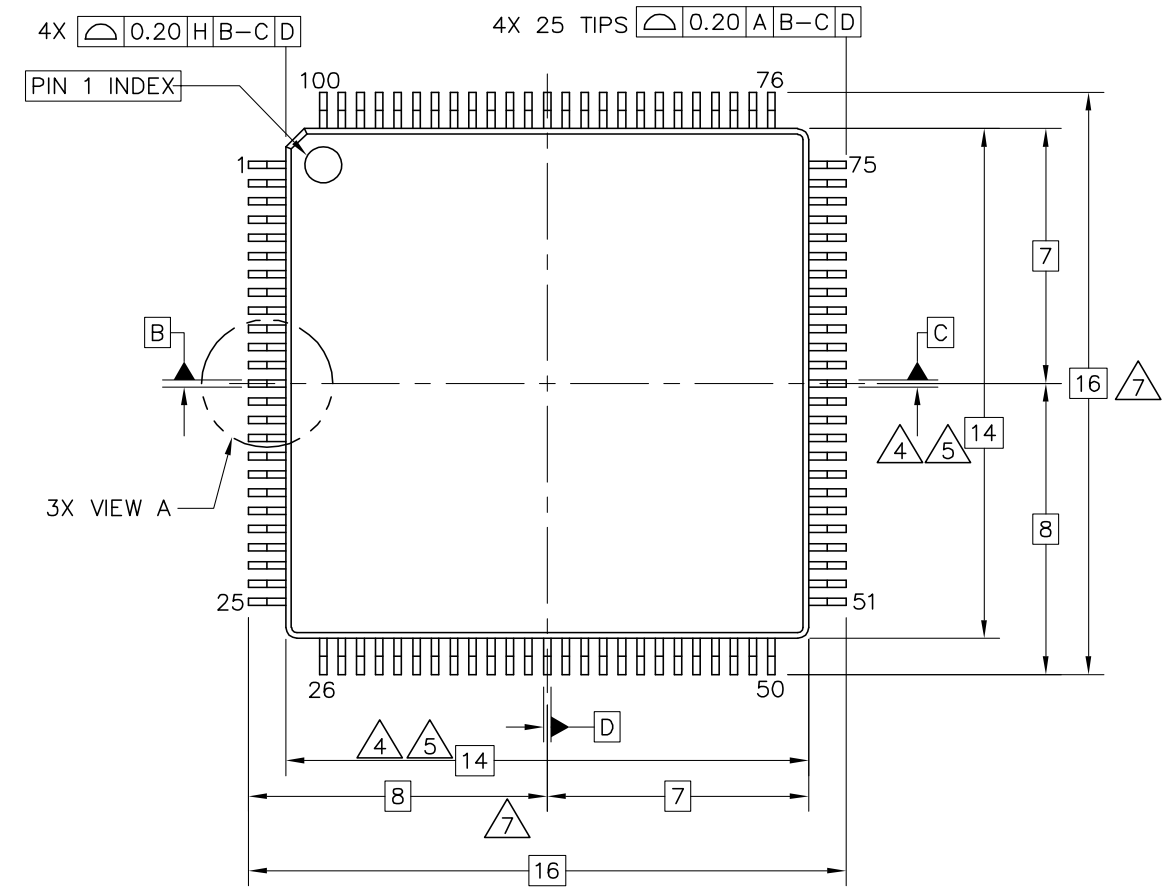
The VDDA, VSSA pin pairs supply the A/D converter and parts of the internal voltage regulator.

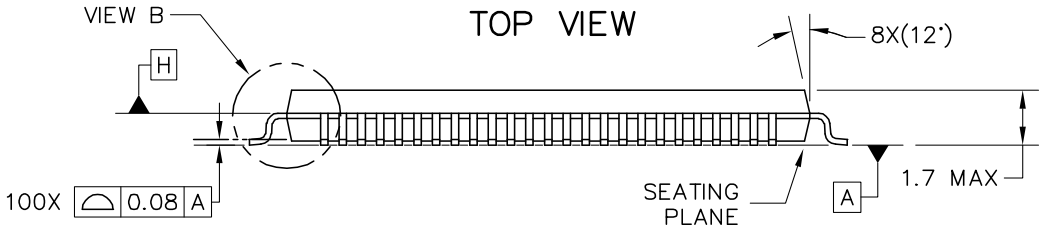
The VDDX, VSSX pin pairs [3:1] supply the I/O pins.

VDDR supplies the internal voltage regulator.

The VDDF, VSS1 pin pair supplies the internal NVM logic.

# D.1 100 LQFP Mechanical Dimensions




SIDE VIEW

| © FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED. | MECHANICAL OUTLINE | PRINT VERSION NOT TO SCALE |
|---|---|---|
| TITLE: 100 LEAD LQFP 14 X 14, 0.5 PITCH, 1.4 THICK | DOCUMENT NO: 98ASS23308W | REV: H |
| | CASE NUMBER: 983–02 | 25 MAY 2005 |
| | STANDARD: NON–JEDEC | |