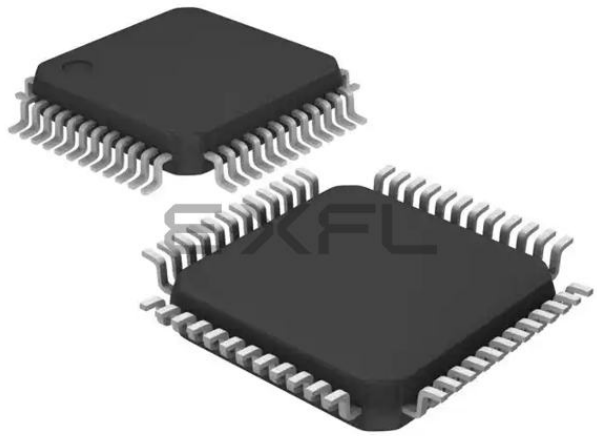

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Product Status	Active
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Connectivity	IrDA, LINbus, SCI, SPI
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Number of I/O	40
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Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	1K x 8
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Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s9s12gn16f0clf

Table 1-21. 64-Pin LQFP Pinout for S12G96 and S12G128

	Function <----lowest-----PRIORITY-----highest---->					Power Supply	Internal Pull Resistor	
Package Pin	**Pin**	**2nd Func.**	**3rd Func.**	**4th Func**	**5th Func**		**CTRL**	**Reset State**
57	PS5	MOSI0	—	—	—	V_{DDX}	PERS/PPSS	Up
58	PS6	SCK0	—	—	—	V_{DDX}	PERS/PPSS	Up
59	PS7	API_EXTCLK	ECLK	$\overline{SS0}$	—	V_{DDX}	PERS/PPSS	Up
60	PM0	RXCAN	—	—	—	V_{DDX}	PERM/PPSM	Disabled
61	PM1	TXCAN	—	—	—	V_{DDX}	PERM/PPSM	Disabled
62	PM2	RXD2	—	—	—	V_{DDX}	PERM/PPSM	Disabled
63	PM3	TXD2	—	—	—	V_{DDX}	PERM/PPSM	Disabled
64	PJ7	KWJ7	$\overline{SS2}$	—	—	V_{DDX}	PERJ/PPSJ	Up

[1] The regular I/O characteristics (see Section A.2, “I/O Characteristics”) apply if the EXTAL/XTAL function is disabled

2.3 PIM Routing - Functional description

Table 2-4. Signals and Priorities

Port	Pin	Signal	Signals per Device and Package (signal priority on pin from top to bottom)																				I/O	Description
			GA240 / GA192	G240 / G192	G128 / GA128 / G96 / GA96	GA240 / GA192	G240 / G192	G128 / GA128 / G96 / GA96	G64 / GA64 / G48 / GA48	GN48	GA240 / GA192	G240 / G192	G128 / GA128 / G96 / GA96	G64 / GA64 / G48 / GA48	GN48	GN32 / GNA32	GN16 / GNA16	G64 / G48	GN48	GN32	GN16	GN32	GN16		
			100			64					48							32				20			
-	BKGD	MODC	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	I	MODC input during RESET
		BKGD	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	I/O	BDM communication
A	PA7-PA0	[PA7:PA0]	?	?	?																		I/O	GPIO
B	PB7-PB6	[PB7:PB6]	?	?	?																		I/O	GPIO
	PB5	$\overline{\text{XIRQ}}$	?	?	?																		I	Non-maskable level-sensitive interrupt
		[PB5]	?	?	?																		I/O	GPIO
	PB4	$\overline{\text{IRQ}}$	?	?	?																		I	Maskable level- or falling-edge sensitive interrupt
		[PB4]	?	?	?																		I/O	GPIO
	PB3	[PB3]	?	?	?																		I/O	GPIO
	PB2	ECLKX2	?	?	?																		O	Free-running clock (ECLK x 2)
		[PB2]	?	?	?																		I/O	GPIO
	PB1	API_EXTCLK	?	?	?																		O	API Clock
		[PB1]	?	?	?																		I/O	GPIO
	PB0	ECLK	?	?	?																		O	Free-running clock
		[PB0]	?	?	?																		I/O	GPIO
C	PC7	DACU1	?																				O	DAC1 output unbuffered
		[PC7]	?	?	?																		I/O	GPIO
	PC6	AMPP1	?																				I	DAC1 non-inv. input (+)
		[PC6]	?	?	?																		I/O	GPIO
	PC5	AMPM1	?																				I	DAC1 inverting input (-)
		[PC5]	?	?	?																		I/O	GPIO
	PC4-PC2	AN15-AN13	?	?																			I	ADC analog
		[PC4:PC2]	?	?	?																		I/O	GPIO
	PC1-PC0	AN11-AN10	?	?																			I	ADC analog
		[PC1:PC0]	?	?	?																		I/O	GPIO
D	PD7-PD0	[PD7:PD0]	?	?	?																		I/O	GPIO

Legend	
?	Signal available on pin
?	Routing option on pin
?	Routing reset location
	Not available on pin

2.4.3.15 Port T Data Register (PTT)

Address 0x0240 (G1, G2) Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	PTT7	PTT6	PTT5	PTT4	PTT3	PTT2	PTT1	PTT0
W								
Reset	0	0	0	0	0	0	0	0

Address 0x0240 (G3) Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	0	0	PTT5	PTT4	PTT3	PTT2	PTT1	PTT0
W								
Reset	0	0	0	0	0	0	0	0

Figure 2-16. Port T Data Register (PTT)

[1] Read: Anytime. The data source is depending on the data direction value.
Write: Anytime

Table 2-35. PTT Register Field Descriptions

Field	Description
7-0 PTT	**Port T general-purpose input/output data**—Data Register When not used with an alternative signal, the associated pin can be used as general-purpose I/O. In general-purpose output mode the port data register bit value is driven to the pin. If the associated data direction bit is set to 1, a read returns the value of the port data register bit, otherwise the buffered pin input state is read.

2.4.3.16 Port T Input Register (PTIT)

Address 0x0241 (G1, G2) Access: User read only[1]

	7	6	5	4	3	2	1	0
R	PTIT7	PTIT6	PTIT5	PTIT4	PTIT3	PTIT2	PTIT1	PTIT0
W								
Reset	0	0	0	0	0	0	0	0

Address 0x0241 (G3) Access: User read only[1]

	7	6	5	4	3	2	1	0
R	0	0	PTIT5	PTIT4	PTIT3	PTIT2	PTIT1	PTIT0
W								
Reset	0	0	0	0	0	0	0	0

Figure 2-17. Port T Input Register (PTIT)

[1] Read: Anytime
Write:Never

7.4.7 Serial Interface Hardware Handshake Protocol

BDM commands that require CPU execution are ultimately treated at the MCU bus rate. Since the BDM clock source can be modified when changing the settings for the VCO frequency (CPMUSYNR), it is very helpful to provide a handshake protocol in which the host could determine when an issued command is executed by the CPU. The BDM clock frequency is always VCO frequency divided by 8. The alternative is to always wait the amount of time equal to the appropriate number of cycles at the slowest possible rate the clock could be running. This sub-section will describe the hardware handshake protocol.

The hardware handshake protocol signals to the host controller when an issued command was successfully executed by the target. This protocol is implemented by a 16 serial clock cycle low pulse followed by a brief speedup pulse in the BKGD pin. This pulse is generated by the target MCU when a command, issued by the host, has been successfully executed (see Figure 7-10). This pulse is referred to as the ACK pulse. After the ACK pulse has finished: the host can start the bit retrieval if the last issued command was a read command, or start a new command if the last command was a write command or a control command (BACKGROUND, GO, GO_UNTIL or TRACE1). The ACK pulse is not issued earlier than 32 serial clock cycles after the BDM command was issued. The end of the BDM command is assumed to be the 16th tick of the last bit. This minimum delay assures enough time for the host to perceive the ACK pulse. Note also that, there is no upper limit for the delay between the command and the related ACK pulse, since the command execution depends upon the CPU bus, which in some cases could be very slow due to long accesses taking place.This protocol allows a great flexibility for the POD designers, since it does not rely on any accurate time measurement or short response time to any event in the serial communication.

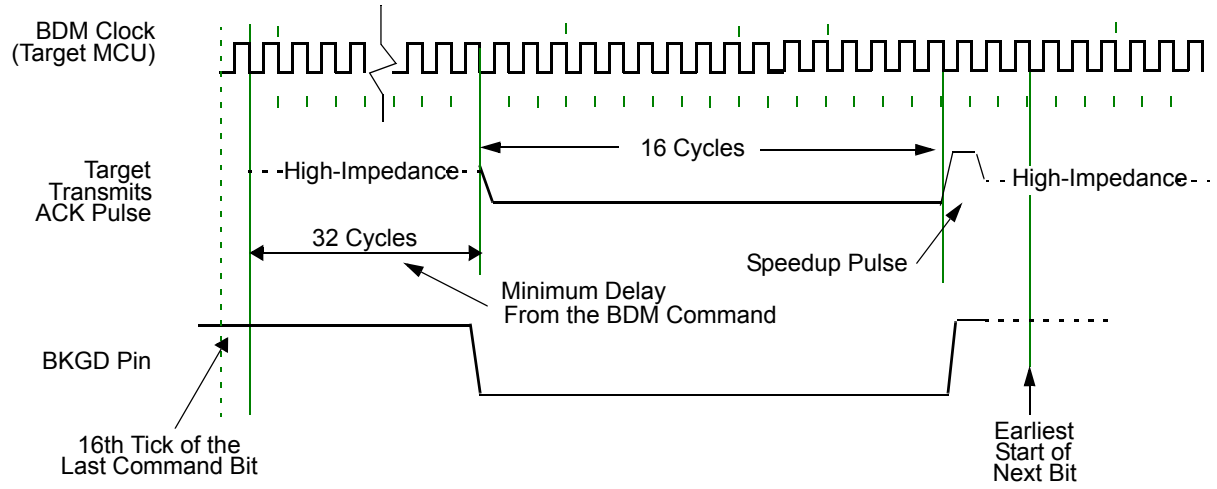

Figure 7-10. Target Acknowledge Pulse (ACK)

NOTE

If the ACK pulse was issued by the target, the host assumes the previous command was executed. If the CPU enters wait or stop prior to executing a hardware command, the ACK pulse will not be issued meaning that the BDM command was not executed. After entering wait or stop mode, the BDM command is no longer pending.

8.3.2.8.5 Debug Comparator Data High Register (DBGADH)

Address: 0x002C

	7	6	5	4	3	2	1	0
R W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Reset	0	0	0	0	0	0	0	0

Figure 8-19. Debug Comparator Data High Register (DBGADH)

Read: If COMRV[1:0] = 00

Write: If COMRV[1:0] = 00 and DBG not armed.

Table 8-28. DBGADH Field Descriptions

Field	Description
7–0 Bits[15:8]	**Comparator Data High Compare Bits**— The Comparator data high compare bits control whether the selected comparator compares the data bus bits [15:8] to a logic one or logic zero. The comparator data compare bits are only used in comparison if the corresponding data mask bit is logic 1. This register is available only for comparator A. Data bus comparisons are only performed if the TAG bit in DBGACTL is clear. 0 Compare corresponding data bit to a logic zero 1 Compare corresponding data bit to a logic one

8.3.2.8.6 Debug Comparator Data Low Register (DBGADL)

Address: 0x002D

	7	6	5	4	3	2	1	0
R W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reset	0	0	0	0	0	0	0	0

Figure 8-20. Debug Comparator Data Low Register (DBGADL)

Read: If COMRV[1:0] = 00

Write: If COMRV[1:0] = 00 and DBG not armed.

Table 8-29. DBGADL Field Descriptions

Field	Description
7–0 Bits[7:0]	**Comparator Data Low Compare Bits** — The Comparator data low compare bits control whether the selected comparator compares the data bus bits [7:0] to a logic one or logic zero. The comparator data compare bits are only used in comparison if the corresponding data mask bit is logic 1. This register is available only for comparator A. Data bus comparisons are only performed if the TAG bit in DBGACTL is clear 0 Compare corresponding data bit to a logic zero 1 Compare corresponding data bit to a logic one

NOTE

A write to this register starts the RTI time-out period. A change of the RTIOSCSEL bit (writing a different value or loosing UPOSC status) re-starts the RTI time-out period.

Table 10-9. CPMURTI Field Descriptions

Field	Description
7 RTDEC	**Decimal or Binary Divider Select Bit** — RTDEC selects decimal or binary based prescaler values. 0 Binary based divider value. See Table 10-10 1 Decimal based divider value. See Table 10-11
6–4 RTR[6:4]	**Real Time Interrupt Prescale Rate Select Bits** — These bits select the prescale rate for the RTI. See Table 10-10 and Table 10-11.
3–0 RTR[3:0]	**Real Time Interrupt Modulus Counter Select Bits** — These bits select the modulus counter target value to provide additional granularity.Table 10-10 and Table 10-11 show all possible divide values selectable by the CPMURTI register**.**

Table 10-10. RTI Frequency Divide Rates for RTDEC = 0

RTR[3:0]	RTR[6:4] =							
	000 (OFF)	**001 (2^{10})**	**010 (2^{11})**	**011 (2^{12})**	**100 (2^{13})**	**101 (2^{14})**	**110 (2^{15})**	**111 (2^{16})**
0000 (÷1)	OFF[1]	2^{10}	2^{11}	2^{12}	2^{13}	2^{14}	2^{15}	2^{16}
0001 (÷2)	OFF	$2x2^{10}$	$2x2^{11}$	$2x2^{12}$	$2x2^{13}$	$2x2^{14}$	$2x2^{15}$	$2x2^{16}$
0010 (÷3)	OFF	$3x2^{10}$	$3x2^{11}$	$3x2^{12}$	$3x2^{13}$	$3x2^{14}$	$3x2^{15}$	$3x2^{16}$
0011 (÷4)	OFF	$4x2^{10}$	$4x2^{11}$	$4x2^{12}$	$4x2^{13}$	$4x2^{14}$	$4x2^{15}$	$4x2^{16}$
0100 (÷5)	OFF	$5x2^{10}$	$5x2^{11}$	$5x2^{12}$	$5x2^{13}$	$5x2^{14}$	$5x2^{15}$	$5x2^{16}$
0101 (÷6)	OFF	$6x2^{10}$	$6x2^{11}$	$6x2^{12}$	$6x2^{13}$	$6x2^{14}$	$6x2^{15}$	$6x2^{16}$
0110 (÷7)	OFF	$7x2^{10}$	$7x2^{11}$	$7x2^{12}$	$7x2^{13}$	$7x2^{14}$	$7x2^{15}$	$7x2^{16}$
0111 (÷8)	OFF	$8x2^{10}$	$8x2^{11}$	$8x2^{12}$	$8x2^{13}$	$8x2^{14}$	$8x2^{15}$	$8x2^{16}$
1000 (÷9)	OFF	$9x2^{10}$	$9x2^{11}$	$9x2^{12}$	$9x2^{13}$	$9x2^{14}$	$9x2^{15}$	$9x2^{16}$
1001 (÷10)	OFF	$10x2^{10}$	$10x2^{11}$	$10x2^{12}$	$10x2^{13}$	$10x2^{14}$	$10x2^{15}$	$10x2^{16}$
1010 (÷11)	OFF	$11x2^{10}$	$11x2^{11}$	$11x2^{12}$	$11x2^{13}$	$11x2^{14}$	$11x2^{15}$	$11x2^{16}$
1011 (÷12)	OFF	$12x2^{10}$	$12x2^{11}$	$12x2^{12}$	$12x2^{13}$	$12x2^{14}$	$12x2^{15}$	$12x2^{16}$
1100 (÷13)	OFF	$13x2^{10}$	$13x2^{11}$	$13x2^{12}$	$13x2^{13}$	$13x2^{14}$	$13x2^{15}$	$13x2^{16}$
1101 (÷14)	OFF	$14x2^{10}$	$14x2^{11}$	$14x2^{12}$	$14x2^{13}$	$14x2^{14}$	$14x2^{15}$	$14x2^{16}$

Chapter 12
Analog-to-Digital Converter (ADC12B8CV2)

Revision History

Version Number	Revision Date	Effective Date	Author	Description of Changes
V02.00	13 May 2009	13 May 2009		Initial version copied from V01.05, changed unused Bits in ATDDIEN to read logic 1
V02.01	17 Dec 2009	17 Dec 2009		Updated Table 12-15 Analog Input Channel Select Coding - description of internal channels. Updated register ATDDR (left/right justified result) description in section 12.3.2.12.1/12-449 and 12.3.2.12.2/12-450 and added Table 12-21 to improve feature description.
V02.02	09 Feb 2010	09 Feb 2010		Fixed typo in Table 12-9 - conversion result for 3mV and 10bit resolution
V02.03	26 Feb 2010	26 Feb 2010		Corrected Table 12-15 Analog Input Channel Select Coding - description of internal channels.
V02.04	14 Apr 2010	14 Apr 2010		Corrected typos to be in-line with SoC level pin naming conventions for VDDA, VSSA, VRL and VRH.
V02.05	25 Aug 2010	25 Aug 2010		Removed feature of conversion during STOP and general wording clean up done in Section 12.4, “Functional Description
V02.06	09 Sep 2010	09 Sep 2010		Update of internal only information.
V02.07	11 Feb 2011	11 Feb 2011		Connectivity Information regarding internal channel_6 added to Table 12-15.
V02.08	22. Jun 2012	22. Jun 2012		Updated register wirte access information in section 12.3.2.9/12-447
V02.09	29. Jun 2012	29 Jun 2012		Removed IP name in block diagram Figure 12-1
V02.10	02 Oct 2012	02 Oct 2012		Added user information to avoid maybe false external trigger events when enabling the external trigger mode (Section 12.4.2.1, “External Trigger Input).

12.1 Introduction

The ADC12B8C is a 8-channel, 12-bit, multiplexed input successive approximation analog-to-digital converter. Refer to device electrical specifications for ATD accuracy.

Chapter 13
Analog-to-Digital Converter (ADC10B12CV2)

Revision History

Version Number	Revision Date	Effective Date	Author	Description of Changes
V02.00	13 May 2009	13 May 2009		Initial version copied from V01.06, changed unused Bits in ATDDIEN to read logic 1
V02.01	30.Nov 2009	30.Nov 2009		Updated Table 13-15 Analog Input Channel Select Coding - description of internal channels. Updated register ATDDR (left/right justified result) description in section 13.3.2.12.1/13-475 and 13.3.2.12.2/13-476 and added table Table 13-21 to improve feature description.
V02.02	09 Feb 2010	09 Feb 2010		Fixed typo in Table 13-9- conversion result for 3mV and 10bit resolution
V02.03	26 Feb 2010	26 Feb 2010		Corrected Table 13-15 Analog Input Channel Select Coding - description of internal channels.
V02.04	14 Apr 2010	14 Apr 2010		Corrected typos to be in-line with SoC level pin naming conventions for VDDA, VSSA, VRL and VRH.
V02.05	25 Aug 2010	25 Aug 2010		Removed feature of conversion during STOP and general wording clean up done in Section 13.4, “Functional Description
V02.06	09 Sep 2010	09 Sep 2010		Update of internal only information.
V02.07	11 Feb 2011	11 Feb 2011		Connectivity Information regarding internal channel_6 added to Table 13-15.
V02.08	29 Mar 2011	29 Mar 2011		Fixed typo in bit description field Table 13-14 for bits CD, CC, CB, CA. Last sentence contained a wrong highest channel number (it is not AN7 to AN0 instead it is AN11 to AN0).
V02.09	22. Jun 2012	22. Jun 2012		Update of register write access information in section 13.3.2.9/13-473.
V02.10	29 Jun 2012	29. Jun 2012		Removed IP name in block diagram Figure 13-1
V02.11	02 Oct 2012	02 Oct 2012		Added user information to avoid maybe false external trigger events when enabling the external trigger mode (Section 13.4.2.1, “External Trigger Input).

14.2 Signal Description

This section lists all inputs to the ADC12B12C block.

14.2.1 Detailed Signal Descriptions

14.2.1.1 AN*x* (*x* = 11, 10, 9, 8, 7, 6, 5, 4, 3, 2, 1, 0)

This pin serves as the analog input Channel *x*. It can also be configured as digital port or external trigger for the ATD conversion.

14.2.1.2 ETRIG3, ETRIG2, ETRIG1, ETRIG0

These inputs can be configured to serve as an external trigger for the ATD conversion.

Refer to device specification for availability and connectivity of these inputs!

14.2.1.3 VRH, VRL

VRH is the high reference voltage, VRL is the low reference voltage for ATD conversion.

14.2.1.4 VDDA, VSSA

These pins are the power supplies for the analog circuitry of the ADC12B12C block.

14.3 Memory Map and Register Definition

This section provides a detailed description of all registers accessible in the ADC12B12C.

14.3.1 Module Memory Map

Figure 14-2 gives an overview on all ADC12B12C registers.

NOTE

Register Address = Base Address + Address Offset, where the Base Address is defined at the MCU level and the Address Offset is defined at the module level.

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0000	ATDCTL0	R W	Reserved	0	0	0	WRAP3	WRAP2	WRAP1	WRAP0
0x0001	ATDCTL1	R W	ETRIGSEL	SRES1	SRES0	SMP_DIS	ETRIGCH3	ETRIGCH2	ETRIGCH1	ETRIGCH0
0x0002	ATDCTL2	R W	0	AFFC	Reserved	ETRIGLE	ETRIGP	ETRIGE	ASCIE	ACMPIE

= Unimplemented or Reserved

Figure 14-2. ADC12B12C Register Summary (Sheet 1 of 3)

16.3.2 Register Descriptions

This section describes in address order all the ADC12B16C registers and their individual bits.

16.3.2.1 ATD Control Register 0 (ATDCTL0)

Writes to this register will abort current conversion sequence.

Module Base + 0x0000

	7	6	5	4	3	2	1	0
R	Reserved	0	0	0	WRAP3	WRAP2	WRAP1	WRAP0
W								
Reset	0	0	0	0	1	1	1	1

= Unimplemented or Reserved

Figure 16-3. ATD Control Register 0 (ATDCTL0)

Read: Anytime

Write: Anytime, in special modes always write 0 to Reserved Bit 7.

Table 16-1. ATDCTL0 Field Descriptions

Field	Description
3-0 WRAP[3-0]	**Wrap Around Channel Select Bits** — These bits determine the channel for wrap around when doing multi-channel conversions. The coding is summarized in Table 16-2.

Table 16-2. Multi-Channel Wrap Around Coding

WRAP3	WRAP2	WRAP1	WRAP0	Multiple Channel Conversions (MULT = 1) Wraparound to AN0 after Converting
0	0	0	0	Reserved[1]
0	0	0	1	AN1
0	0	1	0	AN2
0	0	1	1	AN3
0	1	0	0	AN4
0	1	0	1	AN5
0	1	1	0	AN6
0	1	1	1	AN7
1	0	0	0	AN8
1	0	0	1	AN9
1	0	1	0	AN10
1	0	1	1	AN11
1	1	0	0	AN12
1	1	0	1	AN13
1	1	1	0	AN14
1	1	1	1	AN15

16.3.2.9 ATD Status Register 2 (ATDSTAT2)

This read-only register contains the Conversion Complete Flags CCF[15:0].

Module Base + 0x000A

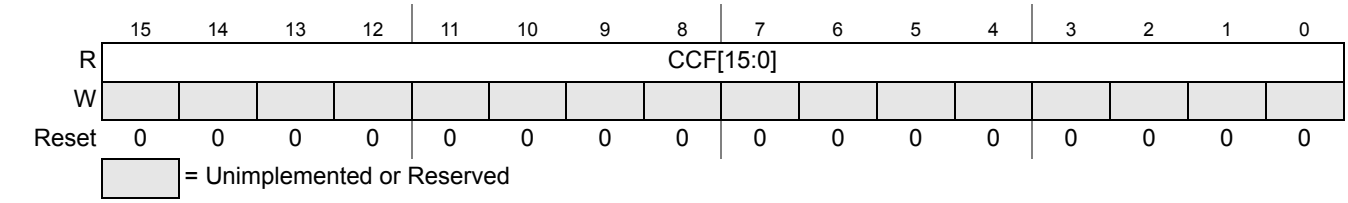

Figure 16-11. ATD Status Register 2 (ATDSTAT2)

Read: Anytime

Write: Anytime (for details see Table 16-18 below)

Table 16-18. ATDSTAT2 Field Descriptions

Field	Description
15–0 CCF[15:0]	**Conversion Complete Flag *n* (*n*= 15, 14, 13, 12, 11, 10, 9, 8, 7, 6, 5, 4, 3, 2, 1, 0) (*n conversion number, NOT channel number!)*—** A conversion complete flag is set at the end of each conversion in a sequence. The flags are associated with the conversion position in a sequence (and also the result register number). Therefore in non-fifo mode, CCF[4] is set when the fifth conversion in a sequence is complete and the result is available in result register ATDDR4; CCF[5] is set when the sixth conversion in a sequence is complete and the result is available in ATDDR5, and so forth. If automatic compare of conversion results is enabled (CMPE[*n*]=1 in ATDCMPE), the conversion complete flag is only set if comparison with ATDDR*n* is true. If ACMPIE=1 a compare interrupt will be requested. In this case, as the ATDDR*n* result register is used to hold the compare value, the result will not be stored there at the end of the conversion but is lost. A flag CCF[*n*] is cleared when one of the following occurs: A) Write to ATDCTL5 (a new conversion sequence is started) B) If AFFC=0, write “1” to CCF[*n*] C) If AFFC=1 and CMPE[*n*]=0, read of result register ATDDR*n* D) If AFFC=1 and CMPE[*n*]=1, write to result register ATDDR*n* In case of a concurrent set and clear on CCF[*n*]: The clearing by method A) will overwrite the set. The clearing by methods B) or C) or D) will be overwritten by the set. 0 Conversion number *n* not completed or successfully compared 1 If (CMPE[*n*]=0): Conversion number *n* has completed. Result is ready in ATDDR*n*. If (CMPE[*n*]=1): Compare for conversion result number *n* with compare value in ATDDR*n*, using compare operator CMPGT[*n*] is true. (No result available in ATDDR*n*)

18.5 Initialization/Application Information

18.5.1 MSCAN initialization

The procedure to initially start up the MSCAN module out of reset is as follows:

1. Assert CANE
2. Write to the configuration registers in initialization mode
3. Clear INITRQ to leave initialization mode

If the configuration of registers which are only writable in initialization mode shall be changed:

1. Bring the module into sleep mode by setting SLPRQ and awaiting SLPAK to assert after the CAN bus becomes idle.
2. Enter initialization mode: assert INITRQ and await INITAK
3. Write to the configuration registers in initialization mode
4. Clear INITRQ to leave initialization mode and continue

18.5.2 Bus-Off Recovery

The bus-off recovery is user configurable. The bus-off state can either be left automatically or on user request.

For reasons of backwards compatibility, the MSCAN defaults to automatic recovery after reset. In this case, the MSCAN will become error active again after counting 128 occurrences of 11 consecutive recessive bits on the CAN bus (see the Bosch CAN 2.0 A/B specification for details).

If the MSCAN is configured for user request (BORM set in MSCAN Control Register 1 (CANCTL1)), the recovery from bus-off starts after both independent events have become true:

- 128 occurrences of 11 consecutive recessive bits on the CAN bus have been monitored
- BOHOLD in MSCAN Miscellaneous Register (CANMISC) has been cleared by the user

These two events may occur in any order.

Any access to TCNT will clear TFLG2 register if the TFFCA bit in TSCR register is set.

Table 23-17. TRLG2 Field Descriptions

Field	Description
7 TOF	**Timer Overflow Flag** — Set when 16-bit free-running timer overflows from 0xFFFF to 0x0000. Clearing this bit requires writing a one to bit 7 of TFLG2 register while the TEN bit of TSCR1 or PAEN bit of PACTL is set to one (See also TCRE control bit explanation) .

23.3.2.14 Timer Input Capture/Output Compare Registers High and Low 0–7(TCxH and TCxL)

Module Base + 0x0010 = TC0H 0x0018=TC4H
0x0012 = TC1H 0x001A=TC5H
0x0014=TC2H 0x001C=TC6H
0x0016=TC3H 0x001E=TC7H

	15	14	13	12	11	10	9	0
R W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Reset	0	0	0	0	0	0	0	0

Figure 23-22. Timer Input Capture/Output Compare Register x High (TCxH)

Module Base + 0x0011 = TC0L 0x0019 =TC4L
0x0013 = TC1L 0x001B=TC5L
0x0015 =TC2L 0x001D=TC6L
0x0017=TC3L 0x001F=TC7L

	7	6	5	4	3	2	1	0
R W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reset	0	0	0	0	0	0	0	0

Figure 23-23. Timer Input Capture/Output Compare Register x Low (TCxL)

[1] This register is available only when the corresponding channel exists and is reserved if that channel does not exist. Writes to a reserved register have no functional effect. Reads from a reserved register return zeroes.

Depending on the TIOS bit for the corresponding channel, these registers are used to latch the value of the free-running counter when a defined transition is sensed by the corresponding input capture edge detector or to trigger an output action for output compare.

Read: Anytime

Write: Anytime for output compare function.Writes to these registers have no meaning or effect during input capture. All timer input capture/output compare registers are reset to 0x0000.

NOTE

Read/Write access in byte mode for high byte should take place before low byte otherwise it will give a different result.

CAUTION

A Flash word or phrase must be in the erased state before being programmed. Cumulative programming of bits within a Flash word or phrase is not allowed.

The Flash memory may be read as bytes and aligned words. Read access time is one bus cycle for bytes and aligned words. For misaligned words access, the CPU has to perform twice the byte read access command. For Flash memory, an erased bit reads 1 and a programmed bit reads 0.

It is possible to read from P-Flash memory while some commands are executing on EEPROM memory. It is not possible to read from EEPROM memory while a command is executing on P-Flash memory. Simultaneous P-Flash and EEPROM operations are discussed in Section 29.4.5.

Both P-Flash and EEPROM memories are implemented with Error Correction Codes (ECC) that can resolve single bit faults and detect double bit faults. For P-Flash memory, the ECC implementation requires that programming be done on an aligned 8 byte basis (a Flash phrase). Since P-Flash memory is always read by half-phrase, only one single bit fault in an aligned 4 byte half-phrase containing the byte or word accessed will be corrected.

29.1.1 Glossary

Command Write Sequence — An MCU instruction sequence to execute built-in algorithms (including program and erase) on the Flash memory.

EEPROM Memory — The EEPROM memory constitutes the nonvolatile memory store for data.

EEPROM Sector — The EEPROM sector is the smallest portion of the EEPROM memory that can be erased. The EEPROM sector consists of 4 bytes.

NVM Command Mode — An NVM mode using the CPU to setup the FCCOB register to pass parameters required for Flash command execution.

Phrase — An aligned group of four 16-bit words within the P-Flash memory. Each phrase includes two sets of aligned double words with each set including 7 ECC bits for single bit fault correction and double bit fault detection within each double word.

P-Flash Memory — The P-Flash memory constitutes the main nonvolatile memory store for applications.

P-Flash Sector — The P-Flash sector is the smallest portion of the P-Flash memory that can be erased. Each P-Flash sector contains 512 bytes.

Program IFR — Nonvolatile information register located in the P-Flash block that contains the Version ID, and the Program Once field.

Table 29-25. FOPT Field Descriptions

Field	Description
7–0 NV[7:0]	**Nonvolatile Bits** — The NV[7:0] bits are available as nonvolatile bits. Refer to the device user guide for proper use of the NV bits.

29.3.2.17 Flash Reserved5 Register (FRSV5)

This Flash register is reserved for factory testing.

Offset Module Base + 0x0011

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 29-23. Flash Reserved5 Register (FRSV5)

All bits in the FRSV5 register read 0 and are not writable.

29.3.2.18 Flash Reserved6 Register (FRSV6)

This Flash register is reserved for factory testing.

Offset Module Base + 0x0012

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 29-24. Flash Reserved6 Register (FRSV6)

All bits in the FRSV6 register read 0 and are not writable.

29.3.2.19 Flash Reserved7 Register (FRSV7)

This Flash register is reserved for factory testing.

Table 30-15. FSTAT Field Descriptions (continued)

Field	Description
3 MGBUSY	**Memory Controller Busy Flag** — The MGBUSY flag reflects the active state of the Memory Controller. 0 Memory Controller is idle 1 Memory Controller is busy executing a Flash command (CCIF = 0)
2 RSVD	**Reserved Bit** — This bit is reserved and always reads 0.
1–0 MGSTAT[1:0]	**Memory Controller Command Completion Status Flag** — One or more MGSTAT flag bits are set if an error is detected during execution of a Flash command or during the Flash reset sequence. See Section 30.4.6, “Flash Command Description,” and Section 30.6, “Initialization” for details.

30.3.2.8 Flash Error Status Register (FERSTAT)

The FERSTAT register reflects the error status of internal Flash operations.

Offset Module Base + 0x0007

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	DFDIF	SFDIF
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 30-12. Flash Error Status Register (FERSTAT)

All flags in the FERSTAT register are readable and only writable to clear the flag.

Table 30-16. FERSTAT Field Descriptions

Field	Description
1 DFDIF	**Double Bit Fault Detect Interrupt Flag** — The setting of the DFDIF flag indicates that a double bit fault was detected in the stored parity and data bits during a Flash array read operation or that a Flash array read operation returning invalid data was attempted on a Flash block that was under a Flash command operation.[1] The DFDIF flag is cleared by writing a 1 to DFDIF. Writing a 0 to DFDIF has no effect on DFDIF.[2] 0 No double bit fault detected 1 Double bit fault detected or a Flash array read operation returning invalid data was attempted while command running
0 SFDIF	**Single Bit Fault Detect Interrupt Flag** — With the IGNSF bit in the FCNFG register clear, the SFDIF flag indicates that a single bit fault was detected in the stored parity and data bits during a Flash array read operation or that a Flash array read operation returning invalid data was attempted on a Flash block that was under a Flash command operation.[1] The SFDIF flag is cleared by writing a 1 to SFDIF. Writing a 0 to SFDIF has no effect on SFDIF. 0 No single bit fault detected 1 Single bit fault detected and corrected or a Flash array read operation returning invalid data was attempted while command running

1 The single bit fault and double bit fault flags are mutually exclusive for parity errors (an ECC fault occurrence can be either single fault or double fault but never both). A simultaneous access collision (Flash array read operation returning invalid data attempted while command running) is indicated when both SFDIF and DFDIF flags are high.

2 There is a one cycle delay in storing the ECC DFDIF and SFDIF fault flags in this register. At least one NOP is required after a flash memory read before checking FERSTAT for the occurrence of ECC errors.

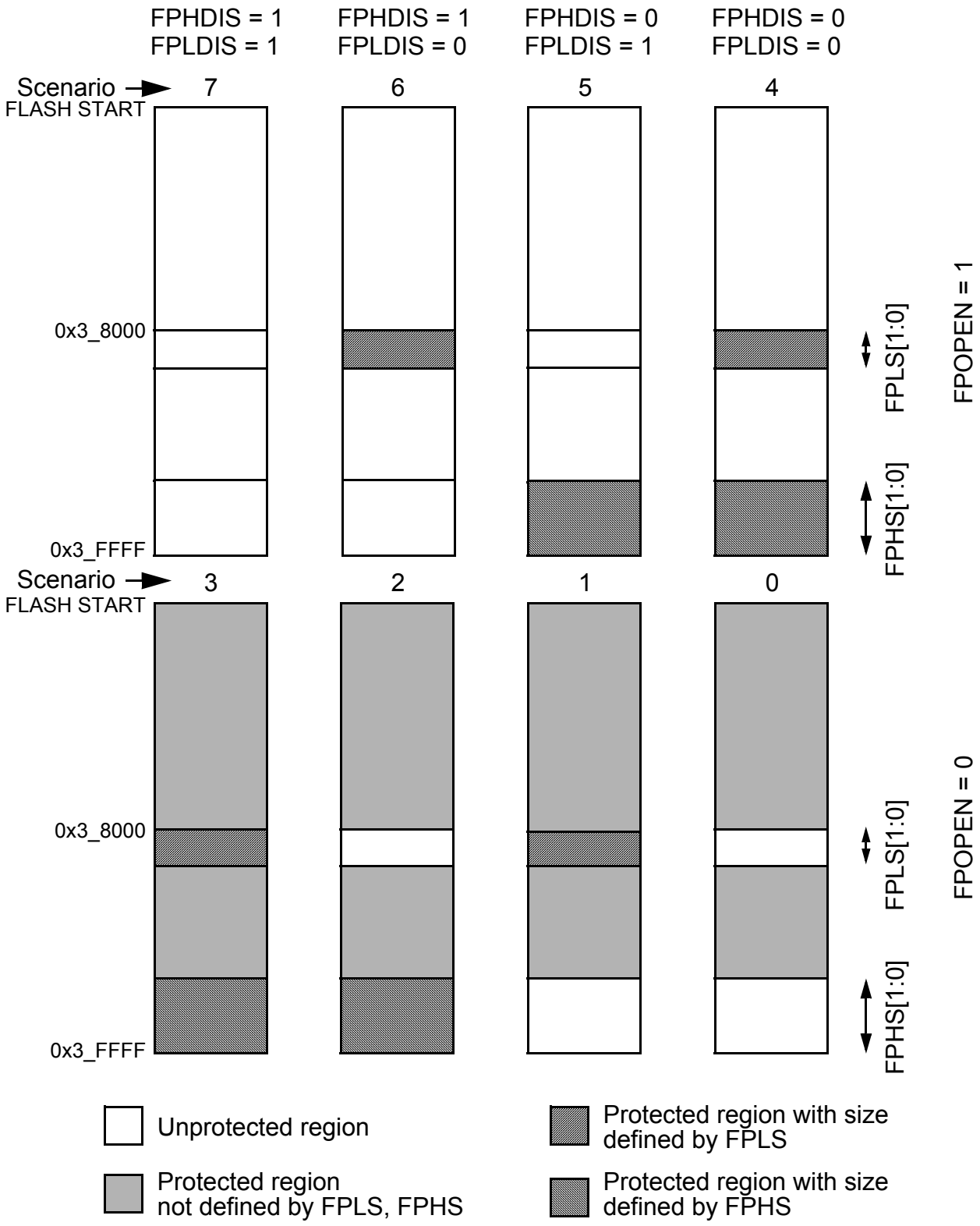

Figure 30-14. P-Flash Protection Scenarios

Upon clearing CCIF to launch the Read Once command, a Read Once phrase is fetched and stored in the FCCOB indexed register. The CCIF flag will set after the Read Once operation has completed. Valid phrase index values for the Read Once command range from 0x0000 to 0x0007. During execution of the Read Once command, any attempt to read addresses within P-Flash block will return invalid data.

Table 30-39. Read Once Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 001 at command launch
		Set if command not available in current mode (see Table 30-27)
		Set if an invalid phrase index is supplied
	FPVIOL	None
	MGSTAT1	Set if any errors have been encountered during the read
	MGSTAT0	Set if any non-correctable errors have been encountered during the read

30.4.6.5 Program P-Flash Command

The Program P-Flash operation will program a previously erased phrase in the P-Flash memory using an embedded algorithm.

CAUTION

A P-Flash phrase must be in the erased state before being programmed. Cumulative programming of bits within a Flash phrase is not allowed.

Table 30-40. Program P-Flash Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x06	Global address [17:16] to identify P-Flash block
001	Global address [15:0] of phrase location to be programmed[1]	
010	Word 0 program value	
011	Word 1 program value	
100	Word 2 program value	
101	Word 3 program value	

[1] Global address [2:0] must be 000

Upon clearing CCIF to launch the Program P-Flash command, the Memory Controller will program the data words to the supplied global address and will then proceed to verify the data words read back as expected. The CCIF flag will set after the Program P-Flash operation has completed.

sequence. If CCIF is 0, the previous command write sequence is still active, a new command write sequence cannot be started, and all writes to the FCCOB register are ignored.

31.4.4.2.1 Define FCCOB Contents

The FCCOB parameter fields must be loaded with all required parameters for the Flash command being executed. Access to the FCCOB parameter fields is controlled via the CCOBIX bits in the FCCOBIX register (see Section 31.3.2.3).

The contents of the FCCOB parameter fields are transferred to the Memory Controller when the user clears the CCIF command completion flag in the FSTAT register (writing 1 clears the CCIF to 0). The CCIF flag will remain clear until the Flash command has completed. Upon completion, the Memory Controller will return CCIF to 1 and the FCCOB register will be used to communicate any results. The flow for a generic command write sequence is shown in Figure 31-26.

A.8.2 Electrical Characteristics for the PLL

Table A-40. PLL Characteristics

Conditions are shown in Table A-15 unless otherwise noted							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	D	VCO frequency during system reset	f_{VCORST}	8		25	MHz
2	C	VCO locking range	f_{VCO}	32		50	MHz
3	C	Reference Clock	f_{REF}	1			MHz
4	D	Lock Detection	$\|\Delta_{Lock}\|$	0		1.5	%[1]
5	D	Un-Lock Detection	$\|\Delta_{unl}\|$	0.5		2.5	%[1]
6	C	Time to lock	t_{lock}			150 + $256/f_{REF}$	µs
7	C	Jitter fit parameter 1[2] IRC as reference clock source	j_{irc}			1.4	%
8	C	Jitter fit parameter 1[3] XOSCLCP as reference clock source	j_{ext}			1.0	%

1 % deviation from target frequency

2 f_{REF} = 1MHz (IRC), f_{BUS} = 25MHz equivalent f_{PLL} = 50MHz, CPMUSYNR=0x58, CPMUREFDIV=0x00, CPMUPOSTDIV=0x00

3 f_{REF} = 4MHz (XOSCLCP), f_{BUS} = 24MHz equivalent f_{PLL} = 48MHz, CPMUSYNR=0x05, CPMUREFDIV=0x40, CPMUPOSTDIV=0x00

A.9 Electrical Characteristics for the IRC1M

Table A-41. IRC1M Characteristics (Junction Temperature From –40°C To +150°C, all packages)

Conditions are: Temperature option C, V, or M (see Table A-4)							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	P	Internal Reference Frequency, factory trimmed	f_{IRC1M_TRIM}	0.987	1	1.013	MHz

Table A-42. IRC1M Characteristics (Junction Temperature From –40°C To +150°C, KGD)

Conditions are: Temperature option C, V, or M (see Table A-4)							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	P	Internal Reference Frequency, factory trimmed	f_{IRC1M_TRIM}	0.980	1	1.020	MHz