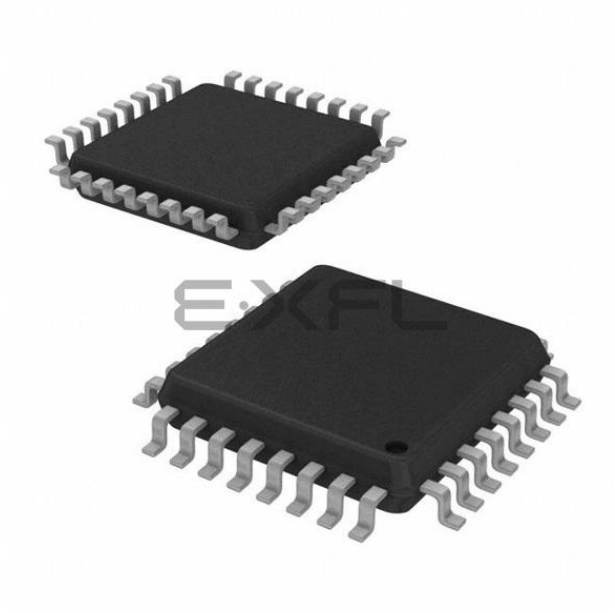

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	12V1
Core Size	16-Bit
Speed	25MHz
Connectivity	IrDA, LINbus, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	26
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	3.13V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s9s12gn16f1mlc

Table 1-2. Maximum Peripheral Availability per Package

Peripheral	20 TSSOP	32 LQFP	48 QFN	48 LQFP	64 LQFP	100 LQFP	KGD (Die)
DAC0	—	—	—	Yes	Yes	Yes	Yes
DAC1	—	—	—	Yes	Yes	Yes	Yes
ACMP	Yes	Yes	Yes	Yes	Yes	—	—
Total GPIO	14	26	40	40	54	86	86

1.2.2 Chip-Level Features

On-chip modules available within the family include the following features:

- S12 CPU core
- Up to 240 Kbyte on-chip flash with ECC
- Up to 4 Kbyte EEPROM with ECC
- Up to 11 Kbyte on-chip SRAM
- Phase locked loop (IPLL) frequency multiplier with internal filter
- 4–16 MHz amplitude controlled Pierce oscillator
- 1 MHz internal RC oscillator
- Timer module (TIM) supporting up to eight channels that provide a range of 16-bit input capture, output compare, counter, and pulse accumulator functions
- Pulse width modulation (PWM) module with up to eight x 8-bit channels
- Up to 16-channel, 10 or 12-bit resolution successive approximation analog-to-digital converter (ADC)
- Up to two 8-bit digital-to-analog converters (DAC)
- Up to one 5V analog comparator (ACMP)
- Up to three serial peripheral interface (SPI) modules
- Up to three serial communication interface (SCI) modules supporting LIN communications
- Up to one multi-scalable controller area network (MSCAN) module (supporting CAN protocol 2.0A/B)
- On-chip voltage regulator (VREG) for regulation of input supply and all internal voltages
- Autonomous periodic interrupt (API)
- Precision fixed voltage reference for ADC conversions
- Optional reference voltage attenuator module to increase ADC accuracy

1.3 Module Features

The following sections provide more details of the modules implemented on the MC9S12G-Family family.

Table 1-16. 48-Pin LQFP Pinout for S12G48 and S12G64

	Function <----lowest-----PRIORITY-----highest---->					Power Supply	Internal Pull Resistor	
Package Pin	Pin	2nd Func.	3rd Func.	4th Func	5th Func		CTRL	Reset State
3	VSSX	—	—	—	—	—	—	—
4	PE0[1]	EXTAL	—	—	—	V_{DDX}	PUCR/PDPEE	Down
5	VSS	—	—	—	—	—	—	—
6	PE1[1]	XTAL	—	—	—	V_{DDX}	PUCR/PDPEE	Down
7	TEST	—	—	—	—	N.A.	$\overline{\text{RESET}}$ pin	Down
8	PJ0	KWJ0	—	MISO1	—	V_{DDX}	PERJ/PPSJ	Up
9	PJ1	KWJ1	—	MOSI1	—	V_{DDX}	PERJ/PPSJ	Up
10	PJ2	KWJ2	—	SCK1	—	V_{DDX}	PERJ/PPSJ	Up
11	PJ3	KWJ3	—	$\overline{\text{SS1}}$	—	V_{DDX}	PERJ/PPSJ	Up
12	BKGD	MODC	—	—	—	V_{DDX}	PUCR/BKPUE	Up
13	PP0	KWP0	ETRIG0	API_EXTCLK	PWM0	V_{DDX}	PERP/PPSP	Disabled
14	PP1	KWP1	ETRIG1	ECLKX2	PWM1	V_{DDX}	PERP/PPSP	Disabled
15	PP2	KWP2	ETRIG2	PWM2	—	V_{DDX}	PERP/PPSP	Disabled
16	PP3	KWP3	ETRIG3	PWM3	—	V_{DDX}	PERP/PPSP	Disabled
17	PP4	KWP4	PWM4	—	—	V_{DDX}	PERP/PPSP	Disabled
18	PP5	KWP5	PWM5	—	—	V_{DDX}	PERP/PPSP	Disabled
19	PT5	IOC5	—	—	—	V_{DDX}	PERT/PPST	Disabled
20	PT4	IOC4	—	—	—	V_{DDX}	PERT/PPST	Disabled
21	PT3	IOC3	—	—	—	V_{DDX}	PERT/PPST	Disabled
22	PT2	IOC2	—	—	—	V_{DDX}	PERT/PPST	Disabled
23	PT1	IOC1	$\overline{\text{IRQ}}$	—	—	V_{DDX}	PERT/PPST	Disabled
24	PT0	IOC0	$\overline{\text{XIRQ}}$	—	—	V_{DDX}	PERT/PPST	Disabled
25	PAD0	KWAD0	AN0	—	—	V_{DDA}	PER1AD/PPS1AD	Disabled
26	PAD8	KWAD8	AN8	—	—	V_{DDA}	PER0AD/PPS0AD	Disabled
27	PAD1	KWAD1	AN1	—	—	V_{DDA}	PER1AD/PPS1AD	Disabled
28	PAD9	KWAD9	AN9	ACMPO	—	V_{DDA}	PER0AD/PPS0AD	Disabled
29	PAD2	KWAD2	AN2	—	—	V_{DDA}	PER1AD/PPS1AD	Disabled
30	PAD10	KWAD10	AN10	ACMPP		V_{DDA}	PER0AD/PPS0AD	Disabled

Table 1-26. 48-Pin LQFP Pinout for S12G192 and S12G240

	Function <----lowest-----PRIORITY-----highest---->					Power Supply	Internal Pull Resistor	
Package Pin	Pin	2nd Func.	3rd Func.	4th Func	5th Func		CTRL	Reset State
2	VDDXR	—	—	—	—	—	—	—
3	VSSX	—	—	—	—	—	—	—
4	PE0[1]	EXTAL	—	—	—	V_{DDX}	PUCR/PDPEE	Down
5	VSS	—	—	—	—	—	—	—
6	PE1[1]	XTAL	—	—	—	V_{DDX}	PUCR/PDPEE	Down
7	TEST	—	—	—	—	N.A.	$\overline{\text{RESET}}$ pin	Down
8	PJ0	KWJ0	PWM6	MISO1	—	V_{DDX}	PERJ/PPSJ	Up
9	PJ1	KWJ1	IOC6	MOSI1	—	V_{DDX}	PERJ/PPSJ	Up
10	PJ2	KWJ2	IOC7	SCK1	—	V_{DDX}	PERJ/PPSJ	Up
11	PJ3	KWJ3	PWM7	$\overline{\text{SS1}}$	—	V_{DDX}	PERJ/PPSJ	Up
12	BKGD	MODC	—	—	—	V_{DDX}	PUCR/BKPUE	Up
13	PP0	KWP0	ETRIG0	API_EXTCLK	PWM0	V_{DDX}	PERP/PPSP	Disabled
14	PP1	KWP1	ETRIG1	ECLKX2	PWM1	V_{DDX}	PERP/PPSP	Disabled
15	PP2	KWP2	ETRIG2	PWM2	—	V_{DDX}	PERP/PPSP	Disabled
16	PP3	KWP3	ETRIG3	PWM3	—	V_{DDX}	PERP/PPSP	Disabled
17	PP4	KWP4	PWM4	—	—	V_{DDX}	PERP/PPSP	Disabled
18	PP5	KWP5	PWM5	—	—	V_{DDX}	PERP/PPSP	Disabled
19	PT5	IOC5	—	—	—	V_{DDX}	PERT/PPST	Disabled
20	PT4	IOC4	—	—	—	V_{DDX}	PERT/PPST	Disabled
21	PT3	IOC3	—	—	—	V_{DDX}	PERT/PPST	Disabled
22	PT2	IOC2	—	—	—	V_{DDX}	PERT/PPST	Disabled
23	PT1	IOC1	$\overline{\text{IRQ}}$	—	—	V_{DDX}	PERT/PPST	Disabled
24	PT0	IOC0	$\overline{\text{XIRQ}}$	—	—	V_{DDX}	PERT/PPST	Disabled
25	PAD0	KWAD0	AN0	—	—	V_{DDA}	PER1AD/PPS1AD	Disabled
26	PAD8	KWAD8	AN8	—	—	V_{DDA}	PER0AD/PPS0AD	Disabled
27	PAD1	KWAD1	AN1	—	—	V_{DDA}	PER1AD/PPS1AD	Disabled
28	PAD9	KWAD9	AN9	—	—	V_{DDA}	PER0AD/PPS0AD	Disabled
29	PAD2	KWAD2	AN2	—	—	V_{DDA}	PER1AD/PPS1AD	Disabled

Table 2-18. Block Memory Map (0x0000-0x027F) (continued)

Port	Global Address	Register	Access	Reset Value	Section/Page
T	0x0240	PTT—Port T Data Register	R/W	0x00	2.4.3.15/2-207
	0x0241	PTIT—Port T Input Register	R	[3]	2.4.3.16/2-207
	0x0242	DDRT—Port T Data Direction Register	R/W	0x00	2.4.3.17/2-208
	0x0243	Reserved	R	0x00	
	0x0244	PERT—Port T Pull Device Enable Register	R/W	0x00	2.4.3.18/2-209
	0x0245	PPST—Port T Polarity Select Register	R/W	0x00	2.4.3.19/2-210
	0x0246	Reserved	R	0x00	
	0x0247	Reserved	R	0x00	
S	0x0248	PTS—Port S Data Register	R/W	0x00	2.4.3.20/2-210
	0x0249	PTIS—Port S Input Register	R	[3]	2.4.3.21/2-211
	0x024A	DDRS—Port S Data Direction Register	R/W	0x00	2.4.3.22/2-211
	0x024B	Reserved	R	0x00	
	0x024C	PERS—Port S Pull Device Enable Register	R/W	0xFF	2.4.3.23/2-212
	0x024D	PPSS—Port S Polarity Select Register	R/W	0x00	2.4.3.24/2-212
	0x024E	WOMS—Port S Wired-Or Mode Register	R/W	0x00	2.4.3.25/2-213
	0x024F	PRR0—Pin Routing Register 0[4]	R/W	0x00	2.4.3.26/2-213
M	0x0250	PTM—Port M Data Register	R/W	0x00	2.4.3.27/2-215
	0x0251	PTIM—Port M Input Register	R	[3]	2.4.3.29/2-216
	0x0252	DDRM—Port M Data Direction Register	R/W	0x00	2.4.3.29/2-216
	0x0253	Reserved	R	0x00	
	0x0254	PERM—Port M Pull Device Enable Register	R/W	0x00	2.4.3.30/2-217
	0x0255	PPSM—Port M Polarity Select Register	R/W	0x00	2.4.3.31/2-218
	0x0256	WOMM—Port M Wired-Or Mode Register	R/W	0x00	2.4.3.32/2-218
	0x0257	PKGCR—Package Code Register	R/W	[5]	2.4.3.33/2-219
P	0x0258	PTP—Port P Data Register	R/W	0x00	2.4.3.34/2-220
	0x0259	PTIP—Port P Input Register	R	[3]	2.4.3.35/2-221
	0x025A	DDRP—Port P Data Direction Register	R/W	0x00	2.4.3.36/2-222
	0x025B	Reserved	R	0x00	
	0x025C	PERP—Port P Pull Device Enable Register	R/W	0x00	2.4.3.37/2-222
	0x025D	PPSP—Port P Polarity Select Register	R/W	0x00	2.4.3.38/2-223
	0x025E	PIEP—Port P Interrupt Enable Register	R/W	0x00	2.4.3.39/2-224
	0x025F	PIFP—Port P Interrupt Flag Register	R/W	0x00	2.4.3.40/2-224

Table 2-64. PERP Register Field Descriptions

Field	Description
7-0 PERP	**Port P pull device enable**—Enable pull device on input pin This bit controls whether a pull device on the associated port input pin is active. If a pin is used as output this bit has no effect. The polarity is selected by the related polarity select register bit. 1 Pull device enabled 0 Pull device disabled

2.4.3.38 Port P Polarity Select Register (PPSP)

Address 0x025D (G1, G2) Access: User read/write[1]

	7	6	5	4	3	2	1	0
R W	PPSP7	PPSP6	PPSP5	PPSP4	PPSP3	PPSP2	PPSP1	PPSP0
Reset	0	0	0	0	0	0	0	0

Address 0x025D (G3) Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	0	0	PPSP5	PPSP4	PPSP3	PPSP2	PPSP1	PPSP0
W								
Reset	0	0	0	0	0	0	0	0

Figure 2-39. Port P Polarity Select Register (PPSP)

[1] Read: Anytime
Write: Anytime

Table 2-65. PPSP Register Field Descriptions

Field	Description
7-0 PPSP	**Port P pull device select**—Configure pull device and pin interrupt edge polarity on input pin This bit selects a pullup or a pulldown device if enabled on the associated port input pin. This bit also selects the polarity of the active pin interrupt edge. 1 Pulldown device selected; rising edge selected 0 Pullup device selected; falling edge selected

21.3.2.3 SPI Baud Rate Register (SPIBR)

Module Base +0x0002

	7	6	5	4	3	2	1	0
R	0	SPPR2	SPPR1	SPPR0	0	SPR2	SPR1	SPR0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 21-5. SPI Baud Rate Register (SPIBR)

Read: Anytime

Write: Anytime; writes to the reserved bits have no effect

Table 21-5. SPIBR Field Descriptions

Field	Description
6–4 SPPR[2:0]	**SPI Baud Rate Preselection Bits** — These bits specify the SPI baud rates as shown in Table 21-6. In master mode, a change of these bits will abort a transmission in progress and force the SPI system into idle state.
2–0 SPR[2:0]	**SPI Baud Rate Selection Bits** — These bits specify the SPI baud rates as shown in Table 21-6. In master mode, a change of these bits will abort a transmission in progress and force the SPI system into idle state.

The baud rate divisor equation is as follows:

$$\text{BaudRateDivisor} = (\text{SPPR} + 1) \bullet 2^{(\text{SPR} + 1)} \qquad \textit{Eqn. 21-1}$$

The baud rate can be calculated with the following equation:

$$\text{Baud Rate} = \text{BusClock} / \text{BaudRateDivisor} \qquad \textit{Eqn. 21-2}$$

NOTE

For maximum allowed baud rates, please refer to the SPI Electrical Specification in the Electricals chapter of this data sheet.

Table 21-6. Example SPI Baud Rate Selection (25 MHz Bus Clock)

SPPR2	SPPR1	SPPR0	SPR2	SPR1	SPR0	Baud Rate Divisor	Baud Rate
0	0	0	0	0	0	2	12.5 Mbit/s
0	0	0	0	0	1	4	6.25 Mbit/s
0	0	0	0	1	0	8	3.125 Mbit/s
0	0	0	0	1	1	16	1.5625 Mbit/s
0	0	0	1	0	0	32	781.25 kbit/s
0	0	0	1	0	1	64	390.63 kbit/s
0	0	0	1	1	0	128	195.31 kbit/s
0	0	0	1	1	1	256	97.66 kbit/s
0	0	1	0	0	0	4	6.25 Mbit/s
0	0	1	0	0	1	8	3.125 Mbit/s

Chapter 22
Timer Module (TIM16B6CV3)

Table 22-1. Revision History

V03.00	Jan. 28, 2009		Initial version
V03.01	Aug. 26, 2009	22.1.2/22-720 22.3.2.2/22-723, 22.4.3/22-735	- Correct typo: TSCR ->TSCR1; - Correct typo: ECTxxx->TIMxxx - Add description, “a counter overflow when TTOV[7] is set”, to be the condition of channel 7 override event. - Phrase the description of OC7M to make it more explicit
V03.02	Apri,12,2010	22.3.2.6/22-726 22.3.2.9/22-728 22.4.3/22-735	-update TCRE bit description
V03.03	Jan,14,2013		-single source generate different channel guide

22.1 Introduction

The basic scalable timer consists of a 16-bit, software-programmable counter driven by a flexible programmable prescaler.

This timer can be used for many purposes, including input waveform measurements while simultaneously generating an output waveform.

This timer could contain up to 6 input capture/output compare channels . The input capture function is used to detect a selected transition edge and record the time. The output compare function is used for generating output signals or for timer software delays.

A full access for the counter registers or the input capture/output compare registers should take place in one clock cycle. Accessing high byte and low byte separately for all of these registers may not yield the same result as accessing them in one word.

22.1.1 Features

The TIM16B6CV3 includes these distinctive features:

- Up to 6 channels available. (refer to device specification for exact number)
- All channels have same input capture/output compare functionality.
- Clock prescaling.
- 16-bit counter.

The security function in the Flash module is described in Section 24.5.

24.3.2.3 Flash CCOB Index Register (FCCOBIX)

The FCCOBIX register is used to index the FCCOB register for Flash memory operations.

Offset Module Base + 0x0002

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	CCOBIX[2:0]		
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 24-7. FCCOB Index Register (FCCOBIX)

CCOBIX bits are readable and writable while remaining bits read 0 and are not writable.

Table 24-12. FCCOBIX Field Descriptions

Field	Description
2–0 CCOBIX[1:0]	**Common Command Register Index**— The CCOBIX bits are used to select which word of the FCCOB register array is being read or written to. See 24.3.2.11 Flash Common Command Object Register (FCCOB),” for more details.

24.3.2.4 Flash Reserved0 Register (FRSV0)

This Flash register is reserved for factory testing.

Offset Module Base + 0x000C

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 24-8. Flash Reserved0 Register (FRSV0)

All bits in the FRSV0 register read 0 and are not writable.

24.3.2.5 Flash Configuration Register (FCNFG)

The FCNFG register enables the Flash command complete interrupt and forces ECC faults on Flash array read access from the CPU.

Table 24-44. Erase Flash Block Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x09	Global address [17:16] to identify Flash block
001	Global address [15:0] in Flash block to be erased	

Upon clearing CCIF to launch the Erase Flash Block command, the Memory Controller will erase the selected Flash block and verify that it is erased. The CCIF flag will set after the Erase Flash Block operation has completed.

Table 24-45. Erase Flash Block Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 001 at command launch
		Set if command not available in current mode (see Table 24-25)
		Set if an invalid global address [17:16] is supplied[1]
		Set if the supplied P-Flash address is not phrase-aligned or if the EEPROM address is not word-aligned
	FPVIOL	Set if an area of the selected Flash block is protected
	MGSTAT1	Set if any errors have been encountered during the verify operation[2]
	MGSTAT0	Set if any non-correctable errors have been encountered during the verify operation[2]

1 As defined by the memory map for FTMRG32K1.

2 As found in the memory map for FTMRG32K1.

24.4.6.9 Erase P-Flash Sector Command

The Erase P-Flash Sector operation will erase all addresses in a P-Flash sector.

Table 24-46. Erase P-Flash Sector Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x0A	Global address [17:16] to identify P-Flash block to be erased
001	Global address [15:0] anywhere within the sector to be erased. Refer to Section 24.1.2.1 for the P-Flash sector size.	

Upon clearing CCIF to launch the Erase P-Flash Sector command, the Memory Controller will erase the selected Flash sector and then verify that it is erased. The CCIF flag will be set after the Erase P-Flash Sector operation has completed.

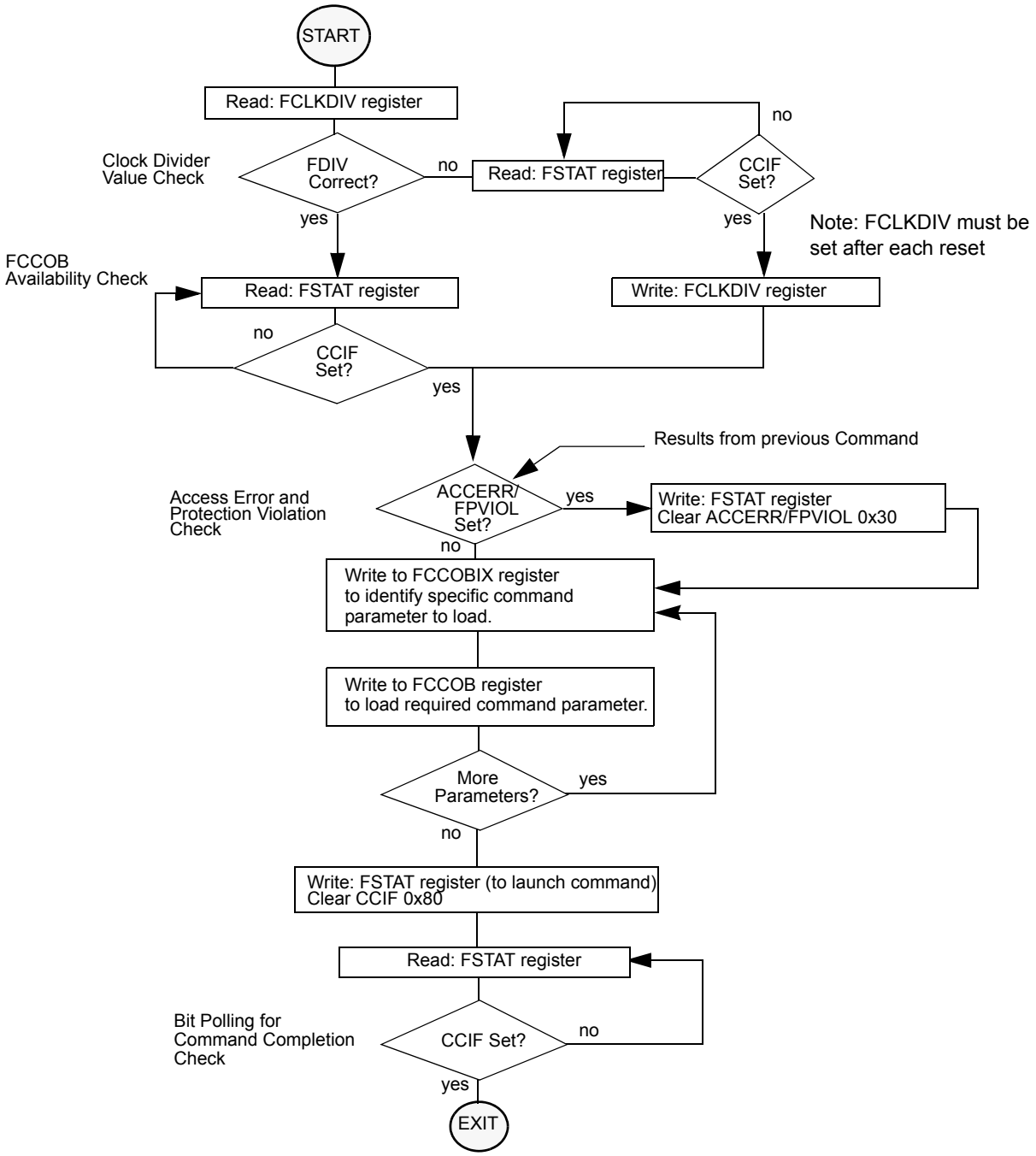

Figure 25-26. Generic Flash Command Write Sequence Flowchart

Table 25-41. Program P-Flash Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 101 at command launch
		Set if command not available in current mode (see Table 25-27)
		Set if an invalid global address [17:0] is supplied see Table 25-3)
		Set if a misaligned phrase address is supplied (global address [2:0] != 000)
	FPVIOL	Set if the global address [17:0] points to a protected area
	MGSTAT1	Set if any errors have been encountered during the verify operation
	MGSTAT0	Set if any non-correctable errors have been encountered during the verify operation

25.4.6.6 Program Once Command

The Program Once command restricts programming to a reserved 64 byte field (8 phrases) in the nonvolatile information register located in P-Flash. The Program Once reserved field can be read using the Read Once command as described in Section 25.4.6.4. The Program Once command must only be issued once since the nonvolatile information register in P-Flash cannot be erased. The Program Once command must not be executed from the Flash block containing the Program Once reserved field to avoid code runaway.

Table 25-42. Program Once Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x07	Not Required
001	Program Once phrase index (0x0000 - 0x0007)	
010	Program Once word 0 value	
011	Program Once word 1 value	
100	Program Once word 2 value	
101	Program Once word 3 value	

Upon clearing CCIF to launch the Program Once command, the Memory Controller first verifies that the selected phrase is erased. If erased, then the selected phrase will be programmed and then verified with read back. The CCIF flag will remain clear, setting only after the Program Once operation has completed.

The reserved nonvolatile information register accessed by the Program Once command cannot be erased and any attempt to program one of these phrases a second time will not be allowed. Valid phrase index values for the Program Once command range from 0x0000 to 0x0007. During execution of the Program Once command, any attempt to read addresses within P-Flash will return invalid data.

Table 25-49. Erase P-Flash Sector Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 001 at command launch
		Set if command not available in current mode (see Table 25-27)
		Set if an invalid global address [17:16] is supplied see Table 25-3)[1]
		Set if a misaligned phrase address is supplied (global address [2:0] != 000)
	FPVIOL	Set if the selected P-Flash sector is protected
	MGSTAT1	Set if any errors have been encountered during the verify operation
	MGSTAT0	Set if any non-correctable errors have been encountered during the verify operation

1 As defined by the memory map for FTMRG32K1.

25.4.6.10 Unsecure Flash Command

The Unsecure Flash command will erase the entire P-Flash and EEPROM memory space and, if the erase is successful, will release security.

Table 25-50. Unsecure Flash Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x0B	Not required

Upon clearing CCIF to launch the Unsecure Flash command, the Memory Controller will erase the entire P-Flash and EEPROM memory space and verify that it is erased. If the Memory Controller verifies that the entire Flash memory space was properly erased, security will be released. If the erase verify is not successful, the Unsecure Flash operation sets MGSTAT1 and terminates without changing the security state. During the execution of this command (CCIF=0) the user must not write to any Flash module register. The CCIF flag is set after the Unsecure Flash operation has completed.

Table 25-51. Unsecure Flash Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 000 at command launch
		Set if command not available in current mode (see Table 25-27)
	FPVIOL	Set if any area of the P-Flash or EEPROM memory is protected
	MGSTAT1	Set if any errors have been encountered during the verify operation
	MGSTAT0	Set if any non-correctable errors have been encountered during the verify operation

25.4.6.11 Verify Backdoor Access Key Command

The Verify Backdoor Access Key command will only execute if it is enabled by the KEYEN bits in the FSEC register (see Table 25-10). The Verify Backdoor Access Key command releases security if

Table 26-19. P-Flash Protection Higher Address Range

FPHS[1:0]	Global Address Range	Protected Size
00	0x3_F800–0x3_FFFF	2 Kbytes
01	0x3_F000–0x3_FFFF	4 Kbytes
10	0x3_E000–0x3_FFFF	8 Kbytes
11	0x3_C000–0x3_FFFF	16 Kbytes

Table 26-20. P-Flash Protection Lower Address Range

FPLS[1:0]	Global Address Range	Protected Size
00	0x3_8000–0x3_83FF	1 Kbyte
01	0x3_8000–0x3_87FF	2 Kbytes
10	0x3_8000–0x3_8FFF	4 Kbytes
11	0x3_8000–0x3_9FFF	8 Kbytes

All possible P-Flash protection scenarios are shown in Figure 26-14 . Although the protection scheme is loaded from the Flash memory at global address 0x3_FF0C during the reset sequence, it can be changed by the user. The P-Flash protection scheme can be used by applications requiring reprogramming in single chip mode while providing as much protection as possible if reprogramming is not required.

26.4.6.2 Erase Verify Block Command

The Erase Verify Block command allows the user to verify that an entire P-Flash or EEPROM block has been erased. The FCCOB FlashBlockSelectionCode[1:0] bits determine which block must be verified.

Table 26-33. Erase Verify Block Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x02	Flash block selection code [1:0]. See Table 26-34

Table 26-34. Flash block selection code description

Selection code[1:0]	Flash block to be verified
00	EEPROM
01	Invalid (ACCERR)
10	Invalid (ACCERR)
11	P-Flash

Upon clearing CCIF to launch the Erase Verify Block command, the Memory Controller will verify that the selected P-Flash or EEPROM block is erased. The CCIF flag will set after the Erase Verify Block operation has completed.If the block is not erased, it means blank check failed, both MGSTAT bits will be set.

Table 26-35. Erase Verify Block Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 000 at command launch
		Set if an invalid FlashBlockSelectionCode[1:0] is supplied
	FPVIOL	None
	MGSTAT1	Set if any errors have been encountered during the read or if blank check failed.
	MGSTAT0	Set if any non-correctable errors have been encountered during the read or if blank check failed.

26.4.6.3 Erase Verify P-Flash Section Command

The Erase Verify P-Flash Section command will verify that a section of code in the P-Flash memory is erased. The Erase Verify P-Flash Section command defines the starting point of the code to be verified and the number of phrases.

28.4.6.3 Erase Verify P-Flash Section Command

The Erase Verify P-Flash Section command will verify that a section of code in the P-Flash memory is erased. The Erase Verify P-Flash Section command defines the starting point of the code to be verified and the number of phrases.

Table 28-36. Erase Verify P-Flash Section Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x03	Global address [17:16] of a P-Flash block
001	Global address [15:0] of the first phrase to be verified	
010	Number of phrases to be verified	

Upon clearing CCIF to launch the Erase Verify P-Flash Section command, the Memory Controller will verify the selected section of Flash memory is erased. The CCIF flag will set after the Erase Verify P-Flash Section operation has completed. If the section is not erased, it means blank check failed, both MGSTAT bits will be set.

Table 28-37. Erase Verify P-Flash Section Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 010 at command launch
		Set if command not available in current mode (see Table 28-27)
		Set if an invalid global address [17:0] is supplied see Table 28-3)[1]
		Set if a misaligned phrase address is supplied (global address [2:0] != 000)
		Set if the requested section crosses a the P-Flash address boundary
	FPVIOL	None
	MGSTAT1	Set if any errors have been encountered during the read[2] or if blank check failed.
	MGSTAT0	Set if any non-correctable errors have been encountered during the read[2] or if blank check failed.

1 As defined by the memory map for FTMRG96K1.

2 As found in the memory map for FTMRG96K1.

28.4.6.4 Read Once Command

The Read Once command provides read access to a reserved 64 byte field (8 phrases) located in the nonvolatile information register of P-Flash. The Read Once field is programmed using the Program Once command described in Section 28.4.6.6. The Read Once command must not be executed from the Flash block containing the Program Once reserved field to avoid code runaway.

Table 28-38. Read Once Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x04	Not Required

28.4.6.8 Erase Flash Block Command

The Erase Flash Block operation will erase all addresses in a P-Flash or EEPROM block.

Table 28-46. Erase Flash Block Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x09	Global address [17:16] to identify Flash block
001	Global address [15:0] in Flash block to be erased	

Upon clearing CCIF to launch the Erase Flash Block command, the Memory Controller will erase the selected Flash block and verify that it is erased. The CCIF flag will set after the Erase Flash Block operation has completed.

Table 28-47. Erase Flash Block Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 001 at command launch
		Set if command not available in current mode (see Table 28-27)
		Set if an invalid global address [17:16] is supplied[1]
		Set if the supplied P-Flash address is not phrase-aligned or if the EEPROM address is not word-aligned
	FPVIOL	Set if an area of the selected Flash block is protected
	MGSTAT1	Set if any errors have been encountered during the verify operation[2]
	MGSTAT0	Set if any non-correctable errors have been encountered during the verify operation[2]

1 As defined by the memory map for FTMRG96K1.

2 As found in the memory map for FTMRG96K1.

28.4.6.9 Erase P-Flash Sector Command

The Erase P-Flash Sector operation will erase all addresses in a P-Flash sector.

Table 28-48. Erase P-Flash Sector Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x0A	Global address [17:16] to identify P-Flash block to be erased
001	Global address [15:0] anywhere within the sector to be erased. Refer to Section 28.1.2.1 for the P-Flash sector size.	

Upon clearing CCIF to launch the Erase P-Flash Sector command, the Memory Controller will erase the selected Flash sector and then verify that it is erased. The CCIF flag will be set after the Erase P-Flash Sector operation has completed.

Table 29-5. Program IFR Fields

Global Address	Size (Bytes)	Field Description
0x0_40B8 – 0x0_40BF	8	Reserved
0x0_40C0 – 0x0_40FF	64	Program Once Field Refer to Section 29.4.6.6, “Program Once Command”

1 Used to track firmware patch versions, see Section 29.4.2

Table 29-6. Memory Controller Resource Fields (NVMRES[1]=1)

Global Address	Size (Bytes)	Description
0x0_4000 – 0x040FF	256	P-Flash IFR (see Table 29-5)
0x0_4100 – 0x0_41FF	256	Reserved.
0x0_4200 – 0x0_57FF		Reserved
0x0_5800 – 0x0_59FF	512	Reserved
0x0_5A00 – 0x0_5FFF	1,536	Reserved
0x0_6000 – 0x0_6BFF	3,072	Reserved
0x0_6C00 – 0x0_7FFF	5,120	Reserved

1 NVMRES - See Section 29.4.3 for NVMRES (NVM Resource) detail.

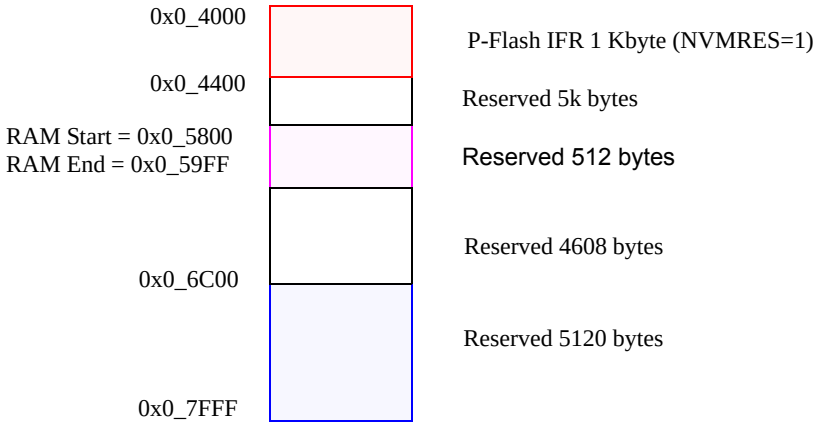

Figure 29-3. Memory Controller Resource Memory Map (NVMRES=1)

Address & Name		7	6	5	4	3	2	1	0
0x000A FCCOBHI	R	CCOB15	CCOB14	CCOB13	CCOB12	CCOB11	CCOB10	CCOB9	CCOB8
	W								
0x000B FCCOBLO	R	CCOB7	CCOB6	CCOB5	CCOB4	CCOB3	CCOB2	CCOB1	CCOB0
	W								
0x000C FRSV1	R	0	0	0	0	0	0	0	0
	W								
0x000D FRSV2	R	0	0	0	0	0	0	0	0
	W								
0x000E FRSV3	R	0	0	0	0	0	0	0	0
	W								
0x000F FRSV4	R	0	0	0	0	0	0	0	0
	W								
0x0010 FOPT	R	NV7	NV6	NV5	NV4	NV3	NV2	NV1	NV0
	W								
0x0011 FRSV5	R	0	0	0	0	0	0	0	0
	W								
0x0012 FRSV6	R	0	0	0	0	0	0	0	0
	W								
0x0013 FRSV7	R	0	0	0	0	0	0	0	0
	W								

= Unimplemented or Reserved

Figure 29-4. FTMRG128K1 Register Summary (continued)

29.3.2.1 Flash Clock Divider Register (FCLKDIV)

The FCLKDIV register is used to control timed events in program and erase algorithms.

Table A-21. ADC Conversion Performance 5V range (Junction Temperature From –40°C To +150°C)

S12GNA16, S12GNA32, S12GAS48, S12GA64, S12GA96, S12GA128, S12GA192 and S12GA240								
Supply voltage 4.5V < V_{DDA} < 5.5 V, -40°C < T_J < 150°C, V_{REF} = V_{RH} - V_{RL} = V_{DDA}, f_{ADCCLK} = 8.0MHz The values are tested to be valid with no port AD output drivers switching simultaneous with conversions.								
Num	**C**	**Rating**[1]		**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	P	Resolution	12-Bit	LSB		1.25		mV
2	P	Differential Nonlinearity	12-Bit	DNL	-4	±2	4	counts
3	P	Integral Nonlinearity	12-Bit	INL	-5	±2.5	5	counts
4	P	Absolute Error[2]	12-Bit	AE	-7	±4	7	counts
5	C	Resolution	10-Bit	LSB		5		mV
6	C	Differential Nonlinearity	10-Bit	DNL	-1	±0.5	1	counts
7	C	Integral Nonlinearity	10-Bit	INL	-2	±1	2	counts
8	C	Absolute Error[2]	10-Bit	AE	-3	±2	3	counts
9	C	Resolution	8-Bit	LSB		20		mV
10	C	Differential Nonlinearity	8-Bit	DNL	-0.5	±0.3	0.5	counts
11	C	Integral Nonlinearity	8-Bit	INL	-1	±0.5	1	counts
12	C	Absolute Error[2]	8-Bit	AE	-1.5	±1	1.5	counts

1 The 8-bit and 10-bit mode operation is structurally tested in production test. Absolute values are tested in 12-bit mode.

2 These values include the quantization error which is inherently 1/2 count for any A/D converter.

0x00A0–0x0C7 Pulse-Width-Modulator (PWM)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x00A0	PWME	R	PWME7	PWME6	PWME5	PWME4	PWME3	PWME2	PWME1	PWME0
		W								
0x00A1	PWMPOL	R	PPOL7	PPOL6	PPOL5	PPOL4	PPOL3	PPOL2	PPOL1	PPOL0
		W								
0x00A2	PWMCLK	R	PCLK7	PCLKL6	PCLK5	PCLK4	PCLK3	PCLK2	PCLK1	PCLK0
		W								
0x00A3	PWMPRCLK	R	0	PCKB2	PCKB1	PCKB0	0	PCKA2	PCKA1	PCKA0
		W								
0x00A4	PWMCAE	R	CAE7	CAE6	CAE5	CAE4	CAE3	CAE2	CAE1	CAE0
		W								
0x00A5	PWMCTL	R	CON67	CON45	CON23	CON01	PSWAI	PFRZ	0	0
		W								
0x00A6	PWMCLKAB	R	PCLKAB7	PCLKAB6	PCLKAB5	PCLKAB4	PCLKAB3	PCLKAB2	PCLKAB1	PCLKAB0
		W								
0x00A7	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x00A8	PWMSCLA	R	Bit 7	6	5	4	3	2	1	Bit 0
		W								
0x00A9	PWMSCLB	R	Bit 7	6	5	4	3	2	1	Bit 0
		W								
0x00AA - 0x00AB	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x00AC	PWMCNT0	R	Bit 7	6	5	4	3	2	1	Bit 0
		W	0	0	0	0	0	0	0	0
0x00AD	PWMCNT1	R	Bit 7	6	5	4	3	2	1	Bit 0
		W	0	0	0	0	0	0	0	0
0x00AE	PWMCNT2	R	Bit 7	6	5	4	3	2	1	Bit 0
		W	0	0	0	0	0	0	0	0
0x00AF	PWMCNT3	R	Bit 7	6	5	4	3	2	1	Bit 0
		W	0	0	0	0	0	0	0	0
0x0B0	PWMCNT4	R	Bit 7	6	5	4	3	2	1	Bit 0
		W	0	0	0	0	0	0	0	0
0x00B1	PWMCNT5	R	Bit 7	6	5	4	3	2	1	Bit 0
		W	0	0	0	0	0	0	0	0
0x00B2	PWMCNT6	R	Bit 7	6	5	4	3	2	1	Bit 0
		W	0	0	0	0	0	0	0	0
0x00B3	PWMCNT7	R	Bit 7	6	5	4	3	2	1	Bit 0
		W	0	0	0	0	0	0	0	0
0x00B4	PWMPER0	R	Bit 7	6	5	4	3	2	1	Bit 0
		W								
0x00B5	PWMPER1	R	Bit 7	6	5	4	3	2	1	Bit 0
		W								
0x00B6	PWMPER2	R	Bit 7	6	5	4	3	2	1	Bit 0
		W								