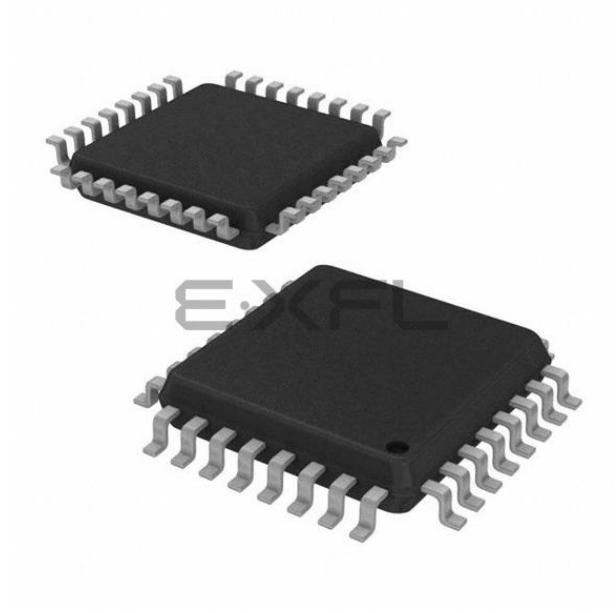

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	12V1
Core Size	16-Bit
Speed	25MHz
Connectivity	IrDA, LINbus, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	26
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	3.13V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s9s12gn16f1vlc

Chapter 1
Device Overview MC9S12G-Family

1.7.2.6 PA[7:0] — Port A I/O Signals

PA[7:0] are general-purpose input or output signals. The signals can have pull-up devices, enabled by a single control bit for this signal group. Out of reset the pull-up devices are disabled .

1.7.2.7 PB[7:0] — Port B I/O Signals

PB[7:0] are general-purpose input or output signals. The signals can have pull-up devices, enabled by a single control bit for this signal group. Out of reset the pull-up devices are disabled .

1.7.2.8 PC[7:0] — Port C I/O Signals

PC[7:0] are general-purpose input or output signals. The signals can have pull-up devices, enabled by a single control bit for this signal group. Out of reset the pull-up devices are disabled .

1.7.2.9 PD[7:0] — Port D I/O Signals

PD[7:0] are general-purpose input or output signals. The signals can have pull-up device, enabled by a single control bit for this signal group. Out of reset the pull-up devices are disabled.

1.7.2.10 PE[1:0] — Port E I/O Signals

PE[1:0] are general-purpose input or output signals. The signals can have pull-down device, enabled by a single control bit for this signal group. Out of reset the pull-down devices are enabled.

1.7.2.11 PJ[7:0] / KWJ[7:0] — Port J I/O Signals

PJ[7:0] are general-purpose input or output signals. The signals can be configured on per signal basis as interrupt inputs with wakeup capability (KWJ[7:0]). They can have a pull-up or pull-down device selected and enabled on per signal basis. Out of reset the pull devices are enabled .

1.7.2.12 PM[3:0] — Port M I/O Signals

PM[3:0] are general-purpose input or output signals. They can have a pull-up or pull-down device selected and enabled on per signal basis. Out of reset the pull devices are disabled. The signals can be configured on per pin basis to open-drain mode.

1.7.2.13 PP[7:0] / KWP[7:0] — Port P I/O Signals

PP[7:0] are general-purpose input or output signals. The signals can be configured on per signal basis as interrupt inputs with wakeup capability (KWP[7:0]). They can have a pull-up or pull-down device selected and enabled on per signal basis. Out of reset the pull devices are disabled .

1.7.2.14 PS[7:0] — Port S I/O Signals

PS[7:0] are general-purpose input or output signals. They can have a pull-up or pull-down device selected and enabled on per signal basis. Out of reset the pull-up devices are enabled. The signals can be configured on per pin basis in open-drain mode.

1.8.4.2 Pinout 48-Pin LQFP

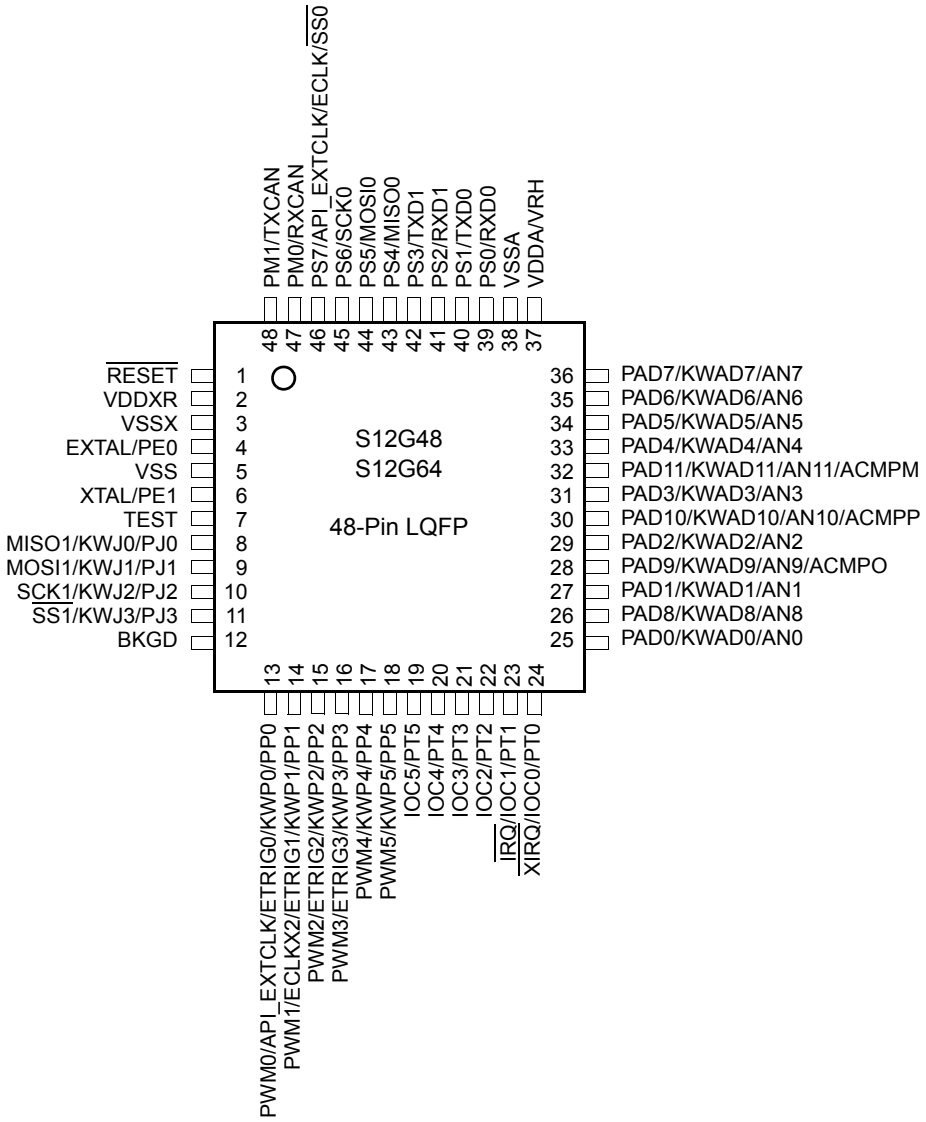

Figure 1-11. 48-Pin LQFP Pinout for S12G48 and S12G64

Table 1-16. 48-Pin LQFP Pinout for S12G48 and S12G64

	Function <----lowest-----PRIORITY-----highest---->					Power Supply	Internal Pull Resistor	
Package Pin	Pin	2nd Func.	3rd Func.	4th Func	5th Func		CTRL	Reset State
1	RESET	—	—	—	—	V_{DDX}	PULLUP	
2	VDDXR	—	—	—	—	—	—	—

2.4.3.41 Reserved Registers

NOTE

Addresses 0x0260-0x0261 are reserved for ACMP registers in G2 and G3 only. Refer to ACMP section “ACMP Control Register (ACMPC)” and “ACMP Status Register (ACMPS)”.

2.4.3.42 Port J Data Register (PTJ)

Address 0x0268 (G1, G2) Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	PTJ7	PTJ6	PTJ5	PTJ4	PTJ3	PTJ2	PTJ1	PTJ0
W								
Reset	0	0	0	0	0	0	0	0

Address 0x0268 (G3) Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	0	0	0	0	PTJ3	PTJ2	PTJ1	PTJ0
W								
Reset	0	0	0	0	0	0	0	0

Figure 2-42. Port J Data Register (PTJ)

[1] Read: Anytime. The data source is depending on the data direction value.
Write: Anytime

Table 2-68. PTJ Register Field Descriptions

Field	Description
7-0 PTJ	**Port J general-purpose input/output data**—Data Register When not used with an alternative signal, the associated pin can be used as general-purpose I/O. In general-purpose output mode the port data register bit value is driven to the pin. If the associated data direction bit is set to 1, a read returns the value of the port data register bit, otherwise the buffered pin input state is read.

5.3.2.4 Program Page Index Register (PPAGE)

Address: 0x0015

	7	6	5	4	3	2	1	0
R	0	0	0	0	PIX3	PIX2	PIX1	PIX0
W								
Reset	0	0	0	0	1	1	1	0

Figure 5-8. Program Page Index Register (PPAGE)

Read: Anytime

Write: Anytime

The four index bits of the PPAGE register select a 16K page in the global memory map (Figure 5-11). The selected 16K page is mapped into the paging window ranging from local address 0x8000 to 0xBFFF. Figure 5-9 illustrates the translation from local to global addresses for accesses to the paging window. The CPU has special access to read and write this register directly during execution of CALL and RTC instructions.

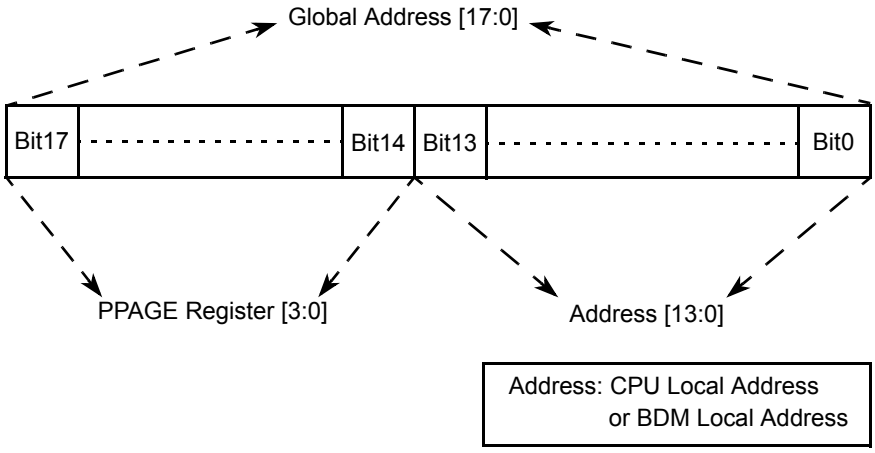

Figure 5-9. PPAGE Address Mapping

NOTE

Writes to this register using the special access of the CALL and RTC instructions will be complete before the end of the instruction execution.

Table 5-7. PPAGE Field Descriptions

Field	Description
3–0 PIX[3:0]	**Program Page Index Bits 3–0** — These page index bits are used to select which of the 256 flash array pages is to be accessed in the Program Page Window.

The fixed 16KB page from 0x0000 to 0x3FFF is the page number 0xC. Parts of this page are covered by Registers, EEPROM and RAM space. See SoC Guide for details.

The fixed 16KB page from 0x4000–0x7FFF is the page number 0xD.

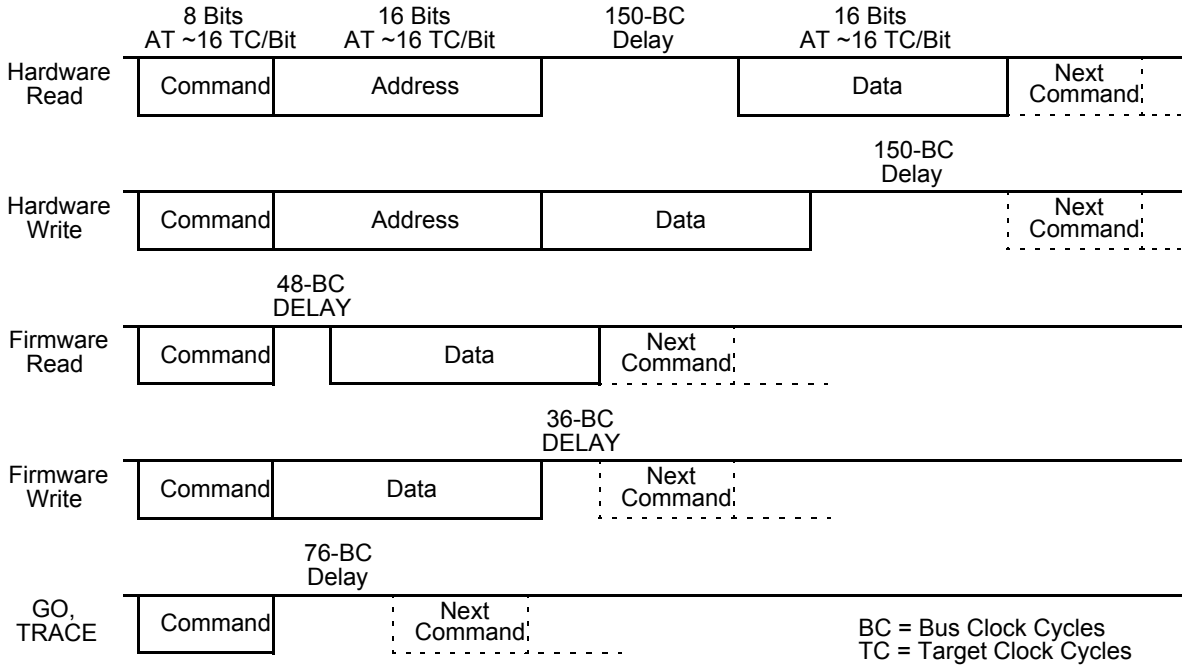

Figure 7-6. BDM Command Structure

7.4.6 BDM Serial Interface

The BDM communicates with external devices serially via the BKGD pin. During reset, this pin is a mode select input which selects between normal and special modes of operation. After reset, this pin becomes the dedicated serial interface pin for the BDM.

The BDM serial interface is timed based on the VCO clock (please refer to the CPMU Block Guide for more details), which gets divided by 8. This clock will be referred to as the target clock in the following explanation.

The BDM serial interface uses a clocking scheme in which the external host generates a falling edge on the BKGD pin to indicate the start of each bit time. This falling edge is sent for every bit whether data is transmitted or received. Data is transferred most significant bit (MSB) first at 16 target clock cycles per bit. The interface times out if 512 clock cycles occur between falling edges from the host.

The BKGD pin is a pseudo open-drain pin and has an weak on-chip active pull-up that is enabled at all times. It is assumed that there is an external pull-up and that drivers connected to BKGD do not typically drive the high level. Since R-C rise time could be unacceptably long, the target system and host provide brief driven-high (speedup) pulses to drive BKGD to a logic 1. The source of this speedup pulse is the host for transmit cases and the target for receive cases.

The timing for host-to-target is shown in Figure 7-7 and that of target-to-host in Figure 7-8 and Figure 7-9. All four cases begin when the host drives the BKGD pin low to generate a falling edge. Since the host and target are operating from separate clocks, it can take the target system up to one full clock cycle to recognize this edge. The target measures delays from this perceived start of the bit time while the host measures delays from the point it actually drove BKGD low to start the bit up to one target clock cycle

Chapter 8
S12S Debug Module (S12SDBGV2)

Table 8-1. Revision History

Revision Number	Revision Date	Sections Affected	Summary of Changes
02.08	09.MAY.2008	General	Spelling corrections. Revision history format changed.
02.09	29.MAY.2008	8.4.5.4	Added note for end aligned, PurePC, rollover case.
02.10	27.SEP.2012	General	Changed cross reference formats

8.1 Introduction

The S12SDBG module provides an on-chip trace buffer with flexible triggering capability to allow non-intrusive debug of application software. The S12SDBG module is optimized for S12SCPU debugging.

Typically the S12SDBG module is used in conjunction with the S12SBDM module, whereby the user configures the S12SDBG module for a debugging session over the BDM interface. Once configured the S12SDBG module is armed and the device leaves BDM returning control to the user program, which is then monitored by the S12SDBG module. Alternatively the S12SDBG module can be configured over a serial interface using SWI routines.

8.1.1 Glossary Of Terms

COF: Change Of Flow. Change in the program flow due to a conditional branch, indexed jump or interrupt

BDM: Background Debug Mode

S12SBDM: Background Debug Module

DUG: Device User Guide, describing the features of the device into which the DBG is integrated

WORD: 16-bit data entity

Data Line: 20-bit data entity

CPU: S12SCPU module

DBG: S12SDBG module

POR: Power On Reset

8.4.5.3.1 Information Bit Organization

The format of the bits is dependent upon the active trace mode as described below.

Field2 Bits in Detail Mode

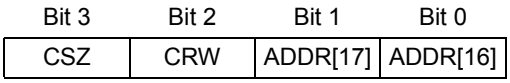

Figure 8-25. Field2 Bits in Detail Mode

In Detail Mode the CSZ and CRW bits indicate the type of access being made by the CPU.

Table 8-38. Field Descriptions

Bit	Description
3 CSZ	**Access Type Indicator**— This bit indicates if the access was a byte or word size when tracing in Detail Mode 0 Word Access 1 Byte Access
2 CRW	**Read Write Indicator** — This bit indicates if the corresponding stored address corresponds to a read or write access when tracing in Detail Mode. 0 Write Access 1 Read Access
1 ADDR[17]	**Address Bus bit 17**— Corresponds to system address bus bit 17.
0 ADDR[16]	**Address Bus bit 16**— Corresponds to system address bus bit 16.

Field2 Bits in Normal and Loop1 Modes

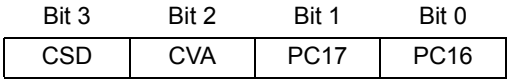

Figure 8-26. Information Bits PCH

Table 8-39. PCH Field Descriptions

Bit	Description
3 CSD	**Source Destination Indicator** — In Normal and Loop1 mode this bit indicates if the corresponding stored address is a source or destination address. This bit has no meaning in Compressed Pure PC mode. 0 Source Address 1 Destination Address
2 CVA	**Vector Indicator** — In Normal and Loop1 mode this bit indicates if the corresponding stored address is a vector address. Vector addresses are destination addresses, thus if CVA is set, then the corresponding CSD is also set. This bit has no meaning in Compressed Pure PC mode. 0 Non-Vector Destination Address 1 Vector Destination Address
1 PC17	**Program Counter bit 17**— In Normal and Loop1 mode this bit corresponds to program counter bit 17.

NOTE

NXP recommends an evaluation of the application board and chosen resonator or crystal by the resonator or crystal supplier.
The loop controlled circuit (XOSCLCP) is not suited for overtone resonators and crystals.

10.2.3 VDDR — Regulator Power Input Pin

Pin V_{DDR} is the power input of IVREG. All currents sourced into the regulator loads flow through this pin.

An off-chip decoupling capacitor (100 nF...220 nF, X7R ceramic) between V_{DDR} and V_{SS} can smooth ripple on V_{DDR}.

10.2.4 VSS — Ground Pin

V_{SS} must be grounded.

10.2.5 VDDA, VSSA — Regulator Reference Supply Pins

Pins V_{DDA} and V_{SSA} are used to supply the analog parts of the regulator.
Internal precision reference circuits are supplied from these signals.

An off-chip decoupling capacitor (100 nF...220 nF, X7R ceramic) between V_{DDA} and V_{SSA} can improve the quality of this supply.

10.2.6 VDDX, VSSX— Pad Supply Pins

This supply domain is monitored by the Low Voltage Reset circuit.

An off-chip decoupling capacitor (100 nF...220 nF, X7R ceramic) between VDDX and VSSX can improve the quality of this supply.

NOTE

Depending on the device package following device supply pins are maybe combined into one pin: VDDR, VDDX and VDDA.
Depending on the device package following device supply pins are maybe combined into one pin: VSS, VSSX and VSSA.
Please refer to the device Reference Manual for information if device supply pins are combined into one supply pin for certain packages and which supply pins are combined together.
An off-chip decoupling capacitor (100 nF...220 nF, X7R ceramic) between the combined supply pin pair can improve the quality of this supply.

10.2.7 VDD — Internal Regulator Output Supply (Core Logic)

Node VDD is a device internal supply output of the voltage regulator that provides the power supply for the core logic.
This supply domain is monitored by the Low Voltage Reset circuit.

10.2.8 VDDF — Internal Regulator Output Supply (NVM Logic)

Node VDDF is a device internal supply output of the voltage regulator that provides the power supply for the NVM logic.
This supply domain is monitored by the Low Voltage Reset circuit

10.2.9 API_EXTCLK — API external clock output pin

This pin provides the signal selected via APIES and is enabled with APIEA bit. See device specification to which pin it connects.

10.3 Memory Map and Registers

This section provides a detailed description of all registers accessible in the S12CPMU.

10.3.1 Module Memory Map

The S12CPMU registers are shown in Figure 10-3.

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0034	CPMU SYNR	R	VCOFRQ[1:0]		SYNDIV[5:0]					
		W								
0x0035	CPMU REFDIV	R	REFFRQ[1:0]		0	0	REFDIV[3:0]			
		W								
0x0036	CPMU POSTDIV	R	0	0	0	POSTDIV[4:0]				
		W								
0x0037	CPMUFLG	R	RTIF	PORF	LVRF	LOCKIF	LOCK	ILAF	OSCIF	UPOSC
		W								
0x0038	CPMUINT	R	RTIE	0	0	LOCKIE	0	0	OSCIE	0
		W								
0x0039	CPMUCLKS	R	PLLSEL	PSTP	0	COP OSCSEL1	PRE	PCE	RTI OSCSEL	COP OSCSEL0
		W								
0x003A	CPMUPLL	R	0	0	FM1	FM0	0	0	0	0
		W								
			= Unimplemented or Reserved							

Figure 10-3. CPMU Register Summary

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0003	ATDCTL3	R	DJM	S8C	S4C	S2C	S1C	FIFO	FRZ1	FRZ0
		W								
0x0004	ATDCTL4	R	SMP2	SMP1	SMP0	PRS[4:0]				
		W								
0x0005	ATDCTL5	R	0	SC	SCAN	MULT	CD	CC	CB	CA
		W								
0x0006	ATDSTAT0	R	SCF	0	ETORF	FIFOR	CC3	CC2	CC1	CC0
		W								
0x0007	Unimple-mented	R	0	0	0	0	0	0	0	0
		W								
0x0008	ATDCMPEH	R	CMPE[15:8]							
		W								
0x0009	ATDCMPEL	R	CMPE[7:0]							
		W								
0x000A	ATDSTAT2H	R	CCF[15:8]							
		W								
0x000B	ATDSTAT2L	R	CCF[7:0]							
		W								
0x000C	ATDDIENH	R	IEN[15:8]							
		W								
0x000D	ATDDIENL	R	IEN[7:0]							
		W								
0x000E	ATDCMPHTH	R	CMPHT[15:8]							
		W								
0x000F	ATDCMPHTL	R	CMPHT[7:0]							
		W								
0x0010	ATDDR0	R	See Section 15.3.2.12.1, “Left Justified Result Data (DJM=0)” and Section 15.3.2.12.2, “Right Justified Result Data (DJM=1)”							
		W								
0x0012	ATDDR1	R	See Section 15.3.2.12.1, “Left Justified Result Data (DJM=0)” and Section 15.3.2.12.2, “Right Justified Result Data (DJM=1)”							
		W								
0x0014	ATDDR2	R	See Section 15.3.2.12.1, “Left Justified Result Data (DJM=0)” and Section 15.3.2.12.2, “Right Justified Result Data (DJM=1)”							
		W								
0x0016	ATDDR3	R	See Section 15.3.2.12.1, “Left Justified Result Data (DJM=0)” and Section 15.3.2.12.2, “Right Justified Result Data (DJM=1)”							
		W								
0x0018	ATDDR4	R	See Section 15.3.2.12.1, “Left Justified Result Data (DJM=0)” and Section 15.3.2.12.2, “Right Justified Result Data (DJM=1)”							
		W								
0x001A	ATDDR5	R	See Section 15.3.2.12.1, “Left Justified Result Data (DJM=0)” and Section 15.3.2.12.2, “Right Justified Result Data (DJM=1)”							
		W								
0x001C	ATDDR6	R	See Section 15.3.2.12.1, “Left Justified Result Data (DJM=0)” and Section 15.3.2.12.2, “Right Justified Result Data (DJM=1)”							
		W								
0x001E	ATDDR7	R	See Section 15.3.2.12.1, “Left Justified Result Data (DJM=0)” and Section 15.3.2.12.2, “Right Justified Result Data (DJM=1)”							
		W								
0x0020	ATDDR8	R	See Section 15.3.2.12.1, “Left Justified Result Data (DJM=0)” and Section 15.3.2.12.2, “Right Justified Result Data (DJM=1)”							
		W								
0x0022	ATDDR9	R	See Section 15.3.2.12.1, “Left Justified Result Data (DJM=0)” and Section 15.3.2.12.2, “Right Justified Result Data (DJM=1)”							
		W								

= Unimplemented or Reserved

Figure 15-2. ADC10B16C Register Summary (Sheet 2 of 3)

16.1.2 Modes of Operation

16.1.2.1 Conversion Modes

There is software programmable selection between performing **single** or **continuous conversion** on a **single channel** or **multiple channels**.

16.1.2.2 MCU Operating Modes

- **Stop Mode**
  Entering Stop Mode aborts any conversion sequence in progress and if a sequence was aborted restarts it after exiting stop mode. This has the same effect/consequences as starting a conversion sequence with write to ATDCTL5. So after exiting from stop mode with a previously aborted sequence all flags are cleared etc.
- **Wait Mode**
  ADC12B16C behaves same in Run and Wait Mode. For reduced power consumption continuous conversions should be aborted before entering Wait mode.
- **Freeze Mode**
  In Freeze Mode the ADC12B16C will either continue or finish or stop converting according to the FRZ1 and FRZ0 bits. This is useful for debugging and emulation.

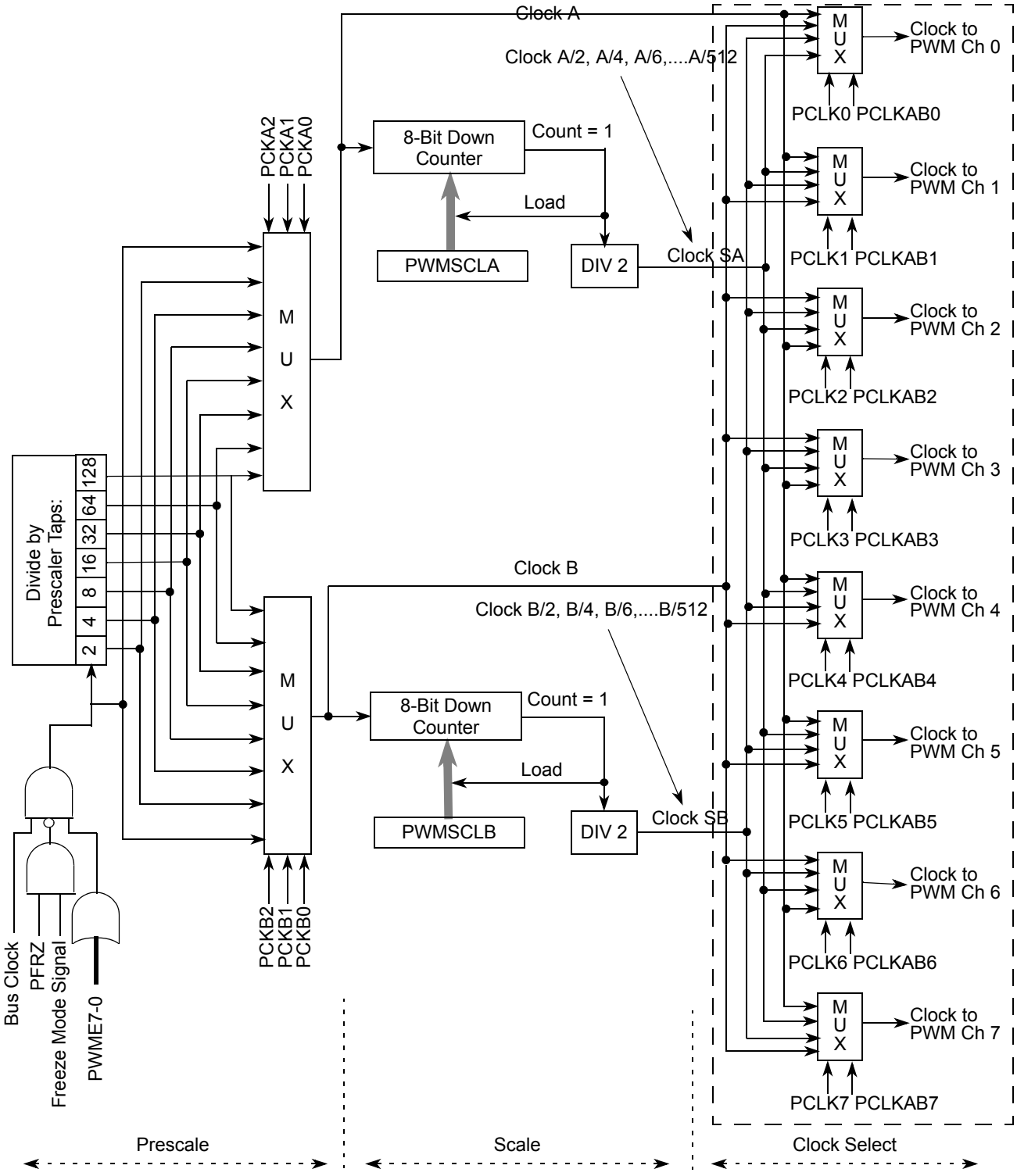

Figure 19-15. PWM Clock Select Block Diagram

NOTE

Changing the PWM output mode from left aligned to center aligned output (or vice versa) while channels are operating can cause irregularities in the PWM output. It is recommended to program the output mode before enabling the PWM channel.

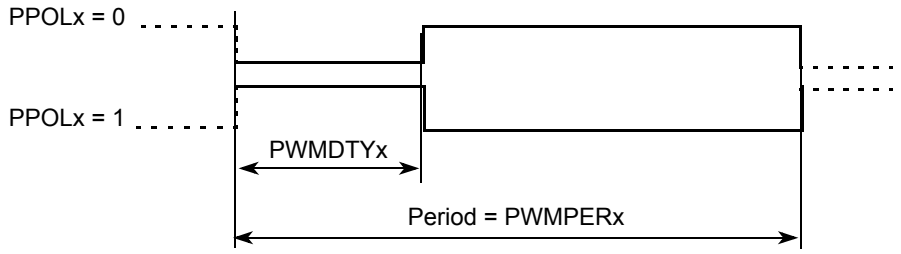

Figure 19-17. PWM Left Aligned Output Waveform

To calculate the output frequency in left aligned output mode for a particular channel, take the selected clock source frequency for the channel (A, B, SA, or SB) and divide it by the value in the period register for that channel.

- PWMx Frequency = Clock (A, B, SA, or SB) / PWMPERx
- PWMx Duty Cycle (high time as a% of period):
  - Polarity = 0 (PPOLx = 0)

    Duty Cycle = [(PWMPERx-PWMDTYx)/PWMPERx] * 100%
  - Polarity = 1 (PPOLx = 1)

    Duty Cycle = [PWMDTYx / PWMPERx] * 100%

As an example of a left aligned output, consider the following case:

Clock Source = E, where E = 10 MHz (100 ns period)

PPOLx = 0

PWMPERx = 4

PWMDTYx = 1

PWMx Frequency = 10 MHz/4 = 2.5 MHz

PWMx Period = 400 ns

PWMx Duty Cycle = 3/4 *100% = 75%

The output waveform generated is shown in Figure 19-18.

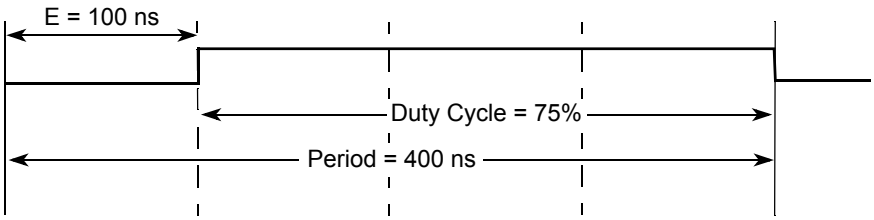

Figure 19-18. PWM Left Aligned Output Example Waveform

23.3.2.8 Timer Control Register 1/Timer Control Register 2 (TCTL1/TCTL2)

Module Base + 0x0008

	7	6	5	4	3	2	1	0
R W	OM7	OL7	OM6	OL6	OM5	OL5	OM4	OL4
Reset	0	0	0	0	0	0	0	0

Figure 23-14. Timer Control Register 1 (TCTL1)

Module Base + 0x0009

	7	6	5	4	3	2	1	0
R W	OM3	OL3	OM2	OL2	OM1	OL1	OM0	OL0
Reset	0	0	0	0	0	0	0	0

Figure 23-15. Timer Control Register 2 (TCTL2)

Read: Anytime

Write: Anytime

Table 23-8. TCTL1/TCTL2 Field Descriptions

Note: Writing to unavailable bits has no effect. Reading from unavailable bits return a zero

Field	Description
7:0 OMx	**Output Mode** — These eight pairs of control bits are encoded to specify the output action to be taken as a result of a successful OCx compare. When either OMx or OLx is 1, the pin associated with OCx becomes an output tied to OCx. **Note:** To enable output action by OMx bits on timer port, the corresponding bit in OC7M should be cleared. For an output line to be driven by an OCx the OCPDx must be cleared.
7:0 OLx	**Output Level** — These eightpairs of control bits are encoded to specify the output action to be taken as a result of a successful OCx compare. When either OMx or OLx is 1, the pin associated with OCx becomes an output tied to OCx. **Note:** To enable output action by OLx bits on timer port, the corresponding bit in OC7M should be cleared. For an output line to be driven by an OCx the OCPDx must be cleared.

Table 23-9. Compare Result Output Action

OMx	OLx	Action
0	0	No output compare action on the timer output signal
0	1	Toggle OCx output line
1	0	Clear OCx output line to zero
1	1	Set OCx output line to one

Table 24-34. Erase Verify P-Flash Section Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x03	Global address [17:16] of a P-Flash block
001	Global address [15:0] of the first phrase to be verified	
010	Number of phrases to be verified	

Upon clearing CCIF to launch the Erase Verify P-Flash Section command, the Memory Controller will verify the selected section of Flash memory is erased. The CCIF flag will set after the Erase Verify P-Flash Section operation has completed. If the section is not erased, it means blank check failed, both MGSTAT bits will be set.

Table 24-35. Erase Verify P-Flash Section Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 010 at command launch
		Set if command not available in current mode (see Table 24-25)
		Set if an invalid global address [17:0] is supplied see Table 24-3)[1]
		Set if a misaligned phrase address is supplied (global address [2:0] != 000)
		Set if the requested section crosses a the P-Flash address boundary
	FPVIOL	None
	MGSTAT1	Set if any errors have been encountered during the read[2] or if blank check failed.
	MGSTAT0	Set if any non-correctable errors have been encountered during the read[2] or if blank check failed.

1 As defined by the memory map for FTMRG32K1.

2 As found in the memory map for FTMRG32K1.

24.4.6.4 Read Once Command

The Read Once command provides read access to a reserved 64 byte field (8 phrases) located in the nonvolatile information register of P-Flash. The Read Once field is programmed using the Program Once command described in Section 24.4.6.6. The Read Once command must not be executed from the Flash block containing the Program Once reserved field to avoid code runaway.

Table 24-36. Read Once Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x04	Not Required
001	Read Once phrase index (0x0000 - 0x0007)	
010	Read Once word 0 value	
011	Read Once word 1 value	
100	Read Once word 2 value	

Table 26-29. EEPROM Commands

FCMD	Command	Function on EEPROM Memory
0x08	Erase All Blocks	Erase all EEPROM (and P-Flash) blocks. An erase of all Flash blocks is only possible when the FPLDIS, FPHDIS, and FPOPEN bits in the FPROT register and the DPOPEN bit in the EEPROT register are set prior to launching the command.
0x09	Erase Flash Block	Erase a EEPROM (or P-Flash) block. An erase of the full EEPROM block is only possible when DPOPEN bit in the EEPROT register is set prior to launching the command.
0x0B	Unsecure Flash	Supports a method of releasing MCU security by erasing all EEPROM (and P-Flash) blocks and verifying that all EEPROM (and P-Flash) blocks are erased.
0x0D	Set User Margin Level	Specifies a user margin read level for the EEPROM block.
0x0E	Set Field Margin Level	Specifies a field margin read level for the EEPROM block (special modes only).
0x10	Erase Verify EEPROM Section	Verify that a given number of words starting at the address provided are erased.
0x11	Program EEPROM	Program up to four words in the EEPROM block.
0x12	Erase EEPROM Sector	Erase all bytes in a sector of the EEPROM block.

26.4.5 Allowed Simultaneous P-Flash and EEPROM Operations

Only the operations marked ‘OK’ in Table 26-30 are permitted to be run simultaneously on the Program Flash and EEPROM blocks. Some operations cannot be executed simultaneously because certain hardware resources are shared by the two memories. The priority has been placed on permitting Program Flash reads while program and erase operations execute on the EEPROM, providing read (P-Flash) while write (EEPROM) functionality.

Table 26-30. Allowed P-Flash and EEPROM Simultaneous Operations

	EEPROM				
Program Flash	**Read**	**Margin Read[1]**	**Program**	**Sector Erase**	**Mass Erase[2]**
Read		OK	OK	OK	
Margin Read[1]					
Program					
Sector Erase					
Mass Erase[2]					OK

1 A ‘Margin Read’ is any read after executing the margin setting commands ‘Set User Margin Level’ or ‘Set Field Margin Level’ with anything but the ‘normal’ level specified. See the Note on margin settings in Section 26.4.6.12 and Section 26.4.6.13.

2 The ‘Mass Erase’ operations are commands ‘Erase All Blocks’ and ‘Erase Flash Block’

Table 28-24. FCCOB - NVM Command Mode (Typical Usage)

CCOBIX[2:0]	Byte	FCCOB Parameter Fields (NVM Command Mode)
010	HI	Data 0 [15:8]
	LO	Data 0 [7:0]
011	HI	Data 1 [15:8]
	LO	Data 1 [7:0]
100	HI	Data 2 [15:8]
	LO	Data 2 [7:0]
101	HI	Data 3 [15:8]
	LO	Data 3 [7:0]

28.3.2.12 Flash Reserved1 Register (FRSV1)

This Flash register is reserved for factory testing.

Offset Module Base + 0x000C

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 28-18. Flash Reserved1 Register (FRSV1)

All bits in the FRSV1 register read 0 and are not writable.

28.3.2.13 Flash Reserved2 Register (FRSV2)

This Flash register is reserved for factory testing.

Offset Module Base + 0x000D

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 28-19. Flash Reserved2 Register (FRSV2)

All bits in the FRSV2 register read 0 and are not writable.

28.3.2.14 Flash Reserved3 Register (FRSV3)

This Flash register is reserved for factory testing.

Table D-1. Bondpad Coordinates

Die Pad	Bond Post	Die Pad X Coordinate	Die Pad Y Coordinate	Function
28	28	-1315.5	-1472.06	PB[3]
29	29	-1134.5	-1472.06	PP[0]
30	30	-964.5	-1472.06	PP[1]
31	31	-794.5	-1472.06	PP[2]
32	32	-660.5	-1472.06	PP[3]
33	33	-526.5	-1472.06	PP[4]
34	34	-404.5	-1472.06	PP[5]
35	35	-292.5	-1472.06	PP[6]
36	36	-190.5	-1472.06	PP[7]
37	37	-105.5	-1472.06	VDDX3
38	38	-0.5	-1472.06	VSSX3
39	39	93.5	-1472.06	PT[7]
40	40	189.5	-1472.06	PT[6]
41	41	291.5	-1472.06	PT[5]
42	42	403.5	-1472.06	PT[4]
43	43	525.5	-1472.06	PT[3]
44	44	659.5	-1472.06	PT[2]
45	45	805.5	-1472.06	PT[1]
46	46	964.5	-1472.06	PT[0]
47	47	1120.5	-1472.06	PB[4]
48	48	1242.5	-1472.06	PB[5]
49	49	1412.5	-1472.06	PB[6]
50	50	1582.5	-1472.06	PB[7]
51	51	-1832.06	-1347.5	PC[0]
52	52	-1832.06	-1139.5	PC[1]
53	53	-1832.06	-1022.5	PC[2]
54	54	-1832.06	-905.5	PC[3]
55	55	-1832.06	-788.5	PAD[0]
56	56	-1832.06	-681.5	PAD[8]
57	57	-1832.06	-574.5	PAD[1]