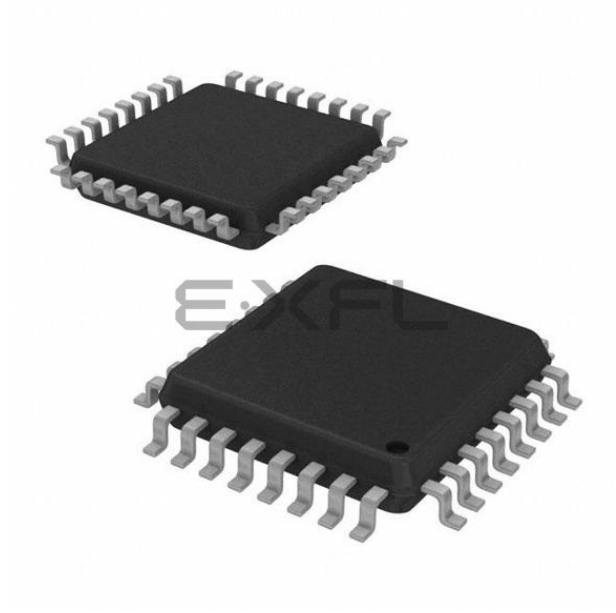

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	12V1
Core Size	16-Bit
Speed	25MHz
Connectivity	IrDA, LINbus, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	26
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	3.13V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s9s12gn16f1vlcr

- Bus-off recovery by software intervention or automatically
- 16-bit time stamp of transmitted/received messages

1.3.12 Serial Communication Interface Module (SCI)

- Up to three SCI modules
- Full-duplex or single-wire operation
- Standard mark/space non-return-to-zero (NRZ) format
- Selectable IrDA 1.4 return-to-zero-inverted (RZI) format with programmable pulse widths
- 13-bit baud rate selection
- Programmable character length
- Programmable polarity for transmitter and receiver
- Active edge receive wakeup
- Break detect and transmit collision detect supporting LIN 1.3, 2.0, 2.1 and SAE J2602

1.3.13 Serial Peripheral Interface Module (SPI)

- Up to three SPI modules
- Configurable 8- or 16-bit data size
- Full-duplex or single-wire bidirectional
- Double-buffered transmit and receive
- Master or slave mode
- MSB-first or LSB-first shifting
- Serial clock phase and polarity options

1.3.14 Analog-to-Digital Converter Module (ADC)

Up to 16-channel, 10-bit/12-bit[1] analog-to-digital converter

  — 3 us conversion time
  — 8-/10[1]-bit resolution
  — Left or right justified result data
  — Wakeup from low power modes on analog comparison > or <= match
  — Continuous conversion mode
  — External triggers to initiate conversions via GPIO or peripheral outputs such as PWM or TIM
  — Multiple channel scans
  — Precision fixed voltage reference for ADC conversions
  —

- Pins can also be used as digital I/O including wakeup capability

1. 12-bit resolution only available on S12GA192 and S12GA240 devices.

1.6.1 Part ID Assignments

The part ID is located in two 8-bit registers PARTIDH and PARTIDL (addresses 0x001A and 0x001B). The read-only value is a unique part ID for each revision of the chip. Table 1-5 shows the assigned part ID number and Mask Set number.

Table 1-5. Assigned Part ID Numbers

Device	Mask Set Number	Part ID
MC9S12GA240	0N95B	0xF080
MC9S12G240	0N95B	0xF080
MC9S12GA192	0N95B	0xF080
MC9S12G192	0N95B	0xF080
MC9S12GA128	0N51A	0xF180
	0N42V	0xF180
MC9S12G128	0N51A	0xF180
	0N42V	0xF180
MC9S12GA96	0N51A	0xF180
	0N42V	0xF180
MC9S12G96	0N51A	0xF180
	0N42V	0xF180
MC9S12GA64	0N75C	0xF280
	0N55V	0xF280
MC9S12G64	0N75C[1]	0xF280[1]
	0N55V[1]	0xF280[1]
	1N75C[2]	0xF281[2]
	1N55V[2]	0xF281[2]
MC9S12GA48	0N75C	0xF280
	0N55V	0xF280
MC9S12G48	0N75C[1]	0xF280[1]
	0N55V[1]	0xF280[1]
	1N75C[2]	0xF281[2]
	1N55V[2]	0xF281[2]
MC9S12GN48	0N75C[1]	0xF280[1]
	0N55V[1]	0xF280[1]
	1N75C[2]	0xF281[2]
	1N55V[2]	0xF281[2]
MC9S12GNA32	0N48A	0xF380
	0N57V	0xF380
MC9S12GN32	0N48A[3]	0xF380[3]
	0N57V[3]	0xF380[3]
	1N48A[4]	0xF381[4]
	1N57V[4]	0xF381[4]

Table 1-28. 100-Pin LQFP Pinout for S12G192 and S12G240

	Function <----lowest-----PRIORITY-----highest---->				Power Supply	Internal Pull Resistor	
Package Pin	Pin	2nd Func.	3rd Func.	4th Func.		CTRL	Reset State
86	PS4	MISO0	—	—	V_{DDX}	PERS/PPSS	Up
87	PS5	MOSI0	—	—	V_{DDX}	PERS/PPSS	Up
88	PS6	SCK0	—	—	V_{DDX}	PERS/PPSS	Up
89	PS7	API_EXTCLK	$\overline{SS0}$	—	V_{DDX}	PERS/PPSS	Up
90	VSSX2	—	—	—	—	—	—
91	VDDX2	—	—	—	—	—	—
92	PM0	RXCAN	—	—	V_{DDX}	PERM/PPSM	Disabled
93	PM1	TXCAN	—	—	V_{DDX}	PERM/PPSM	Disabled
94	PD4	—	—	—	V_{DDX}	PUCR/PUPDE	Disabled
95	PD5	—	—	—	V_{DDX}	PUCR/PUPDE	Disabled
96	PD6	—	—	—	V_{DDX}	PUCR/PUPDE	Disabled
97	PD7	—	—	—	V_{DDX}	PUCR/PUPDE	Disabled
98	PM2	RXD2	—	—	V_{DDX}	PERM/PPSM	Disabled
99	PM3	TXD2	—	—	V_{DDX}	PERM/PPSM	Disabled
100	PJ7	KWJ7	$\overline{SS2}$	—	V_{DDX}	PERJ/PPSJ	Up

1 The regular I/O characteristics (see Section A.2, “I/O Characteristics”) apply if the EXTAL/XTAL function is disabled

Chapter 2
Port Integration Module (S12GPIMV1)

Revision History

Rev. No. (Item No.)	Date (Submitted By)	Sections Affected	Substantial Change(s)
V01.01	01 Dec 2010	Table 2-4 Table 2-5 Table 2-8 Table 2-16 Table 2-17	• Removed TXD2 and RXD2 from PM1 and PM0 for G64 • Simplified input buffer control description on port C and AD • Corrected DAC signal priorities on pins PAD10 and PAD11 with shared AMP and DACU output functions
V01.02	30 Aug 2011	2.4.3.40/2-224 2.4.3.48/2-230 2.4.3.63/2-239 2.4.3.64/2-240	• Corrected PIFx descriptions
V01.03	15 Mar 2012	Table 2-2./2-150 Table 2-4./2-154	• Added GA and GNA derivatives

2.1 Introduction

This section describes the S12G-family port integration module (PIM) in its configurations depending on the family devices in their available package options.

It is split up into two parts, firstly determining the routing of the various signals to the available package pins (“PIM Routing”) and secondly describing the general-purpose port related logic (“PIM Ports”).

2.1.1 Glossary

Table 2-1. Glossary Of Terms

Term	Definition
Pin	Package terminal with a unique number defined in the device pinout section
Signal	Input or output line of a peripheral module or general-purpose I/O function arbitrating for a dedicated pin
Port	Group of general-purpose I/O pins sharing peripheral signals

5.3.2.4 Program Page Index Register (PPAGE)

Address: 0x0015

	7	6	5	4	3	2	1	0
R	0	0	0	0	PIX3	PIX2	PIX1	PIX0
W								
Reset	0	0	0	0	1	1	1	0

Figure 5-8. Program Page Index Register (PPAGE)

Read: Anytime

Write: Anytime

The four index bits of the PPAGE register select a 16K page in the global memory map (Figure 5-11). The selected 16K page is mapped into the paging window ranging from local address 0x8000 to 0xBFFF. Figure 5-9 illustrates the translation from local to global addresses for accesses to the paging window. The CPU has special access to read and write this register directly during execution of CALL and RTC instructions.

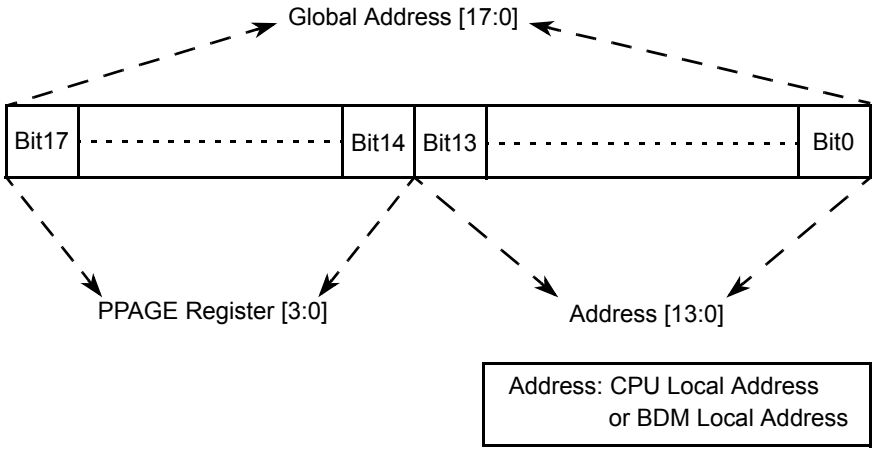


Figure 5-9. PPAGE Address Mapping

NOTE

Writes to this register using the special access of the CALL and RTC instructions will be complete before the end of the instruction execution.

Table 5-7. PPAGE Field Descriptions

Field	Description
3–0 PIX[3:0]	**Program Page Index Bits 3–0** — These page index bits are used to select which of the 256 flash array pages is to be accessed in the Program Page Window.

The fixed 16KB page from 0x0000 to 0x3FFF is the page number 0xC. Parts of this page are covered by Registers, EEPROM and RAM space. See SoC Guide for details.

The fixed 16KB page from 0x4000–0x7FFF is the page number 0xD.

Read: DBGACTL if COMRV[1:0] = 00
DBGBCTL if COMRV[1:0] = 01
DBGCCTL if COMRV[1:0] = 10

Write: DBGACTL if COMRV[1:0] = 00 and DBG not armed
DBGBCTL if COMRV[1:0] = 01 and DBG not armed
DBGCCTL if COMRV[1:0] = 10 and DBG not armed

Table 8-22. DBGXCTL Field Descriptions

Field	Description
7 SZE (Comparators A and B)	**Size Comparator Enable Bit** — The SZE bit controls whether access size comparison is enabled for the associated comparator. This bit is ignored if the TAG bit in the same register is set. 0 Word/Byte access size is not used in comparison 1 Word/Byte access size is used in comparison
6 SZ (Comparators A and B)	**Size Comparator Value Bit** — The SZ bit selects either word or byte access size in comparison for the associated comparator. This bit is ignored if the SZE bit is cleared or if the TAG bit in the same register is set. 0 Word access size is compared 1 Byte access size is compared
5 TAG	**Tag Select**— This bit controls whether the comparator match has immediate effect, causing an immediate state sequencer transition or tag the opcode at the matched address. Tagged opcodes trigger only if they reach the execution stage of the instruction queue. 0 Allow state sequencer transition immediately on match 1 On match, tag the opcode. If the opcode is about to be executed allow a state sequencer transition
4 BRK	**Break**— This bit controls whether a comparator match terminates a debug session immediately, independent of state sequencer state. To generate an immediate breakpoint the module breakpoints must be enabled using the DBGC1 bit DBGBRK. 0 The debug session termination is dependent upon the state sequencer and trigger conditions. 1 A match on this channel terminates the debug session immediately; breakpoints if active are generated, tracing, if active, is terminated and the module disarmed.
3 RW	**Read/Write Comparator Value Bit** — The RW bit controls whether read or write is used in compare for the associated comparator. The RW bit is not used if RWE = 0. This bit is ignored if the TAG bit in the same register is set. 0 Write cycle is matched1Read cycle is matched
2 RWE	**Read/Write Enable Bit** — The RWE bit controls whether read or write comparison is enabled for the associated comparator.This bit is ignored if the TAG bit in the same register is set 0 Read/Write is not used in comparison 1 Read/Write is used in comparison
1 NDB (Comparator A)	**Not Data Bus** — The NDB bit controls whether the match occurs when the data bus matches the comparator register value or when the data bus differs from the register value. This bit is ignored if the TAG bit in the same register is set. This bit is only available for comparator A. 0 Match on data bus equivalence to comparator register contents 1 Match on data bus difference to comparator register contents
0 COMPE	Determines if comparator is enabled 0 The comparator is not enabled 1 The comparator is enabled

Table 8-23 shows the effect for RWE and RW on the comparison conditions. These bits are ignored if the corresponding TAG bit is set since the match occurs based on the tagged opcode reaching the execution stage of the instruction queue.

- **Pseudo Stop Mode (PSTP = 1 and OSCE=1)**
  External oscillator (XOSCLCP) continues to run.
  - If COPOSCSEL1=0:
    If the respective enable bits are set (PCE=1 and PRE=1) the COP and RTI will continue to run with a clock derived from the oscillator clock.
    The clock configuration bits PLLSEL, COPOSCSEL0, RTIOSCSEL are unchanged.
  - If COPOSCSEL1=1:
    If the respective enable bit for the RTI is set (PRE=1) the RTI will continue to run with a clock derived from the oscillator clock.
    The COP will continue to run on ACLK.
    The clock configuration bits PLLSEL, COPOSCSEL0, RTIOSCSEL are unchanged.

NOTE

When starting up the external oscillator (either by programming OSCE bit to 1 or on exit from Full Stop Mode with OSCE bit already 1) the software must wait for a minimum time equivalent to the startup-time of the external oscillator t_{UPOSC} before entering Pseudo Stop Mode.

NOTE

Care should be taken to ensure that the bus frequency does not exceed the specified maximum when frequency modulation is enabled.

Table 10-7. CPMUPLL Field Descriptions

Field	Description
5, 4 FM1, FM0	PLL **Frequency Modulation Enable Bits** — FM1 and FM0 enable frequency modulation on the VCOCLK. This is to reduce noise emission. The modulation frequency is f_{ref} divided by 16. See Table 10-8 for coding.

Table 10-8. FM Amplitude selection

FM1	FM0	FM Amplitude / f_{VCO} Variation
0	0	FM off
0	1	±1%
1	0	±2%
1	1	±4%

10.3.2.8 S12CPMU RTI Control Register (CPMURTI)

This register selects the time-out period for the Real Time Interrupt.

The clock source for the RTI is either IRCCLK or OSCCLK depending on the setting of the RTIOSCSEL bit. In Stop Mode with PSTP=1 (Pseudo Stop Mode) and RTIOSCSEL=1 the RTI continues to run, else the RTI counter halts in Stop Mode.

0x003B

	7	6	5	4	3	2	1	0
R W	RTDEC	RTR6	RTR5	RTR4	RTR3	RTR2	RTR1	RTR0
Reset	0	0	0	0	0	0	0	0

Figure 10-11. S12CPMU RTI Control Register (CPMURTI)

Read: Anytime

Write: Anytime

16.3.2.12.2 Right Justified Result Data (DJM=1)

Module Base +
0x0010 = ATDDR0, 0x0012 = ATDDR1, 0x0014 = ATDDR2, 0x0016 = ATDDR3
0x0018 = ATDDR4, 0x001A = ATDDR5, 0x001C = ATDDR6, 0x001E = ATDDR7
0x0020 = ATDDR8, 0x0022 = ATDDR9, 0x0024 = ATDDR10, 0x0026 = ATDDR11
0x0028 = ATDDR12, 0x002A = ATDDR13, 0x002C = ATDDR14, 0x002E = ATDDR15

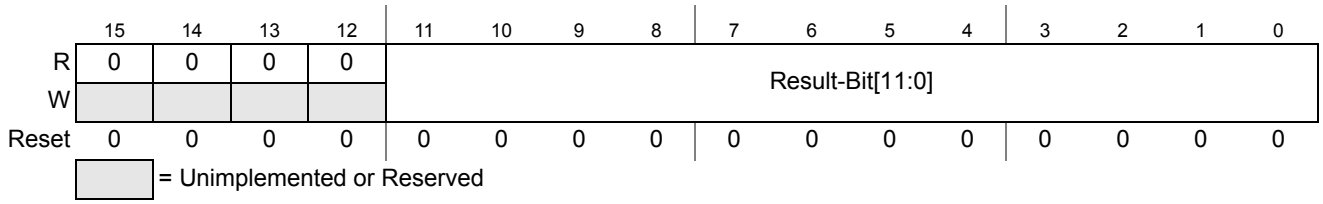


Figure 16-15. Right justified ATD conversion result register (ATDDR*n*)

Table 16-22 shows how depending on the A/D resolution the conversion result is transferred to the ATD result registers for right justified data. Compare is always done using all 12 bits of both the conversion result and the compare value in ATDDRn.

Table 16-22. Conversion result mapping to ATDDRn

A/D resolution	DJM	conversion result mapping to ATDDR*n*
8-bit data	1	Result-Bit[7:0] = result, Result-Bit[11:8]=0000
10-bit data	1	Result-Bit[9:0] = result, Result-Bit[11:10]=00
12-bit data	1	Result-Bit[11:0] = result

Table 20-2. SCIBDH and SCIBDL Field Descriptions

Field	Description
7 IREN	**Infrared Enable Bit** — This bit enables/disables the infrared modulation/demodulation submodule. 0 IR disabled 1 IR enabled
6:5 TNP[1:0]	**Transmitter Narrow Pulse Bits** — These bits enable whether the SCI transmits a 1/16, 3/16, 1/32 or 1/4 narrow pulse. See Table 20-3.
4:0 7:0 SBR[12:0]	**SCI Baud Rate Bits** — The baud rate for the SCI is determined by the bits in this register. The baud rate is calculated two different ways depending on the state of the IREN bit. The formulas for calculating the baud rate are: When IREN = 0 then, SCI baud rate = SCI bus clock / (16 x SBR[12:0]) When IREN = 1 then, SCI baud rate = SCI bus clock / (32 x SBR[12:1]) **Note:** The baud rate generator is disabled after reset and not started until the TE bit or the RE bit is set for the first time. The baud rate generator is disabled when (SBR[12:0] = 0 and IREN = 0) or (SBR[12:1] = 0 and IREN = 1). **Note:** Writing to SCIBDH has no effect without writing to SCIBDL, because writing to SCIBDH puts the data in a temporary location until SCIBDL is written to.

Table 20-3. IRSCI Transmit Pulse Width

TNP[1:0]	Narrow Pulse Width
11	1/4
10	1/32
01	1/16
00	3/16

20.3.2.2 SCI Control Register 1 (SCICR1)

Module Base + 0x0002

	7	6	5	4	3	2	1	0
R W	LOOPS	SCISWAI	RSRC	M	WAKE	ILT	PE	PT
Reset	0	0	0	0	0	0	0	0

Figure 20-5. SCI Control Register 1 (SCICR1)

Read: Anytime, if AMAP = 0.

Write: Anytime, if AMAP = 0.

NOTE

This register is only visible in the memory map if AMAP = 0 (reset condition).

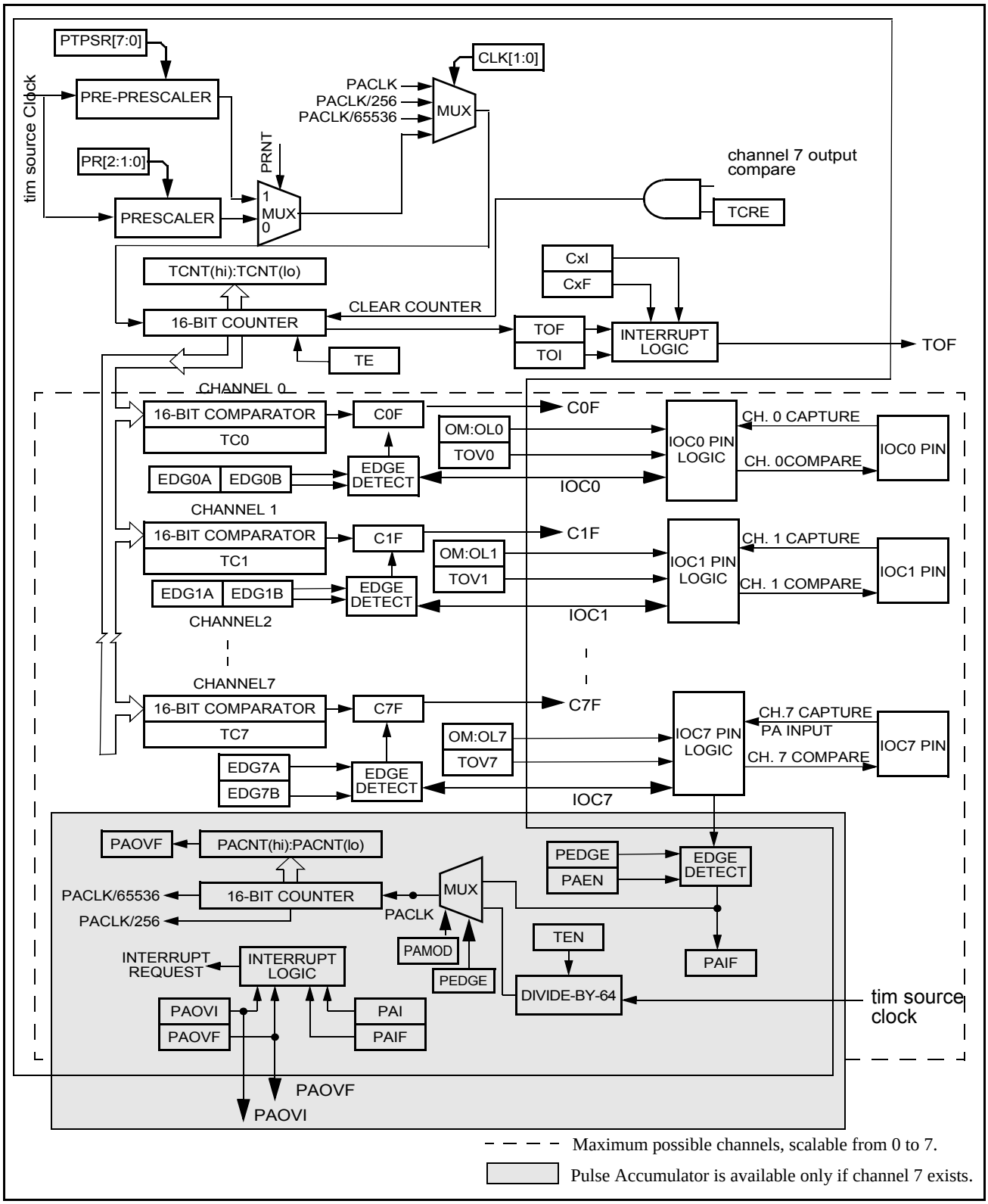


Figure 23-30. Detailed Timer Block Diagram

24.4.6.2 Erase Verify Block Command

The Erase Verify Block command allows the user to verify that an entire P-Flash or EEPROM block has been erased. The FCCOB FlashBlockSelectionCode[1:0] bits determine which block must be verified.

Table 24-31. Erase Verify Block Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x02	Flash block selection code [1:0]. See Table 24-32

Table 24-32. Flash block selection code description

Selection code[1:0]	Flash block to be verified
00	EEPROM
01	Invalid (ACCERR)
10	Invalid (ACCERR)
11	P-Flash

Upon clearing CCIF to launch the Erase Verify Block command, the Memory Controller will verify that the selected P-Flash or EEPROM block is erased. The CCIF flag will set after the Erase Verify Block operation has completed.If the block is not erased, it means blank check failed, both MGSTAT bits will be set.

Table 24-33. Erase Verify Block Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 000 at command launch
		Set if an invalid FlashBlockSelectionCode[1:0] is supplied[1]
	FPVIOL	None
	MGSTAT1	Set if any errors have been encountered during the read[2] or if blank check failed.
	MGSTAT0	Set if any non-correctable errors have been encountered during the read[2] or if blank check failed.

1 As defined by the memory map for FTMRG32K1.

2 As found in the memory map for FTMRG32K1.

24.4.6.3 Erase Verify P-Flash Section Command

The Erase Verify P-Flash Section command will verify that a section of code in the P-Flash memory is erased. The Erase Verify P-Flash Section command defines the starting point of the code to be verified and the number of phrases.

Table 26-49. Erase P-Flash Sector Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 001 at command launch
		Set if command not available in current mode (see Table 26-27)
		Set if an invalid global address [17:16] is supplied see Table 26-3)
		Set if a misaligned phrase address is supplied (global address [2:0] != 000)
	FPVIOL	Set if the selected P-Flash sector is protected
	MGSTAT1	Set if any errors have been encountered during the verify operation
	MGSTAT0	Set if any non-correctable errors have been encountered during the verify operation

26.4.6.10 Unsecure Flash Command

The Unsecure Flash command will erase the entire P-Flash and EEPROM memory space and, if the erase is successful, will release security.

Table 26-50. Unsecure Flash Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x0B	Not required

Upon clearing CCIF to launch the Unsecure Flash command, the Memory Controller will erase the entire P-Flash and EEPROM memory space and verify that it is erased. If the Memory Controller verifies that the entire Flash memory space was properly erased, security will be released. If the erase verify is not successful, the Unsecure Flash operation sets MGSTAT1 and terminates without changing the security state. During the execution of this command (CCIF=0) the user must not write to any Flash module register. The CCIF flag is set after the Unsecure Flash operation has completed.

Table 26-51. Unsecure Flash Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 000 at command launch
		Set if command not available in current mode (see Table 26-27)
	FPVIOL	Set if any area of the P-Flash or EEPROM memory is protected
	MGSTAT1	Set if any errors have been encountered during the verify operation
	MGSTAT0	Set if any non-correctable errors have been encountered during the verify operation

26.4.6.11 Verify Backdoor Access Key Command

The Verify Backdoor Access Key command will only execute if it is enabled by the KEYEN bits in the FSEC register (see Table 26-10). The Verify Backdoor Access Key command releases security if user-supplied keys match those stored in the Flash security bytes of the Flash configuration field (see

Offset Module Base + 0x000E

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 28-20. Flash Reserved3 Register (FRSV3)

All bits in the FRSV3 register read 0 and are not writable.

28.3.2.15 Flash Reserved4 Register (FRSV4)

This Flash register is reserved for factory testing.

Offset Module Base + 0x000F

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 28-21. Flash Reserved4 Register (FRSV4)

All bits in the FRSV4 register read 0 and are not writable.

28.3.2.16 Flash Option Register (FOPT)

The FOPT register is the Flash option register.

Offset Module Base + 0x0010

	7	6	5	4	3	2	1	0
R	NV[7:0]							
W								
Reset	F[1]	F[1]	F[1]	F[1]	F[1]	F[1]	F[1]	F[1]

= Unimplemented or Reserved

Figure 28-22. Flash Option Register (FOPT)

1 Loaded from IFR Flash configuration field, during reset sequence.

All bits in the FOPT register are readable but are not writable.

During the reset sequence, the FOPT register is loaded from the Flash nonvolatile byte in the Flash configuration field at global address 0x3_FF0E located in P-Flash memory (see Table 28-4) as indicated by reset condition F in Figure 28-22. If a double bit fault is detected while reading the P-Flash phrase containing the Flash nonvolatile byte during the reset sequence, all bits in the FOPT register will be set.

Table 29-13. FCNFG Field Descriptions

Field	Description
7 CCIE	**Command Complete Interrupt Enable** — The CCIE bit controls interrupt generation when a Flash command has completed. 0 Command complete interrupt disabled 1 An interrupt will be requested whenever the CCIF flag in the FSTAT register is set (see Section 29.3.2.7)
4 IGNSF	**Ignore Single Bit Fault** — The IGNSF controls single bit fault reporting in the FERSTAT register (see Section 29.3.2.8). 0 All single bit faults detected during array reads are reported 1 Single bit faults detected during array reads are not reported and the single bit fault interrupt will not be generated
1 FDFD	**Force Double Bit Fault Detect** — The FDFD bit allows the user to simulate a double bit fault during Flash array read operations and check the associated interrupt routine. The FDFD bit is cleared by writing a 0 to FDFD. 0 Flash array read operations will set the DFDIF flag in the FERSTAT register only if a double bit fault is detected 1 Any Flash array read operation will force the DFDIF flag in the FERSTAT register to be set (see Section 29.3.2.7) and an interrupt will be generated as long as the DFDIE interrupt enable in the FERCNFG register is set (see Section 29.3.2.6)
0 FSFD	**Force Single Bit Fault Detect** — The FSFD bit allows the user to simulate a single bit fault during Flash array read operations and check the associated interrupt routine. The FSFD bit is cleared by writing a 0 to FSFD. 0 Flash array read operations will set the SFDIF flag in the FERSTAT register only if a single bit fault is detected 1 Flash array read operation will force the SFDIF flag in the FERSTAT register to be set (see Section 29.3.2.7) and an interrupt will be generated as long as the SFDIE interrupt enable in the FERCNFG register is set (see Section 29.3.2.6)

29.3.2.6 Flash Error Configuration Register (FERCNFG)

The FERCNFG register enables the Flash error interrupts for the FERSTAT flags.

Offset Module Base + 0x0005

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	DFDIE	SFDIE
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 29-10. Flash Error Configuration Register (FERCNFG)

All assigned bits in the FERCNFG register are readable and writable.

Table A-5. Thermal Package Characteristics[1]

Num	C	Rating	Symbol	S12GN32, S12GNA32, S12GN16, S12GNA16	S12G64, S12GA64, S12G48, S12GN48, S12GA64	S12G128, S12GA128, S12G96, S12GA96	S12G240, S12GA240, S12G192, S12GA192	Unit
48-pin QFN								
22	D	Thermal resistance single sided PCB, natural convection[2]	θ_{JA}	82				°C/W
23	D	Thermal resistance single sided PCB @ 200 ft/min[3]	θ_{JMA}	67				°C/W
24	D	Thermal resistance double sided PCB with 2 internal planes, natural convection[3]	θ_{JA}	28				°C/W
25	D	Thermal resistance double sided PCB with 2 internal planes @ 200 ft/min[3]	θ_{JMA}	23				°C/W
26	D	Junction to Board[4]	θ_{JB}	11				°C/W
27	D	Junction to Case[5]	θ_{JC}	N/A				°C/W
28	D	Junction to Package Top[6]	Ψ_{JT}	4				°C/W
64-pin LQFP								
29	D	Thermal resistance single sided PCB, natural convection[2]	θ_{JA}		70	70	70	°C/W
30	D	Thermal resistance single sided PCB @ 200 ft/min[3]	θ_{JMA}		59	58	58	°C/W
31	D	Thermal resistance double sided PCB with 2 internal planes, natural convection[3]	θ_{JA}		52	52	52	°C/W
32	D	Thermal resistance double sided PCB with 2 internal planes @ 200 ft/min[3]	θ_{JMA}		46	46	45	°C/W
33	D	Junction to Board[4]	θ_{JB}		34	34	35	°C/W
34	D	Junction to Case[5]	θ_{JC}		20	18	17	°C/W
35	D	Junction to Package Top[6]	Ψ_{JT}		5	4	N/A	°C/W
100-pin LQFP								
36	D	Thermal resistance single sided PCB, natural convection[2]	θ_{JA}			61	62	°C/W
37	D	Thermal resistance single sided PCB @ 200 ft/min[3]	θ_{JMA}			51	55	°C/W
38	D	Thermal resistance double sided PCB with 2 internal planes, natural convection[3]	θ_{JA}			49	51	°C/W
39	D	Thermal resistance double sided PCB with 2 internal planes @ 200 ft/min[3]	θ_{JMA}			43	47	°C/W
40	D	Junction to Board[4]	θ_{JB}			34	37	°C/W
41	D	Junction to Case[5]	θ_{JC}			16	17	°C/W
42	D	Junction to Package Top[6]	Ψ_{JT}			3	N/A	°C/W

2 These values include the quantization error which is inherently 1/2 count for any A/D converter.

Table A-26. ADC Conversion Performance 3.3V range (Junction Temperature From +150°C To +160°C)

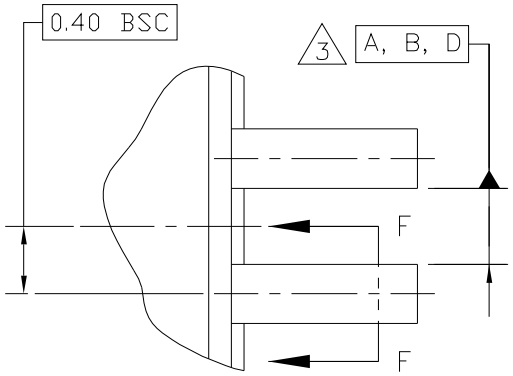
S12GNA16, S12GNA32								
Supply voltage 3.13V < V_{DDA} < 4.5 V, 150°C < T_J < 160°C, V_{REF} = V_{RH} - V_{RL} = V_{DDA}, f_{ADCCLK} = 8.0MHz The values are tested to be valid with no port AD output drivers switching simultaneous with conversions.								
Num	**C**	**Rating[1]**		**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	M	Resolution	12-Bit	LSB		0.80		mV
2	M	Differential Nonlinearity	12-Bit	DNL		±3		counts
3	M	Integral Nonlinearity	12-Bit	INL		±3		counts
4	M	Absolute Error[2]	12-Bit	AE		±4		counts
5	C	Resolution	10-Bit	LSB		3.22		mV
6	C	Differential Nonlinearity	10-Bit	DNL		±1		counts
7	C	Integral Nonlinearity	10-Bit	INL		±1		counts
8	C	Absolute Error[2]	10-Bit	AE		±2		counts
9	C	Resolution	8-Bit	LSB		12.89		mV
10	C	Differential Nonlinearity	8-Bit	DNL		±0.3		counts
11	C	Integral Nonlinearity	8-Bit	INL		±0.5		counts
12	C	Absolute Error[2]	8-Bit	AE		±1		counts

1 The 8-bit and 10-bit mode operation is structurally tested in production test. Absolute values are tested in 12-bit mode.

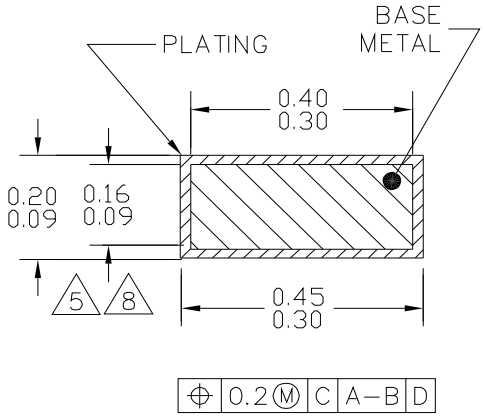
2 These values include the quantization error which is inherently 1/2 count for any A/D converter.

Table A-27. ADC Conversion Performance 3.3V range (Junction Temperature From –40°C To +150°C)

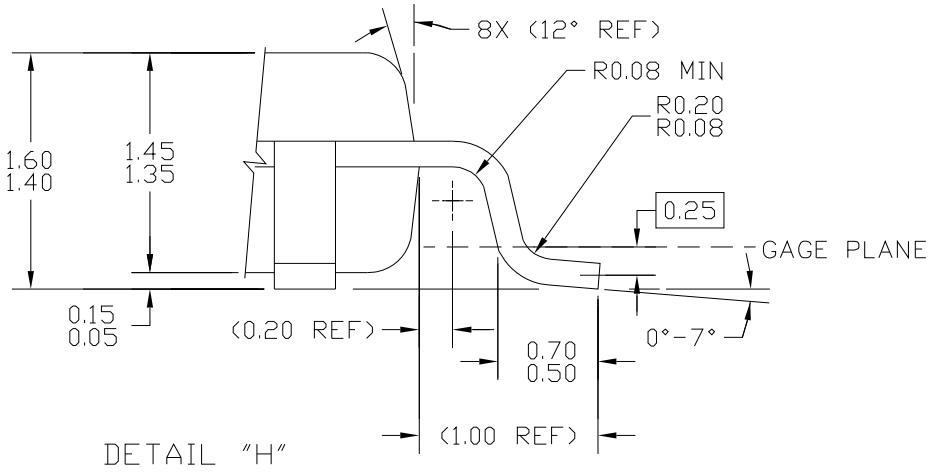
S12GN16, S12GN32, S12GN48, S12G48, S12G64, S12G96, S12G128, S12G192, and S12G240								
Supply voltage 3.13V < V_{DDA} < 4.5 V, -40°C < T_J < 150°C, V_{REF} = V_{RH} - V_{RL} = V_{DDA}, f_{ADCCLK} = 8.0MHz The values are tested to be valid with no port AD output drivers switching simultaneous with conversions.								
Num	**C**	**Rating[1]**		**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	P	Resolution	10-Bit	LSB		3.22		mV
2	P	Differential Nonlinearity	10-Bit	DNL	-1.5	±1	1.5	counts
3	P	Integral Nonlinearity	10-Bit	INL	-2	±1	2	counts
4	P	Absolute Error[2]	10-Bit[3] 10-Bit[4]	AE	-3 -4	±2 ±2	3 4	counts
5	C	Resolution	8-Bit	LSB		12.89		mV
6	C	Differential Nonlinearity	8-Bit	DNL	-0.5	±0.3	0.5	counts
7	C	Integral Nonlinearity	8-Bit	INL	-1	±0.5	1	counts
8	C	Absolute Error[2]	8-Bit	AE	-1.5	±1	1.5	counts



DETAIL G



SECTION F–F
ROTATED 90°CW
32 PLACES



DETAIL "H"

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	CASE NUMBER: 873A-03	19 MAY 2005
	STANDARD: JEDEC MS-026 BBA	