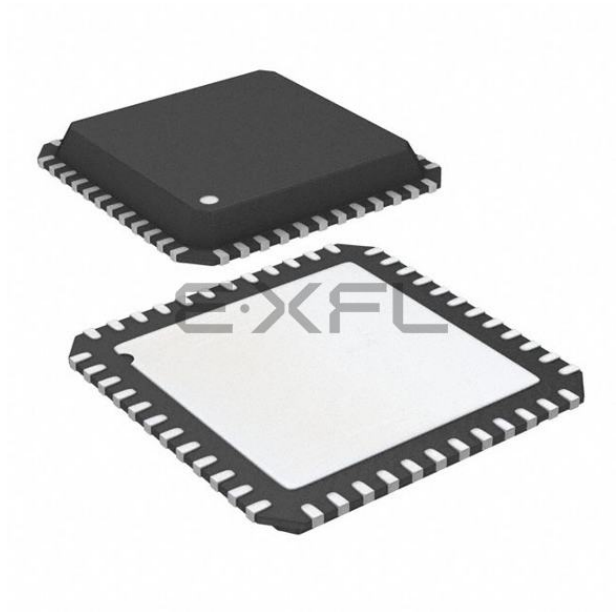

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Product Status	Active
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Connectivity	IrDA, LINbus, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	40
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3.13V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-TFQFN Exposed Pad
Supplier Device Package	48-QFN-EP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s9s12gn32f0cft

Table 1-30. 64-Pin LQFP Pinout for S12GA192 and S12GA240

	Function <----lowest-----PRIORITY-----highest---->					Power Supply	Internal Pull Resistor	
Package Pin	**Pin**	**2nd Func.**	**3rd Func.**	**4th Func**	**5th Func**		**CTRL**	**Reset State**
57	PS5	MOSI0	—	—	—	V_{DDX}	PERS/PPSS	Up
58	PS6	SCK0	—	—	—	V_{DDX}	PERS/PPSS	Up
59	PS7	API_EXTCLK	ECLK	$\overline{SS0}$	—	V_{DDX}	PERS/PPSS	Up
60	PM0	RXCAN	—	—	—	V_{DDX}	PERM/PPSM	Disabled
61	PM1	TXCAN	—	—	—	V_{DDX}	PERM/PPSM	Disabled
62	PM2	RXD2	—	—	—	V_{DDX}	PERM/PPSM	Disabled
63	PM3	TXD2	—	—	—	V_{DDX}	PERM/PPSM	Disabled
64	PJ7	KWJ7	$\overline{SS2}$	—	—	V_{DDX}	PERJ/PPSJ	Up

[1] The regular I/O characteristics (see Section A.2, “I/O Characteristics”) apply if the EXTAL/XTAL function is disabled

2.3.8 Pins PS7-0

Table 2-12. Port S Pins PS7-0

PS7	• The SPI0 $\overline{SS}$ signal is mapped to this pin when used with the SPI function. Depending on the configuration of the enabled SPI0 the I/O state is forced to be input or output. • 20 TSSOP: The SCI0 TXD signal is mapped to this pin when used with the SCI function. If the SCI0 TXD signal is enabled and routed here the I/O state will depend on the SCI0 configuration. • 20 TSSOP: The PWM channel 3 signal is mapped to this pin when used with the PWM function. If the PWM channel is enabled and routed here the I/O state is forced to output.The enabled PWM channel forces the I/O state to be an output. • 32 LQFP: The PWM channel 5 signal is mapped to this pin when used with the PWM function. The enabled PWM channel forces the I/O state to be an output. • 64/48/32/20 LQFP: The ECLK signal is mapped to this pin when used with the external clock function. If the ECLK output is enabled the I/O state will be forced to output. • The API_EXTCLK signal is mapped to this pin when used with the external clock function. If the Autonomous Periodic Interrupt clock is enabled and routed here the I/O state is forced to output. • 20 TSSOP: The ADC ETRIG3 signal is mapped to this pin if PWM channel 3 is routed here. The enabled external trigger function has no effect on the I/O state. Refer to Section 2.6.4, “ADC External Triggers ETRIG3-0”. • Signal priority: 20 TSSOP: $\overline{SS0}$ > TXD0 > PWM3 > ECLK > API_EXTCLK > GPO 32 LQFP: $\overline{SS0}$ > PWM5 > ECLK > API_EXTCLK > GPO 48/64 LQFP: $\overline{SS0}$ > ECLK > API_EXTCLK > GPO 100 LQFP: $\overline{SS0}$ > API_EXTCLK > GPO
PS6	• The SPI0 SCK signal is mapped to this pin when used with the SPI function. Depending on the configuration of the enabled SPI0 the I/O state is forced to be input or output. • 20 TSSOP: The TIM channel 3 signal is mapped to this pin when used with the timer function. If the TIM output compare signal is enabled and routed here the I/O state will be forced to output. • 32 LQFP: The TIM channel 5 signal is mapped to this pin when used with the timer function. If the TIM output compare signal is enabled and routed here the I/O state will be forced to output. If the ACMP timer link is enabled this pin is disconnected from the timer input so that it can still be used as general-purpose I/O or as timer output. The use case for the ACMP timer link requires the timer input capture function to be enabled. • Signal priority: 20 TSSOP: SCK0 > IOC3 > GPO 32 LQFP: SCK0 > IOC5 > GPO Others: SCK0 > GPO
PS5	• The SPI0 MOSI signal is mapped to this pin when used with the SPI function. Depending on the configuration of the enabled SPI0 the I/O state is forced to be input or output. • 20 TSSOP: The TIM channel 2 signal is mapped to this pin when used with the timer function. If the TIM output compare signal is enabled and routed here the I/O state will be forced to output. • 32 LQFP: The TIM channel 4 signal is mapped to this pin when used with the timer function. If the TIM output compare signal is enabled and routed here the I/O state will be forced to output. • Signal priority: 20 TSSOP: MOSI0 > IOC2 > GPO 32 LQFP: MOSI0 > IOC4 > GPO Others: MOSI0 > GPO

Table 2-20. Block Register Map (G2) (continued)

Global Address Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x027B PPS1AD	R	PPS1AD7	PPS1AD6	PPS1AD5	PPS1AD4	PPS1AD3	PPS1AD2	PPS1AD1	PPS1AD0
	W								
0x027C PIE0AD	R	PIE0AD7	PIE0AD6	PIE0AD5	PIE0AD4	PIE0AD3	PIE0AD2	PIE0AD1	PIE0AD0
	W								
0x027D PIE1AD	R	PIE1AD7	PIE1AD6	PIE1AD5	PIE1AD4	PIE1AD3	PIE1AD2	PIE1AD1	PIE1AD0
	W								
0x027E PIF0AD	R	PIF0AD7	PIF0AD6	PIF0AD5	PIF0AD4	PIF0AD3	PIF0AD2	PIF0AD1	PIF0AD0
	W								
0x027F PIF1AD	R	PIF1AD7	PIF1AD6	PIF1AD5	PIF1AD4	PIF1AD3	PIF1AD2	PIF1AD1	PIF1AD0
	W								

= Unimplemented or Reserved

2.4.2.3 Block Register Map (G3)

Table 2-21. Block Register Map (G3)

Global Address Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0000–0x0007 Reserved	R	0	0	0	0	0	0	0	0
	W								
0x0008 PORTE	R	0	0	0	0	0	0	PE1	PE0
	W								
0x0009 DDRE	R	0	0	0	0	0	0	DDRE1	DDRE0
	W								
0x000A–0x000B Non-PIM Address Range	R	Non-PIM Address Range							
	W								
0x000C PUCR	R	0	BKPUE	0	PDPEE	0	0	0	0
	W								
0x000D Reserved	R	0	0	0	0	0	0	0	0
	W								

= Unimplemented or Reserved

Table 5-8. Global Address Ranges

	S12GN16	S12GN32	S12G48, S12GN48	S12G64	S12G96	S12G128	S12G192	S12G240
0x04000-0x07FFF (NVMRES=1)	Internal NVM Resources (for details refer to section FTMRG)							
0x04000-0x07FFF (NVMRES=0)	Unimplemented						Reserved	Flash
0x08000-0x0FFFF								
0x08000-0x1FFFF								
0x20000-0x27FFF					Reserved			
0x28000-0x2FFFF								
0x30000-0x33FFF			Reserved					
0x34000-0x37FFF								
0x38000-0x3BFFF	Reserved							
0x3C000-0x3FFFF	16k	32k	48k	64k	96k	128k	192k	240k

5.4.4 Prioritization of Memory Accesses

On S12G devices, the CPU and the BDM are not able to access the memory in parallel. An arbitration occurs whenever both modules attempt a memory access at the same time. CPU accesses are handled with higher priority than BDM accesses unless the BDM module has been stalled for more then 128 bus cycles. In this case the pending BDM access will be processed immediately.

5.4.5 Interrupts

The S12GMMC does not generate any interrupts.

Table 8-14. State Control Register Access Encoding

COMRV	Visible State Control Register
01	DBGSCR2
10	DBGSCR3
11	DBGMFR

8.3.2.7.1 Debug State Control Register 1 (DBGSCR1)

Address: 0x0027

	7	6	5	4	3	2	1	0
R	0	0	0	0	SC3	SC2	SC1	SC0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 8-9. Debug State Control Register 1 (DBGSCR1)

Read: If COMRV[1:0] = 00

Write: If COMRV[1:0] = 00 and DBG is not armed.

This register is visible at 0x0027 only with COMRV[1:0] = 00. The state control register 1 selects the targeted next state whilst in State1. The matches refer to the match channels of the comparator match control logic as depicted in Figure 8-1 and described in Section 8.3.2.8.1, “Debug Comparator Control Register (DBGXCTL). Comparators must be enabled by setting the comparator enable bit in the associated DBGXCTL control register.

Table 8-15. DBGSCR1 Field Descriptions

Field	Description
3–0 SC[3:0]	These bits select the targeted next state whilst in State1, based upon the match event.

Table 8-16. State1 Sequencer Next State Selection

SC[3:0]	Description (Unspecified matches have no effect)
0000	Any match to Final State
0001	Match1 to State3
0010	Match2 to State2
0011	Match1 to State2
0100	Match0 to State2..... Match1 to State3
0101	Match1 to State3.....Match0 to Final State
0110	Match0 to State2..... Match2 to State3
0111	Either Match0 or Match1 to State2
1000	Reserved
1001	Match0 to State3

8.4.5.1.1 Storing with Begin Trigger Alignment

Storing with begin alignment, data is not stored in the Trace Buffer until the Final State is entered. Once the trigger condition is met the DBG module remains armed until 64 lines are stored in the Trace Buffer. If the trigger is at the address of the change-of-flow instruction the change of flow associated with the trigger is stored in the Trace Buffer. Using begin alignment together with tagging, if the tagged instruction is about to be executed then the trace is started. Upon completion of the tracing session the breakpoint is generated, thus the breakpoint does not occur at the tagged instruction boundary.

8.4.5.1.2 Storing with End Trigger Alignment

Storing with end alignment, data is stored in the Trace Buffer until the Final State is entered, at which point the DBG module becomes disarmed and no more data is stored. If the trigger is at the address of a change of flow instruction, the trigger event is not stored in the Trace Buffer. If all trace buffer lines have been used before a trigger event occurrs then the trace continues at the first line, overwriting the oldest entries.

8.4.5.2 Trace Modes

Four trace modes are available. The mode is selected using the TRCMOD bits in the DBGTCR register. Tracing is enabled using the TSOURCE bit in the DBGTCR register. The modes are described in the following subsections.

8.4.5.2.1 Normal Mode

In Normal Mode, change of flow (COF) program counter (PC) addresses are stored.

COF addresses are defined as follows:

- Source address of taken conditional branches (long, short, bit-conditional, and loop primitives)
- Destination address of indexed JMP, JSR, and CALL instruction
- Destination address of RTI, RTS, and RTC instructions
- Vector address of interrupts, except for BDM vectors

LBRA, BRA, BSR, BGND as well as non-indexed JMP, JSR, and CALL instructions are not classified as change of flow and are not stored in the trace buffer.

Stored information includes the full 18-bit address bus and information bits, which contains a source/destination bit to indicate whether the stored address was a source address or destination address.

NOTE

When a COF instruction with destination address is executed, the destination address is stored to the trace buffer on instruction completion, indicating the COF has taken place. If an interrupt occurs simultaneously then the next instruction carried out is actually from the interrupt service routine. The instruction at the destination address of the original program flow gets executed after the interrupt service routine.

to erase the EEPROM and Flash memory without giving access to their contents. After erasing both Flash memory and EEPROM, another reset into special single chip mode will cause the blank check to succeed and the options/security byte can be programmed to “unsecured” state via BDM.

While the BDM is executing the blank check, the BDM interface is completely blocked, which means that all BDM commands are temporarily blocked.

9.1.5 Unsecuring the Microcontroller

Unsecuring the microcontroller can be done by three different methods:

1. Backdoor key access
2. Reprogramming the security bits
3. Complete memory erase (special modes)

9.1.5.1 Unsecuring the MCU Using the Backdoor Key Access

In normal modes (single chip and expanded), security can be temporarily disabled using the backdoor key access method. This method requires that:

- The backdoor key at 0xFF00–0xFF07 (= global addresses 0x3_FF00–0x3_FF07) has been programmed to a valid value.
- The KEYEN[1:0] bits within the Flash options/security byte select ‘enabled’.
- In single chip mode, the application program programmed into the microcontroller must be designed to have the capability to write to the backdoor key locations.

The backdoor key values themselves would not normally be stored within the application data, which means the application program would have to be designed to receive the backdoor key values from an external source (e.g. through a serial port).

The backdoor key access method allows debugging of a secured microcontroller without having to erase the Flash. This is particularly useful for failure analysis.

NOTE

No word of the backdoor key is allowed to have the value 0x0000 or 0xFFFF.

9.1.6 Reprogramming the Security Bits

In normal single chip mode (NS), security can also be disabled by erasing and reprogramming the security bits within Flash options/security byte to the unsecured value. Because the erase operation will erase the entire sector from 0xFE00–0xFFFF (0x7F_FE00–0x7F_FFFF), the backdoor key and the interrupt vectors will also be erased; this method is not recommended for normal single chip mode. The application software can only erase and program the Flash options/security byte if the Flash sector containing the Flash options/security byte is not protected (see Flash protection). Thus Flash protection is a useful means of preventing this method. The microcontroller will enter the unsecured state after the next reset following the programming of the security bits to the unsecured value.

Table 11-9. Examples of ideal decimal ATD Results

Input Signal VRL = 0 Volts VRH = 5.12 Volts	8-Bit Codes (resolution=20mV)	10-Bit Codes (resolution=5mV)	Reserved
5.120 Volts	255	1023	Reserved
...	...	...	
0.022	1	4	
0.020	1	4	
0.018	1	4	
0.016	1	3	
0.014	1	3	
0.012	1	2	
0.010	1	2	
0.008	0	2	
0.006	0	1	
0.004	0	1	
0.003	0	1	
0.002	0	0	
0.000	0	0	

Table 11-10. Conversion Sequence Length Coding

S8C	S4C	S2C	S1C	Number of Conversions per Sequence
0	0	0	0	8
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	8
1	0	1	0	8
1	0	1	1	8
1	1	0	0	8
1	1	0	1	8
1	1	1	0	8
1	1	1	1	8

Table 11-11. ATD Behavior in Freeze Mode (Breakpoint)

FRZ1	FRZ0	Behavior in Freeze Mode
0	0	Continue conversion

Table 15-11. ATD Behavior in Freeze Mode (Breakpoint)

FRZ1	FRZ0	Behavior in Freeze Mode
0	1	Reserved
1	0	Finish current conversion, then freeze
1	1	Freeze Immediately

15.3.2.5 ATD Control Register 4 (ATDCTL4)

Writes to this register will abort current conversion sequence.

Module Base + 0x0004

	7	6	5	4	3	2	1	0
R W	SMP2	SMP1	SMP0	PRS[4:0]				
Reset	0	0	0	0	0	1	0	1

Figure 15-7. ATD Control Register 4 (ATDCTL4)

Read: Anytime

Write: Anytime

Table 15-12. ATDCTL4 Field Descriptions

Field	Description
7–5 SMP[2:0]	**Sample Time Select** — These three bits select the length of the sample time in units of ATD conversion clock cycles. Note that the ATD conversion clock period is itself a function of the prescaler value (bits PRS4-0). Table 15-13 lists the available sample time lengths.
4–0 PRS[4:0]	**ATD Clock Prescaler** — These 5 bits are the binary prescaler value PRS. The ATD conversion clock frequency is calculated as follows: $f_{ATDCLK} = \frac{f_{BUS}}{2 \times (PRS + 1)}$ Refer to Device Specification for allowed frequency range of f_{ATDCLK}.

Table 15-13. Sample Time Select

SMP2	SMP1	SMP0	Sample Time in Number of ATD Clock Cycles
0	0	0	4
0	0	1	6
0	1	0	8
0	1	1	10
1	0	0	12
1	0	1	16
1	1	0	20
1	1	1	24

24.4.4.3 Valid Flash Module Commands

Table 24-25 present the valid Flash commands, as enabled by the combination of the functional MCU mode (Normal SingleChip NS, Special Singlechip SS) with the MCU security state (Unsecured, Secured).

Special Singlechip mode is selected by input mmc_ss_mode_ts2 asserted. MCU Secured state is selected by input mmc_secure input asserted.

Table 24-25. Flash Commands by Mode and Security State

FCMD	Command	Unsecured		Secured	
		NS[1]	SS[2]	NS[3]	SS[4]
0x01	Erase Verify All Blocks	*	*	*	*
0x02	Erase Verify Block	*	*	*	*
0x03	Erase Verify P-Flash Section	*	*	*	
0x04	Read Once	*	*	*	
0x06	Program P-Flash	*	*	*	
0x07	Program Once	*	*	*	
0x08	Erase All Blocks		*		*
0x09	Erase Flash Block	*	*	*	
0x0A	Erase P-Flash Sector	*	*	*	
0x0B	Unsecure Flash		*		*
0x0C	Verify Backdoor Access Key	*		*	
0x0D	Set User Margin Level	*	*	*	
0x0E	Set Field Margin Level		*		
0x10	Erase Verify EEPROM Section	*	*	*	
0x11	Program EEPROM	*	*	*	
0x12	Erase EEPROM Sector	*	*	*	

1 Unsecured Normal Single Chip mode
2 Unsecured Special Single Chip mode.
3 Secured Normal Single Chip mode.
4 Secured Special Single Chip mode.

24.4.4.4 P-Flash Commands

Table 24-26 summarizes the valid P-Flash commands along with the effects of the commands on the P-Flash block and other resources within the Flash module.

Table 24-26. P-Flash Commands

FCMD	Command	Function on P-Flash Memory
0x01	Erase Verify All Blocks	Verify that all P-Flash (and EEPROM) blocks are erased.

Chapter 27
64 KByte Flash Module (S12FTMRG64K1V1)

Table 27-1. Revision History

Revision Number	Revision Date	Sections Affected	Description of Changes
V01.04	17 Jun 2010	27.4.6.1/27-950 27.4.6.2/27-951 27.4.6.3/27-951 27.4.6.14/27-961	Clarify Erase Verify Commands Descriptions related to the bits MGSTAT[1:0] of the register FSTAT.
V01.05	20 aug 2010	27.4.6.2/27-951 27.4.6.12/27-958 27.4.6.13/27-960	Updated description of the commands RD1BLK, MLOADU and MLOADF
Rev.1.27	31 Jan 2011	27.3.2.9/27-933	Updated description of protection on Section 27.3.2.9

27.1 Introduction

The FTMRG64K1 module implements the following:

- 64Kbytes of P-Flash (Program Flash) memory
- 2 Kbytes of EEPROM memory

The Flash memory is ideal for single-supply applications allowing for field reprogramming without requiring external high voltage sources for program or erase operations. The Flash module includes a memory controller that executes commands to modify Flash memory contents. The user interface to the memory controller consists of the indexed Flash Common Command Object (FCCOB) register which is written to with the command, global address, data, and any required command parameters. The memory controller must complete the execution of a command before the FCCOB register can be written to with a new command.

CAUTION

A Flash word or phrase must be in the erased state before being programmed. Cumulative programming of bits within a Flash word or phrase is not allowed.

The Flash memory may be read as bytes and aligned words. Read access time is one bus cycle for bytes and aligned words. For misaligned words access, the CPU has to perform twice the byte read access command. For Flash memory, an erased bit reads 1 and a programmed bit reads 0.

Offset Module Base + 0x000E

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 27-20. Flash Reserved3 Register (FRSV3)

All bits in the FRSV3 register read 0 and are not writable.

27.3.2.15 Flash Reserved4 Register (FRSV4)

This Flash register is reserved for factory testing.

Offset Module Base + 0x000F

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 27-21. Flash Reserved4 Register (FRSV4)

All bits in the FRSV4 register read 0 and are not writable.

27.3.2.16 Flash Option Register (FOPT)

The FOPT register is the Flash option register.

Offset Module Base + 0x0010

	7	6	5	4	3	2	1	0
R	NV[7:0]							
W								
Reset	F[1]	F[1]	F[1]	F[1]	F[1]	F[1]	F[1]	F[1]

= Unimplemented or Reserved

Figure 27-22. Flash Option Register (FOPT)

1 Loaded from IFR Flash configuration field, during reset sequence.

All bits in the FOPT register are readable but are not writable.

During the reset sequence, the FOPT register is loaded from the Flash nonvolatile byte in the Flash configuration field at global address 0x3_FF0E located in P-Flash memory (see Table 27-4) as indicated by reset condition F in Figure 27-22. If a double bit fault is detected while reading the P-Flash phrase containing the Flash nonvolatile byte during the reset sequence, all bits in the FOPT register will be set.

29.4.6 Flash Command Description

This section provides details of all available Flash commands launched by a command write sequence. The ACCERR bit in the FSTAT register will be set during the command write sequence if any of the following illegal steps are performed, causing the command not to be processed by the Memory Controller:

- Starting any command write sequence that programs or erases Flash memory before initializing the FCLKDIV register
- Writing an invalid command as part of the command write sequence
- For additional possible errors, refer to the error handling table provided for each command

If a Flash block is read during execution of an algorithm (CCIF = 0) on that same block, the read operation will return invalid data if both flags SFDIF and DFDIF are set. If the SFDIF or DFDIF flags were not previously set when the invalid read operation occurred, both the SFDIF and DFDIF flags will be set.

If the ACCERR or FPVIOL bits are set in the FSTAT register, the user must clear these bits before starting any command write sequence (see Section 29.3.2.7).

CAUTION

A Flash word or phrase must be in the erased state before being programmed. Cumulative programming of bits within a Flash word or phrase is not allowed.

29.4.6.1 Erase Verify All Blocks Command

The Erase Verify All Blocks command will verify that all P-Flash and EEPROM blocks have been erased.

Table 29-31. Erase Verify All Blocks Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x01	Not required

Upon clearing CCIF to launch the Erase Verify All Blocks command, the Memory Controller will verify that the entire Flash memory space is erased. The CCIF flag will set after the Erase Verify All Blocks operation has completed. If all blocks are not erased, it means blank check failed, both MGSTAT bits will be set.

Table 29-32. Erase Verify All Blocks Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 000 at command launch
	FPVIOL	None
	MGSTAT1	Set if any errors have been encountered during the reador if blank check failed .
	MGSTAT0	Set if any non-correctable errors have been encountered during the read or if blank check failed.

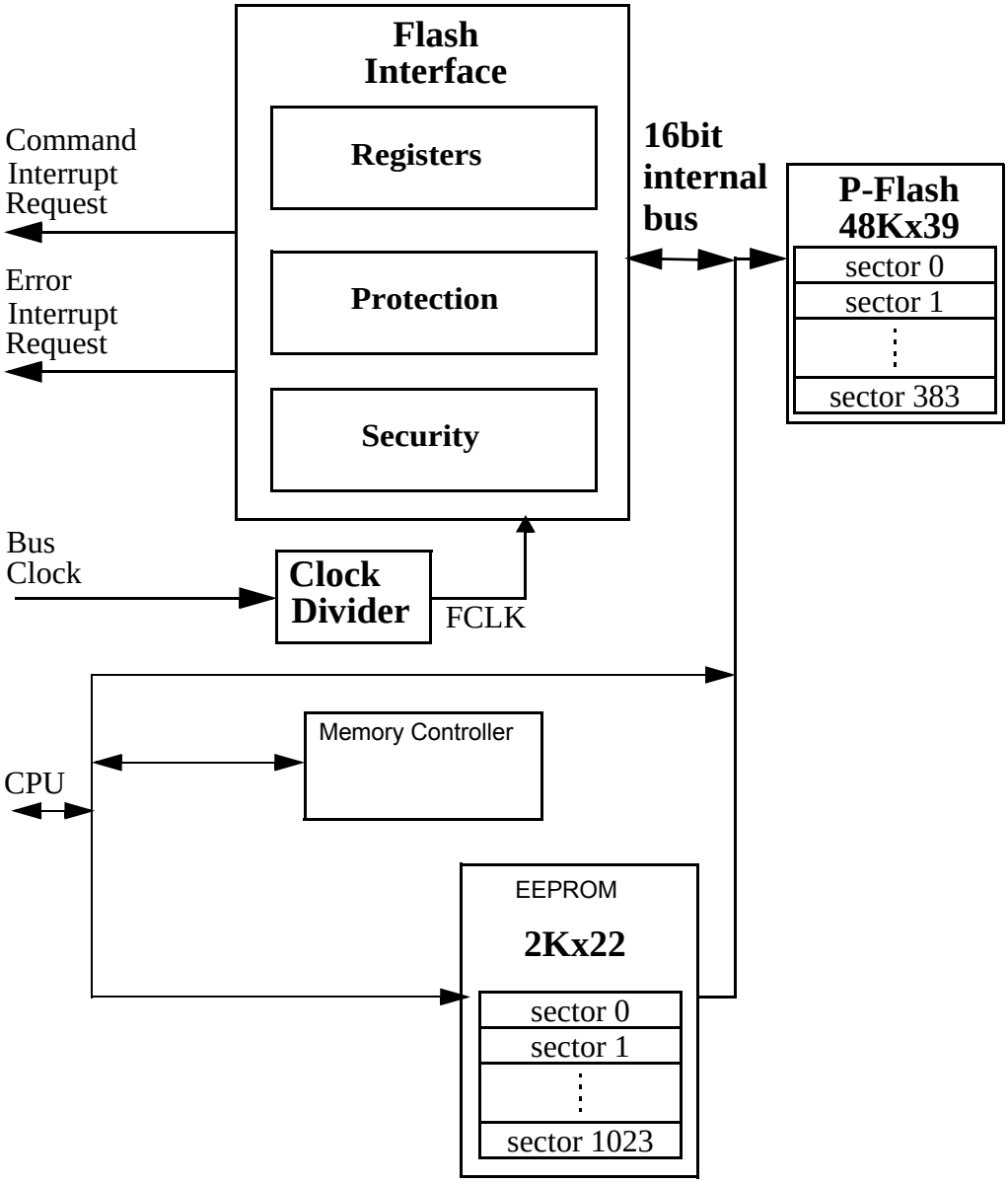

Figure 30-1. FTMRG192K2 Block Diagram

30.2 External Signal Description

The Flash module contains no signals that connect off-chip.

Offset Module Base + 0x0013

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 30-25. Flash Reserved7 Register (FRSV7)

All bits in the FRSV7 register read 0 and are not writable.

30.4 Functional Description

30.4.1 Modes of Operation

The FTMRG192K2 module provides the modes of operation normal and special . The operating mode is determined by module-level inputs and affects the FCLKDIV, FCNFG, and EEPROT registers (see Table 30-27).

30.4.2 IFR Version ID Word

The version ID word is stored in the IFR at address 0x0_40B6. The contents of the word are defined in Table 30-26.

Table 30-26. IFR Version ID Fields

[15:4]	[3:0]
Reserved	VERNUM

0x0040–0x067 Timer Module (TIM)

0x0050 – 0x005F	TCxH – TCxL	R	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		W								
		R	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		W								
0x0060	PACTL	R	0	PAEN	PAMOD	PEDGE	CLK1	CLK0	PAOVI	PAI
		W								
0x0061	PAFLG	R	0	0	0	0	0	0	PAOVF	PAIF
		W								
0x0062	PACNTH	R	PACNT15	PACNT14	PACNT13	PACNT12	PACNT11	PACNT10	PACNT9	PACNT8
		W								
0x0063	PACNTL	R	PACNT7	PACNT6	PACNT5	PACNT4	PACNT3	PACNT2	PACNT1	PACNT0
		W								
0x0064- 0x006B	Reserved	R								
		W								
0x006C	OCPD	R	OCPD7	OCPD6	OCPD5	OCPD4	OCPD3	OCPD2	OCPD1	OCPD0
		W								
0x006D	Reserved	R								
		W								
0x006E	PTPSR	R	PTPS7	PTPS6	PTPS5	PTPS4	PTPS3	PTPS2	PTPS1	PTPS0
		W								
0x006F	Reserved	R								
		W								

0x0070–0x09F Analog to Digital Converter (ADC)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0070	ATDCTL0	R	Reserved	0	0	0	WRAP3	WRAP2	WRAP1	WRAP0
		W								
0x0071	ATDCTL1	R	ETRIGSEL	SRES1	SRES0	SMP_DIS	ETRIGCH 3	ETRIGCH 2	ETRIGCH 1	ETRIGCH 0
		W								
0x0072	ATDCTL2	R	0	AFFC	Reseved	ETRIGLE	ETRIGP	ETRIGE	ASCIE	ACMPIE
		W								
0x0073	ATDCTL3	R	DJM	S8C	S4C	S2C	S1C	FIFO	FRZ1	FRZ0
		W								
0x0074	ATDCTL4	R	SMP2	SMP1	SMP0	PRS[4:0]				
		W								
0x0075	ATDCTL5	R	0	SC	SCAN	MULT	CD	CC	CB	CA
		W								
0x0076	ATDSTAT0	R	SCF	0	ETORF	FIFOR	CC3	CC2	CC1	CC0
		W								
0x0077	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0078	ATDCMPEH	R	CMPE[15:8]							
		W								
0x0079	ATDCMPEL	R	CMPE[7:0]							
		W								

0x0140–0x017F CAN Controller (MSCAN)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0140	CANCTL0	R	RXFRM	RXACT	CSWAI	SYNCH	TIME	WUPE	SLPRQ	INITRQ
		W								
0x0141	CANCTL1	R	CANE	CLKSRC	LOOPB	LISTEN	BORM	WUPM	SLPAK	INITAK
		W								
0x0142	CANBTR0	R	SJW1	SJW0	BRP5	BRP4	BRP3	BRP2	BRP1	BRP0
		W								
0x0143	CANBTR1	R	SAMP	TSEG22	TSEG21	TSEG20	TSEG13	TSEG12	TSEG11	TSEG10
		W								
0x0144	CANRFLG	R	WUPIF	CSCIF	RSTAT1	RSTAT0	TSTAT1	TSTAT0	OVRIF	RXF
		W								
0x0145	CANRIER	R	WUPIE	CSCIE	RSTATE1	RSTATE0	TSTATE1	TSTATE0	OVRIE	RXFIE
		W								
0x0146	CANTFLG	R	0	0	0	0	0	TXE2	TXE1	TXE0
		W								
0x0147	CANTIER	R	0	0	0	0	0	TXEIE2	TXEIE1	TXEIE0
		W								
0x0148	CANTARQ	R	0	0	0	0	0	ABTRQ2	ABTRQ1	ABTRQ0
		W								
0x0149	CANTAAK	R	0	0	0	0	0	ABTAK2	ABTAK1	ABTAK0
		W								
0x014A	CANTBSEL	R	0	0	0	0	0	TX2	TX1	TX0
		W								
0x014B	CANIDAC	R	0	0	IDAM1	IDAM0	0	IDHIT2	IDHIT1	IDHIT0
		W								
0x014C	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x014D	CANMISC	R	0	0	0	0	0	0	0	BOHOLD
		W								
0x014E	CANRXERR	R	RXERR7	RXERR6	RXERR5	RXERR4	RXERR3	RXERR2	RXERR1	RXERR0
		W								
0x014F	CANTXERR	R	TXERR7	TXERR6	TXERR5	TXERR4	TXERR3	TXERR2	TXERR1	TXERR0
		W								
0x0150-0x0153	CANIDAR0–3	R	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
		W								
0x0154-0x0157	CANIDMRx	R	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
		W								
0x0158-0x015B	CANIDAR4–7	R	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
		W								
0x015C-0x015F	CANIDMR4–7	R	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
		W								
0x0160-0x016F	CANRXFG	R	See Section 18.3.3, “Programmer’s Model of Message Storage”							
		W								
0x0170-0x017F	CANTXFG	R	See Section 18.3.3, “Programmer’s Model of Message Storage”							
		W								

0x02F0–0x02FF Clock and Power Management (CPMU) Map 2 of 2

0x02FB	CPMUPROT	R	0	0	0	0	0	0	0	PROT
		W								
0x02FC	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x02FD-0x02FF	Reserved	R	0	0	0	0	0	0	0	0
		W								

0x0300–0x03BF Reserved

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0300-0x03BF	Reserved	R	0	0	0	0	0	0	0	0
		W								

0x03C0–0x03C7 Digital to Analog Converter (DAC0)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x03C0	DAC0CTL	R	FVR	Drive	0	0	0	Mode[2:0]		
		W								
0x03C1	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x03C2	DAC0VOLTAGE	R	Voltage[7:0]							
		W								
0x03C3	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x03C4	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x03C5	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x03C6	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x03C7	Reserved	R	0	0	0	0	0	0	0	0
		W								

0x03C8–0x03CF Digital to Analog Converter (DAC1)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x03C8	DAC1CTL	R	FVR	Drive	0	0	0	Mode[2:0]		
		W								
0x03C9	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x03CA	DAC1VOLTAGE	R	Voltage[7:0]							
		W								
0x03CB	Reserved	R	0	0	0	0	0	0	0	0
		W								

Appendix C
Ordering and Shipping Information

Revision History

Version Number	Revision Date	Description of Changes
Rev 0.01	2-Jan-2009	Initial release
Rev 0.02	22-Nov-2012	Added temperature option W
Rev 0.03	25-Jan-2013	• Updated C.1, “Ordering Information” (added KGD option) • Added C.2, “KGD Shipping Information”
Rev 0.04	1-Feb-2013	• Removed C.2, “KGD Shipping Information”

C.1 Ordering Information

The following figure provides an ordering part number example for the devices covered by this data book. There are two options when ordering a device. Customers must choose between ordering either the mask-specific part number or the generic / mask-independent part number. Ordering the mask-specific part number enables the customer to specify which particular mask set they will receive whereas ordering the generic mask set means that FSL will ship the currently preferred mask set (which may change over time).

In either case, the marking on the device will always show the generic / mask-independent part number and the mask set number.

NOTE

The mask identifier suffix and the Tape & Reel suffix are always both omitted from the part number which is actually marked on the device.

For specific part numbers to order, please contact your local sales office. The below figure illustrates the structure of a typical mask-specific ordering number for the MC9S12G devices