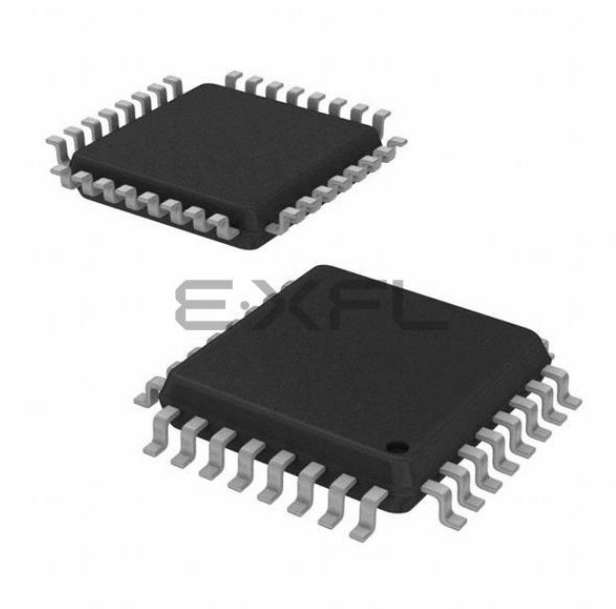

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Details	
Product Status	Active
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Speed	25MHz
Connectivity	IrDA, LINbus, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	26
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3.13V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s9s12gn32f1vlcr

5 Preset by factory.

6 Routing register only available on G(A)240 and G(A)192 only. Takes only effect if the PKGCR is set to 100 LQFP.

2.4.2 Register Map

The following tables show the individual register maps of groups G1 (Table 2-19), G2 (Table 2-20) and G3 (Table 2-21).

NOTE

To maintain SW compatibility write data to unimplemented register bits must be zero.

2.4.2.1 Block Register Map (G1)

Table 2-19. Block Register Map (G1)

Global Address Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0000 PORTA	R	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
	W								
0x0001 PORTB	R	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
	W								
0x0002 DDRA	R	DDRA7	DDRA6	DDRA5	DDRA4	DDRA3	DDRA2	DDRA1	DDRA0
	W								
0x0003 DDRB	R	DDRB7	DDRB6	DDRB5	DDRB4	DDRB3	DDRB2	DDRB1	DDRB0
	W								
0x0004 PORTC	R	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
	W								
0x0005 PORTD	R	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
	W								
0x0006 DDRC	R	DDRC7	DDRC6	DDRC5	DDRC4	DDRC3	DDRC2	DDRC1	DDRC0
	W								
0x0007 DDRD	R	DDRD7	DDRD6	DDRD5	DDRD4	DDRD3	DDRD2	DDRD1	DDRD0
	W								
0x0008 PORTE	R	0	0	0	0	0	0	PE1	PE0
	W								
0x0009 DDRE	R	0	0	0	0	0	0	DDRE1	DDRE0
	W								

= Unimplemented or Reserved

Table 2-50. IOC2 Routing Options

PRR0T21	PRR0T20	IOC2 Associated Pin
0	0	PS5 - IOC2
0	1	PE0 - IOC2
1	0	PAD4 - IOC2
1	1	Reserved

Table 2-51. SCI0 Routing Options

PRR0S1	PRR0S0	SCI0 Associated Pin
0	0	PE0 - RXD, PE1 - TXD
0	1	PS4 - RXD, PS7 - TXD
1	0	PAD4 - RXD, PAD5 - TXD
1	1	Reserved

2.4.3.27 Port M Data Register (PTM)

Address 0x0250 (G1, G2) Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	0	0	0	0	PTM3	PTM2	PTM1	PTM0
W								
Reset	0	0	0	0	0	0	0	0

Address 0x0250 (G3) Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	PTM1	PTM0
W								
Reset	0	0	0	0	0	0	0	0

Figure 2-28. Port M Data Register (PTM)

[1] Read: Anytime. The data source is depending on the data direction value.
Write: Anytime

Table 2-52. PTM Register Field Descriptions

Field	Description
3-0 PTM	**Port M general-purpose input/output data**—Data Register When not used with an alternative signal, the associated pin can be used as general-purpose I/O. In general-purpose output mode the port data register bit value is driven to the pin. If the associated data direction bit is set to 1, a read returns the value of the port data register bit, otherwise the buffered pin input state is read.

2.4.3.43 Port J Input Register (PTIJ)

Address 0x0269 (G1, G2) Access: User read only[1]

	7	6	5	4	3	2	1	0
R	PTIJ7	PTIJ6	PTIJ5	PTIJ4	PTIJ3	PTIJ2	PTIJ1	PTIJ0
W								
Reset	0	0	0	0	0	0	0	0

Address 0x0269 (G3) Access: User read only[1]

	7	6	5	4	3	2	1	0
R	0	0	0	0	PTIJ3	PTIJ2	PTIJ1	PTIJ0
W								
Reset	0	0	0	0	0	0	0	0

Figure 2-43. Port J Input Register (PTIJ)

[1] Read: Anytime
Write:Never

Table 2-69. PTIJ Register Field Descriptions

Field	Description
7-0 PTIJ	**Port J input data—** A read always returns the buffered input state of the associated pin. It can be used to detect overload or short circuit conditions on output pins.

2.4.3.44 Port J Data Direction Register (DDRJ)

Address 0x026A (G1, G2) Access: User read/write[1]

	7	6	5	4	3	2	1	0
R W	DDRJ7	DDRJ6	DDRJ5	DDRJ4	DDRJ3	DDRJ2	DDRJ1	DDRJ0
Reset	0	0	0	0	0	0	0	0

Address 0x026A (G3) Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	0	0	0	0	DDRJ3	DDRJ2	DDRJ1	DDRJ0
W								
Reset	0	0	0	0	0	0	0	0

Figure 2-44. Port J Data Direction Register (DDRJ)

[1] Read: Anytime
Write: Anytime

2.5 PIM Ports - Functional Description

2.5.1 General

Each pin except BKGD can act as general-purpose I/O. In addition most pins can act as an output or input of a peripheral module.

2.5.2 Registers

A set of configuration registers is common to all ports with exception of the ADC port (Table 2-91). All registers can be written at any time, however a specific configuration might not become active.

Example: Selecting a pullup device. This device does not become active while the port is used as a push-pull output.

Table 2-91. Register availability per port[1]

Port	Data (Portx, PTx)	Input (PTIx)	Data Direction (DDRx)	Pull Enable (PERx)	Polarity Select (PPSx)	Wired-Or Mode (WOMx)	Interrupt Enable (PIEx)	Interrupt Flag (PIFx)
A	yes	-	yes	yes	-	-	-	-
B	yes	-	yes		-	-	-	-
C	yes	-	yes		-	-	-	-
D	yes	-	yes		-	-	-	-
E	yes	-	yes		-	-	-	-
T	yes	yes	yes	yes	yes	-	-	-
S	yes	yes	yes	yes	yes	yes	-	-
M	yes	yes	yes	yes	yes	yes	-	-
P	yes	yes	yes	yes	yes	-	yes	yes
J	yes	yes	yes	yes	yes	-	yes	yes
AD	yes	yes	yes	yes	yes	-	yes	yes

[1] Each cell represents one register with individual configuration bits

2.5.2.1 Data Register (PORTx, PTx)

This register holds the value driven out to the pin if the pin is used as a general-purpose I/O.

Writing to this register has only an effect on the pin if the pin is used as general-purpose output. When reading this address, the buffered state of the pin is returned if the associated data direction register bit is set to 0.

If the data direction register bits are set to 1, the contents of the data register is returned. This is independent of any other configuration (Figure 2-64).

2.5.2.2 Input Register (PTIx)

This register is read-only and always returns the buffered state of the pin (Figure 2-64).

Chapter 8
S12S Debug Module (S12SDBGV2)

Table 8-1. Revision History

Revision Number	Revision Date	Sections Affected	Summary of Changes
02.08	09.MAY.2008	General	Spelling corrections. Revision history format changed.
02.09	29.MAY.2008	8.4.5.4	Added note for end aligned, PurePC, rollover case.
02.10	27.SEP.2012	General	Changed cross reference formats

8.1 Introduction

The S12SDBG module provides an on-chip trace buffer with flexible triggering capability to allow non-intrusive debug of application software. The S12SDBG module is optimized for S12SCPU debugging.

Typically the S12SDBG module is used in conjunction with the S12SBDM module, whereby the user configures the S12SDBG module for a debugging session over the BDM interface. Once configured the S12SDBG module is armed and the device leaves BDM returning control to the user program, which is then monitored by the S12SDBG module. Alternatively the S12SDBG module can be configured over a serial interface using SWI routines.

8.1.1 Glossary Of Terms

COF: Change Of Flow. Change in the program flow due to a conditional branch, indexed jump or interrupt

BDM: Background Debug Mode

S12SBDM: Background Debug Module

DUG: Device User Guide, describing the features of the device into which the DBG is integrated

WORD: 16-bit data entity

Data Line: 20-bit data entity

CPU: S12SCPU module

DBG: S12SDBG module

POR: Power On Reset

On simultaneous matches the lowest channel number has priority so with this configuration the forking from State1 has the peculiar effect that a simultaneous match0/match1 transitions to final state but a simultaneous match2/match1transitions to state2.

8.5.9 Scenario 8

Trigger when a routine/event at M2 follows either M1 or M0.

Figure 8-37. Scenario 8a

Trigger when an event M2 is followed by either event M0 or event M1

Figure 8-38. Scenario 8b

Scenario 8a and 8b are possible with the S12SDBGV1 and S12SDBGV2 SCR encoding

8.5.10 Scenario 9

Trigger when a routine/event at A (M2) does not follow either B or C (M1 or M0) before they are executed again. This cannot be realized with theS12SDBGV1 SCR encoding due to OR limitations. By changing the SCR2 encoding as shown in red this scenario becomes possible.

Figure 8-39. Scenario 9

8.5.11 Scenario 10

Trigger if an event M0 occurs following up to two successive M2 events without the resetting event M1. As shown up to 2 consecutive M2 events are allowed, whereby a reset to State1 is possible after either one or two M2 events. If an event M0 occurs following the second M2, before M1 resets to State1 then a trigger

11.3.2.4 ATD Control Register 3 (ATDCTL3)

Writes to this register will abort current conversion sequence.

Module Base + 0x0003

	7	6	5	4	3	2	1	0
R W	DJM	S8C	S4C	S2C	S1C	FIFO	FRZ1	FRZ0
Reset	0	0	1	0	0	0	0	0

= Unimplemented or Reserved

Figure 11-6. ATD Control Register 3 (ATDCTL3)

Read: Anytime

Write: Anytime

Table 11-8. ATDCTL3 Field Descriptions

Field	Description
7 DJM	**Result Register Data Justification** — Result data format is always unsigned. This bit controls justification of conversion data in the result registers. 0 Left justified data in the result registers. 1 Right justified data in the result registers. Table 11-9 gives example ATD results for an input signal range between 0 and 5.12 Volts.
6–3 S8C, S4C, S2C, S1C	**Conversion Sequence Length** — These bits control the number of conversions per sequence. Table 11-10 shows all combinations. At reset, S4C is set to 1 (sequence length is 4). This is to maintain software continuity to HC12 family.
2 FIFO	**Result Register FIFO Mode** — If this bit is zero (non-FIFO mode), the A/D conversion results map into the result registers based on the conversion sequence; the result of the first conversion appears in the first result register (ATDDR0), the second result in the second result register (ATDDR1), and so on. If this bit is one (FIFO mode) the conversion counter is not reset at the beginning or end of a conversion sequence; sequential conversion results are placed in consecutive result registers. In a continuously scanning conversion sequence, the result register counter will wrap around when it reaches the end of the result register file. The conversion counter value (CC3-0 in ATDSTAT0) can be used to determine where in the result register file, the current conversion result will be placed. Aborting a conversion or starting a new conversion clears the conversion counter even if FIFO=1. So the first result of a new conversion sequence, started by writing to ATDCTL5, will always be place in the first result register (ATDDDR0). Intended usage of FIFO mode is continuos conversion (SCAN=1) or triggered conversion (ETRIG=1). Which result registers hold valid data can be tracked using the conversion complete flags. Fast flag clear mode may be useful in a particular application to track valid data. If this bit is one, automatic compare of result registers is always disabled, that is ADC10B8C will behave as if ACMPIE and all CPME[*n*] were zero. 0 Conversion results are placed in the corresponding result register up to the selected sequence length. 1 Conversion results are placed in consecutive result registers (wrap around at end).
1–0 FRZ[1:0]	**Background Debug Freeze Enable** — When debugging an application, it is useful in many cases to have the ATD pause when a breakpoint (Freeze Mode) is encountered. These 2 bits determine how the ATD will respond to a breakpoint as shown in Table 11-11. Leakage onto the storage node and comparator reference capacitors may compromise the accuracy of an immediately frozen conversion depending on the length of the freeze period.

14.1.3 Block Diagram

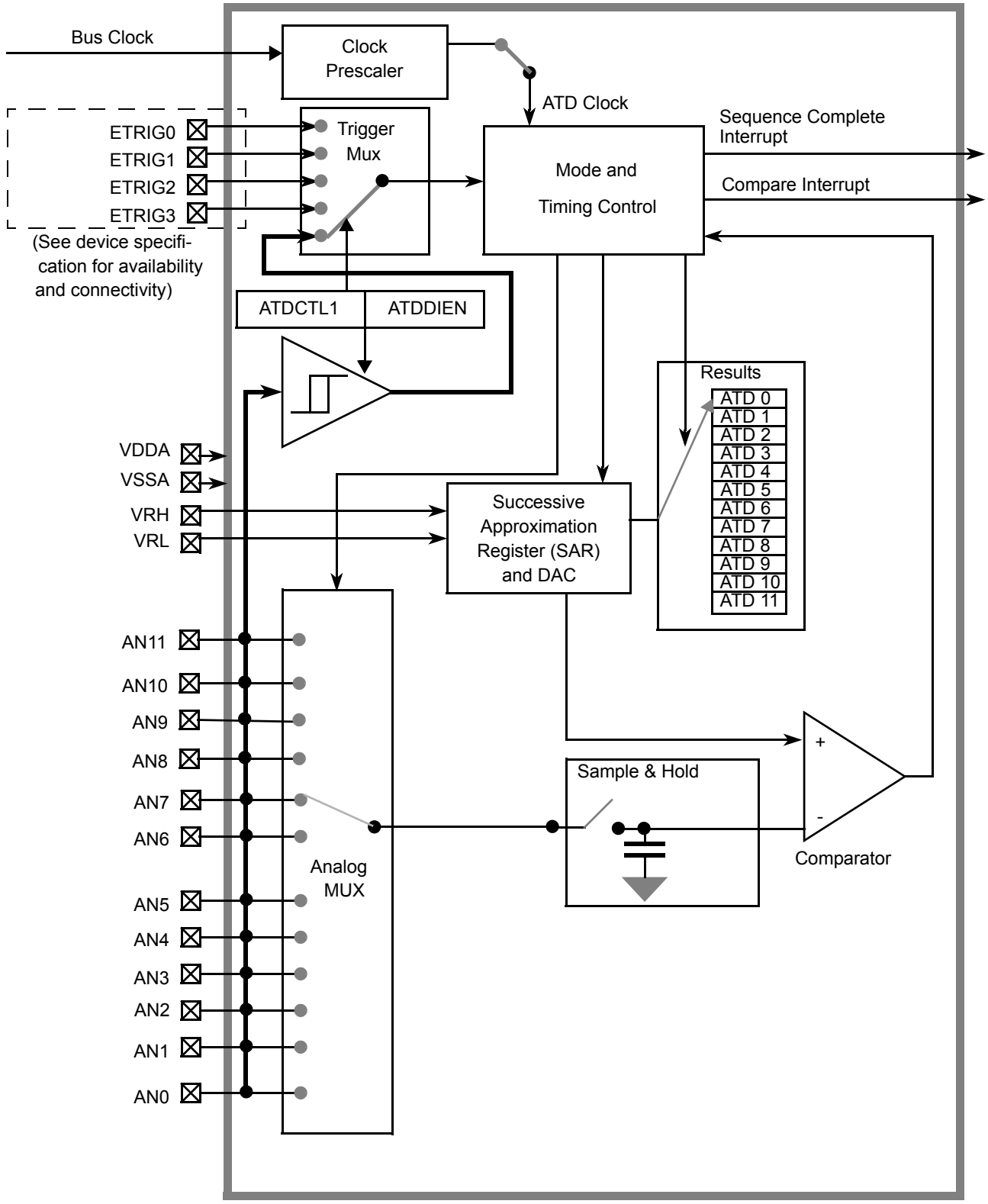

Figure 14-1. ADC12B12C Block Diagram

Chapter 16
Analog-to-Digital Converter (ADC12B16CV2)

Revision History

Version Number	Revision Date	Effective Date	Author	Description of Changes
V02.00	18 June 2009	18 June 2009		Initial version copied 12 channel block guide
V02.01	09 Feb 2010	09 Feb 2010		Updated Table 16-15 Analog Input Channel Select Coding - description of internal channels. Updated register ATDDR (left/right justified result) description in section 16.3.2.12.1/16-554 and 16.3.2.12.2/16-555 and added Table 16-21 to improve feature description. Fixed typo in Table 16-9 - conversion result for 3mV and 10bit resolution
V02.03	26 Feb 2010	26 Feb 2010		Corrected Table 16-15 Analog Input Channel Select Coding - description of internal channels.
V02.04	26 Mar 2010	16 Mar 2010		Corrected typo: Reset value of ATDDIEN register
V02.05	14 Apr 2010	14 Apr 2010		Corrected typos to be in-line with SoC level pin naming conventions for VDDA, VSSA, VRL and VRH.
V02.06	25 Aug 2010	25 Aug 2010		Removed feature of conversion during STOP and general wording clean up done in Section 16.4, “Functional Description
v02.07	09 Sep 2010	09 Sep 2010		Update of internal only information.
V02.08	11 Feb 2011	11 Feb 2011		Connectivity Information regarding internal channel_6 added to Table 16-15.
V02.09	29 Mar 2011	29 Mar 2011		Fixed typo in bit description field Table 16-14 for bits CD, CC, CB, CA. Last sentence contained a wrong highest channel number (it is not AN7 to AN0 instead it is AN15 to AN0).
V02.10	22. Jun 2012	22. Jun 2012		Updated register wirte access information in section 16.3.2.9/16-552
V02.11	29. Jun 2012	29. Jun 2012		Removed IP name in block diagram Figure 16-1
V02.12	02 Oct 2012	02 Oct 2012		Added user information to avoid maybe false external trigger events when enabling the external trigger mode (Section 16.4.2.1, “External Trigger Input).

Table 18-12. CANRIER Register Field Descriptions

Field	Description
7 WUPIE[1]	**Wake-Up Interrupt Enable** 0 No interrupt request is generated from this event. 1 A wake-up event causes a Wake-Up interrupt request.
6 CSCIE	**CAN Status Change Interrupt Enable** 0 No interrupt request is generated from this event. 1 A CAN Status Change event causes an error interrupt request.
5-4 RSTATE[1:0]	**Receiver Status Change Enable** — These RSTAT enable bits control the sensitivity level in which receiver state changes are causing CSCIF interrupts. Independent of the chosen sensitivity level the RSTAT flags continue to indicate the actual receiver state and are only updated if no CSCIF interrupt is pending. 00 Do not generate any CSCIF interrupt caused by receiver state changes. 01 Generate CSCIF interrupt only if the receiver enters or leaves “bus-off” state. Discard other receiver state changes for generating CSCIF interrupt. 10 Generate CSCIF interrupt only if the receiver enters or leaves “RxErr” or “bus-off”[2] state. Discard other receiver state changes for generating CSCIF interrupt. 11 Generate CSCIF interrupt on all state changes.
3-2 TSTATE[1:0]	**Transmitter Status Change Enable** — These TSTAT enable bits control the sensitivity level in which transmitter state changes are causing CSCIF interrupts. Independent of the chosen sensitivity level, the TSTAT flags continue to indicate the actual transmitter state and are only updated if no CSCIF interrupt is pending. 00 Do not generate any CSCIF interrupt caused by transmitter state changes. 01 Generate CSCIF interrupt only if the transmitter enters or leaves “bus-off” state. Discard other transmitter state changes for generating CSCIF interrupt. 10 Generate CSCIF interrupt only if the transmitter enters or leaves “TxErr” or “bus-off” state. Discard other transmitter state changes for generating CSCIF interrupt. 11 Generate CSCIF interrupt on all state changes.
1 OVRIE	**Overrun Interrupt Enable** 0 No interrupt request is generated from this event. 1 An overrun event causes an error interrupt request.
0 RXFIE	**Receiver Full Interrupt Enable** 0 No interrupt request is generated from this event. 1 A receive buffer full (successful message reception) event causes a receiver interrupt request.

1 WUPIE and WUPE (see Section 18.3.2.1, “MSCAN Control Register 0 (CANCTL0)”) must both be enabled if the recovery mechanism from stop or wait is required.

2 Bus-off state is only defined for transmitters by the CAN standard (see Bosch CAN 2.0A/B protocol specification). Because the only possible state change for the transmitter from bus-off to TxOK also forces the receiver to skip its current state to RxOK, the coding of the RXSTAT[1:0] flags define an additional bus-off state for the receiver (see Section 18.3.2.5, “MSCAN Receiver Flag Register (CANRFLG)”).

18.3.2.7 MSCAN Transmitter Flag Register (CANTFLG)

The transmit buffer empty flags each have an associated interrupt enable bit in the CANTIER register.

Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0016 PWMPER2[2]	R	Bit 7	6	5	4	3	2	1	Bit 0
	W								
0x0017 PWMPER3[2]	R	Bit 7	6	5	4	3	2	1	Bit 0
	W								
0x0018 PWMPER4[2]	R	Bit 7	6	5	4	3	2	1	Bit 0
	W								
0x0019 PWMPER5[2]	R	Bit 7	6	5	4	3	2	1	Bit 0
	W								
0x001A PWMPER6[2]	R	Bit 7	6	5	4	3	2	1	Bit 0
	W								
0x001B PWMPER7[2]	R	Bit 7	6	5	4	3	2	1	Bit 0
	W								
0x001C PWMDTY0[2]	R	Bit 7	6	5	4	3	2	1	Bit 0
	W								
0x001D PWMDTY1[2]	R	Bit 7	6	5	4	3	2	1	Bit 0
	W								
0x001E PWMDTY2[2]	R	Bit 7	6	5	4	3	2	1	Bit 0
	W								
0x001F PWMDTY3[2]	R	Bit 7	6	5	4	3	2	1	Bit 0
	W								
0x0010 PWMDTY4[2]	R	Bit 7	6	5	4	3	2	1	Bit 0
	W								
0x0021 PWMDTY5[2]	R	Bit 7	6	5	4	3	2	1	Bit 0
	W								
0x0022 PWMDTY6[2]	R	Bit 7	6	5	4	3	2	1	Bit 0
	W								
0x0023 PWMDTY7[2]	R	Bit 7	6	5	4	3	2	1	Bit 0
	W								
0x0024 RESERVED	R	0	0	0	0	0	0	0	0
	W								
		= Unimplemented or Reserved							

Figure 19-2. The scalable PWM Register Summary (Sheet 1 of 4)

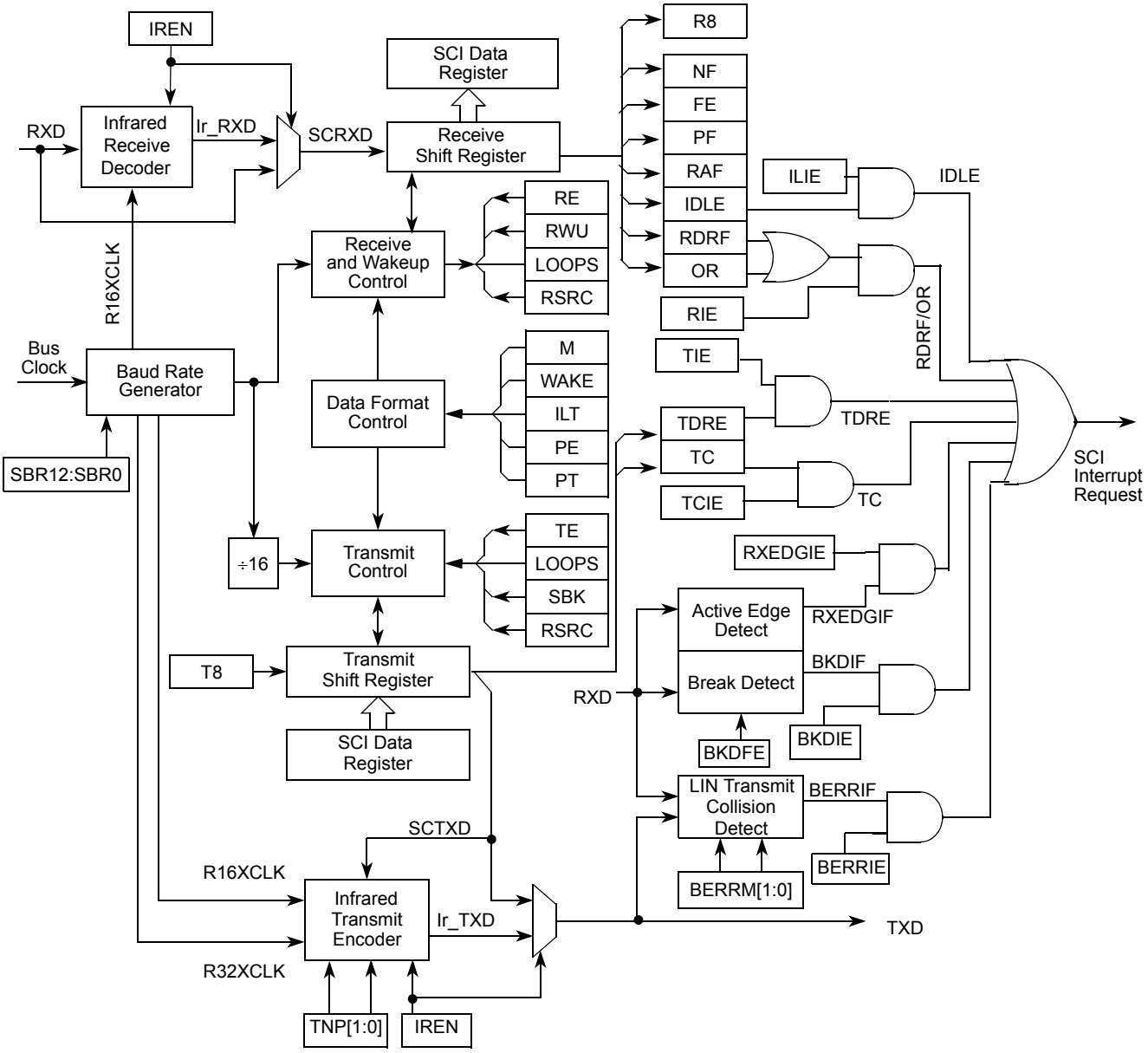

Figure 20-14. Detailed SCI Block Diagram

20.4.1 Infrared Interface Submodule

This module provides the capability of transmitting narrow pulses to an IR LED and receiving narrow pulses and transforming them to serial bits, which are sent to the SCI. The IrDA physical layer specification defines a half-duplex infrared communication link for exchange data. The full standard includes data rates up to 16 Mbits/s. This design covers only data rates between 2.4 Kbits/s and 115.2 Kbits/s.

The infrared submodule consists of two major blocks: the transmit encoder and the receive decoder. The SCI transmits serial bits of data which are encoded by the infrared submodule to transmit a narrow pulse

If MODFEN is set and SSOE is cleared, the $\overline{SS}$ pin is configured as input for detecting mode fault error. If the $\overline{SS}$ input becomes low this indicates a mode fault error where another master tries to drive the MOSI and SCK lines. In this case, the SPI immediately switches to slave mode, by clearing the MSTR bit and also disables the slave output buffer MISO (or SISO in bidirectional mode). So the result is that all outputs are disabled and SCK, MOSI, and MISO are inputs. If a transmission is in progress when the mode fault occurs, the transmission is aborted and the SPI is forced into idle state.

This mode fault error also sets the mode fault (MODF) flag in the SPI status register (SPISR). If the SPI interrupt enable bit (SPIE) is set when the MODF flag becomes set, then an SPI interrupt sequence is also requested.

When a write to the SPI data register in the master occurs, there is a half SCK-cycle delay. After the delay, SCK is started within the master. The rest of the transfer operation differs slightly, depending on the clock format specified by the SPI clock phase bit, CPHA, in SPI control register 1 (see Section 21.4.3, “Transmission Formats”).

NOTE

A change of the bits CPOL, CPHA, SSOE, LSBFE, XFRW, MODFEN, SPC0, or BIDIROE with SPC0 set, SPPR2-SPPR0 and SPR2-SPR0 in master mode will abort a transmission in progress and force the SPI into idle state. The remote slave cannot detect this, therefore the master must ensure that the remote slave is returned to idle state.

21.4.2 Slave Mode

The SPI operates in slave mode when the MSTR bit in SPI control register 1 is clear.

- Serial clock

  In slave mode, SCK is the SPI clock input from the master.

- MISO, MOSI pin

  In slave mode, the function of the serial data output pin (MISO) and serial data input pin (MOSI) is determined by the SPC0 bit and BIDIROE bit in SPI control register 2.

- $\overline{SS}$ pin

  The $\overline{SS}$ pin is the slave select input. Before a data transmission occurs, the $\overline{SS}$ pin of the slave SPI must be low. $\overline{SS}$ must remain low until the transmission is complete. If $\overline{SS}$ goes high, the SPI is forced into idle state.

  The $\overline{SS}$ input also controls the serial data output pin, if $\overline{SS}$ is high (not selected), the serial data output pin is high impedance, and, if $\overline{SS}$ is low, the first bit in the SPI data register is driven out of the serial data output pin. Also, if the slave is not selected ($\overline{SS}$ is high), then the SCK input is ignored and no internal shifting of the SPI shift register occurs.

  Although the SPI is capable of duplex operation, some SPI peripherals are capable of only receiving SPI data in a slave mode. For these simpler devices, there is no serial data out pin.

Chapter 25
32 KByte Flash Module (S12FTMRG32K1V1)

Table 25-1. Revision History

Revision Number	Revision Date	Sections Affected	Description of Changes
V01.04	17 Jun 2010	25.4.6.1/25-846 25.4.6.2/25-847 25.4.6.3/25-847 25.4.6.14/25-857	Clarify Erase Verify Commands Descriptions related to the bits MGSTAT[1:0] of the register FSTAT.
V01.05	20 aug 2010	25.4.6.2/25-847 25.4.6.12/25-854 25.4.6.13/25-856	Updated description of the commands RD1BLK, MLOADU and MLOADF
Rev.1.27	31 Jan 2011	25.3.2.9/25-829	Updated description of protection on Section 25.3.2.9

25.1 Introduction

The FTMRG32K1 module implements the following:

- 32Kbytes of P-Flash (Program Flash) memory
- 1 Kbytes of EEPROM memory

The Flash memory is ideal for single-supply applications allowing for field reprogramming without requiring external high voltage sources for program or erase operations. The Flash module includes a memory controller that executes commands to modify Flash memory contents. The user interface to the memory controller consists of the indexed Flash Common Command Object (FCCOB) register which is written to with the command, global address, data, and any required command parameters. The memory controller must complete the execution of a command before the FCCOB register can be written to with a new command.

CAUTION

A Flash word or phrase must be in the erased state before being programmed. Cumulative programming of bits within a Flash word or phrase is not allowed.

The Flash memory may be read as bytes and aligned words. Read access time is one bus cycle for bytes and aligned words. For misaligned words access, the CPU has to perform twice the byte read access command. For Flash memory, an erased bit reads 1 and a programmed bit reads 0.

28.4.4.3 Valid Flash Module Commands

Table 28-27 present the valid Flash commands, as enabled by the combination of the functional MCU mode (Normal SingleChip NS, Special Singlechip SS) with the MCU security state (Unsecured, Secured).

Special Singlechip mode is selected by input mmc_ss_mode_ts2 asserted. MCU Secured state is selected by input mmc_secure input asserted.

Table 28-27. Flash Commands by Mode and Security State

FCMD	Command	Unsecured		Secured	
		NS[1]	SS[2]	NS[3]	SS[4]
0x01	Erase Verify All Blocks	*	*	*	*
0x02	Erase Verify Block	*	*	*	*
0x03	Erase Verify P-Flash Section	*	*	*	
0x04	Read Once	*	*	*	
0x06	Program P-Flash	*	*	*	
0x07	Program Once	*	*	*	
0x08	Erase All Blocks		*		*
0x09	Erase Flash Block	*	*	*	
0x0A	Erase P-Flash Sector	*	*	*	
0x0B	Unsecure Flash		*		*
0x0C	Verify Backdoor Access Key	*		*	
0x0D	Set User Margin Level	*	*	*	
0x0E	Set Field Margin Level		*		
0x10	Erase Verify EEPROM Section	*	*	*	
0x11	Program EEPROM	*	*	*	
0x12	Erase EEPROM Sector	*	*	*	

1 Unsecured Normal Single Chip mode
2 Unsecured Special Single Chip mode.
3 Secured Normal Single Chip mode.
4 Secured Special Single Chip mode.

28.4.4.4 P-Flash Commands

Table 28-28 summarizes the valid P-Flash commands along with the effects of the commands on the P-Flash block and other resources within the Flash module.

Table 28-28. P-Flash Commands

FCMD	Command	Function on P-Flash Memory
0x01	Erase Verify All Blocks	Verify that all P-Flash (and EEPROM) blocks are erased.

29.1.2 Features

29.1.2.1 P-Flash Features

- 128 Kbytes of P-Flash memory composed of one 128 Kbyte Flash block divided into 256 sectors of 512 bytes
- Single bit fault correction and double bit fault detection within a 32-bit double word during read operations
- Automated program and erase algorithm with verify and generation of ECC parity bits
- Fast sector erase and phrase program operation
- Ability to read the P-Flash memory while programming a word in the EEPROM memory
- Flexible protection scheme to prevent accidental program or erase of P-Flash memory

29.1.2.2 EEPROM Features

- 4 Kbytes of EEPROM memory composed of one 4 Kbyte Flash block divided into 1024 sectors of 4 bytes
- Single bit fault correction and double bit fault detection within a word during read operations
- Automated program and erase algorithm with verify and generation of ECC parity bits
- Fast sector erase and word program operation
- Protection scheme to prevent accidental program or erase of EEPROM memory
- Ability to program up to four words in a burst sequence

29.1.2.3 Other Flash Module Features

- No external high-voltage power supply required for Flash memory program and erase operations
- Interrupt generation on Flash command completion and Flash error detection
- Security mechanism to prevent unauthorized access to the Flash memory

29.1.3 Block Diagram

The block diagram of the Flash module is shown in Figure 29-1.

29.3.2.9 P-Flash Protection Register (FPROT)

The FPROT register defines which P-Flash sectors are protected against program and erase operations.

Offset Module Base + 0x0008

	7	6	5	4	3	2	1	0
R	FPOPEN	RNV6	FPHDIS	FPHS[1:0]		FPLDIS	FPLS[1:0]	
W								
Reset	F[1]	F[1]	F[1]	F[1]	F[1]	F[1]	F[1]	F[1]

= Unimplemented or Reserved

Figure 29-13. Flash Protection Register (FPROT)

[1] Loaded from IFR Flash configuration field, during reset sequence.

The (unreserved) bits of the FPROT register are writable with the restriction that the size of the protected region can only be increased (see Section 29.3.2.9.1, “P-Flash Protection Restrictions,” and Table 29-21).

During the reset sequence, the FPROT register is loaded with the contents of the P-Flash protection byte in the Flash configuration field at global address 0x3_FF0C located in P-Flash memory (see Table 29-4) as indicated by reset condition ‘F’ in Figure 29-13. To change the P-Flash protection that will be loaded during the reset sequence, the upper sector of the P-Flash memory must be unprotected, then the P-Flash protection byte must be reprogrammed. If a double bit fault is detected while reading the P-Flash phrase containing the P-Flash protection byte during the reset sequence, the FPOPEN bit will be cleared and remaining bits in the FPROT register will be set to leave the P-Flash memory fully protected.

Trying to alter data in any protected area in the P-Flash memory will result in a protection violation error and the FPVIOL bit will be set in the FSTAT register. The block erase of a P-Flash block is not possible if any of the P-Flash sectors contained in the same P-Flash block are protected.

Table 29-17. FPROT Field Descriptions

Field	Description
7 FPOPEN	**Flash Protection Operation Enable** — The FPOPEN bit determines the protection function for program or erase operations as shown in Table 29-18 for the P-Flash block. 0 When FPOPEN is clear, the FPHDIS and FPLDIS bits define unprotected address ranges as specified by the corresponding FPHS and FPLS bits 1 When FPOPEN is set, the FPHDIS and FPLDIS bits enable protection for the address range specified by the corresponding FPHS and FPLS bits
6 RNV[6]	**Reserved Nonvolatile Bit** — The RNV bit should remain in the erased state for future enhancements.
5 FPHDIS	**Flash Protection Higher Address Range Disable** — The FPHDIS bit determines whether there is a protected/unprotected area in a specific region of the P-Flash memory ending with global address 0x3_FFFF. 0 Protection/Unprotection enabled 1 Protection/Unprotection disabled
4–3 FPHS[1:0]	**Flash Protection Higher Address Size** — The FPHS bits determine the size of the protected/unprotected area in P-Flash memory as shown inTable 29-19. The FPHS bits can only be written to while the FPHDIS bit is set.

Table 29-59. Set Field Margin Level Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 001 at command launch
		Set if command not available in current mode (see Table 29-27)
		Set if an invalid FlashBlockSelectionCode[1:0] is supplied (See Table 29-34)
		Set if an invalid margin level setting is supplied
	FPVIOL	None
	MGSTAT1	None
	MGSTAT0	None

CAUTION

Field margin levels must only be used during verify of the initial factory programming.

NOTE

Field margin levels can be used to check that Flash memory contents have adequate margin for data retention at the normal level setting. If unexpected results are encountered when checking Flash memory contents at field margin levels, the Flash memory contents should be erased and reprogrammed.

29.4.6.14 Erase Verify EEPROM Section Command

The Erase Verify EEPROM Section command will verify that a section of code in the EEPROM is erased. The Erase Verify EEPROM Section command defines the starting point of the data to be verified and the number of words.

Table 29-60. Erase Verify EEPROM Section Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x10	Global address [17:16] to identify the EEPROM block
001	Global address [15:0] of the first word to be verified	
010	Number of words to be verified	

Upon clearing CCIF to launch the Erase Verify EEPROM Section command, the Memory Controller will verify the selected section of EEPROM memory is erased. The CCIF flag will set after the Erase Verify EEPROM Section operation has completed. If the section is not erased, it means blank check failed, both MGSTAT bits will be set.

Table A-18. Pseudo Stop Current Characteristics

Conditions are: V_{DDX}=5V, V_{DDR}=5V, V_{DDA}=5V, RTI and COP and API enabled, see Table A-12.							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
S12GN16, S12GN32							
1	C	-40°C	I_{DDPS}		155		µA
2	C	25°C	I_{DDPS}		165		µA
3	C	150°C	I_{DDPS}		265		µA
4	C	160°C	I_{DDPS}		295		µA
S12GN48, S12G48, S12G64							
5	C	-40°C	I_{DDPS}		160		µA
6	C	25°C	I_{DDPS}		170		µA
7	C	150°C	I_{DDPS}		285		µA
S12G96, S12G128							
8	C	-40°C	I_{DDPS}		165		µA
9	C	25°C	I_{DDPS}		175		µA
10	C	150°C	I_{DDPS}		320		µA
S12G192, S12GA192, S12G240, S12GA240							
11	C	-40°C	I_{DDPS}		175		µA
12	C	25°C	I_{DDPS}		185		µA
13	C	150°C	I_{DDPS}		430		µA

A.4 ADC Characteristics

This section describes the characteristics of the analog-to-digital converter.

A.4.1 ADC Operating Characteristics

The Table A-19 and Table A-20 show conditions under which the ADC operates.

The following constraints exist to obtain full-scale, full range results:

$$V_{SSA} \le V_{RL} \le V_{IN} \le V_{RH} \le V_{DDA}.$$

2 These values include the quantization error which is inherently 1/2 count for any A/D converter.

Table A-26. ADC Conversion Performance 3.3V range (Junction Temperature From +150°C To +160°C)

S12GNA16, S12GNA32								
Supply voltage 3.13V < V_{DDA} < 4.5 V, 150°C < T_J < 160°C, V_{REF} = V_{RH} - V_{RL} = V_{DDA}, f_{ADCCLK} = 8.0MHz The values are tested to be valid with no port AD output drivers switching simultaneous with conversions.								
Num	**C**	**Rating[1]**		**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	M	Resolution	12-Bit	LSB		0.80		mV
2	M	Differential Nonlinearity	12-Bit	DNL		±3		counts
3	M	Integral Nonlinearity	12-Bit	INL		±3		counts
4	M	Absolute Error[2]	12-Bit	AE		±4		counts
5	C	Resolution	10-Bit	LSB		3.22		mV
6	C	Differential Nonlinearity	10-Bit	DNL		±1		counts
7	C	Integral Nonlinearity	10-Bit	INL		±1		counts
8	C	Absolute Error[2]	10-Bit	AE		±2		counts
9	C	Resolution	8-Bit	LSB		12.89		mV
10	C	Differential Nonlinearity	8-Bit	DNL		±0.3		counts
11	C	Integral Nonlinearity	8-Bit	INL		±0.5		counts
12	C	Absolute Error[2]	8-Bit	AE		±1		counts

1 The 8-bit and 10-bit mode operation is structurally tested in production test. Absolute values are tested in 12-bit mode.

2 These values include the quantization error which is inherently 1/2 count for any A/D converter.

Table A-27. ADC Conversion Performance 3.3V range (Junction Temperature From –40°C To +150°C)

S12GN16, S12GN32, S12GN48, S12G48, S12G64, S12G96, S12G128, S12G192, and S12G240								
Supply voltage 3.13V < V_{DDA} < 4.5 V, -40°C < T_J < 150°C, V_{REF} = V_{RH} - V_{RL} = V_{DDA}, f_{ADCCLK} = 8.0MHz The values are tested to be valid with no port AD output drivers switching simultaneous with conversions.								
Num	**C**	**Rating[1]**		**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	P	Resolution	10-Bit	LSB		3.22		mV
2	P	Differential Nonlinearity	10-Bit	DNL	-1.5	±1	1.5	counts
3	P	Integral Nonlinearity	10-Bit	INL	-2	±1	2	counts
4	P	Absolute Error[2]	10-Bit[3] 10-Bit[4]	AE	-3 -4	±2 ±2	3 4	counts
5	C	Resolution	8-Bit	LSB		12.89		mV
6	C	Differential Nonlinearity	8-Bit	DNL	-0.5	±0.3	0.5	counts
7	C	Integral Nonlinearity	8-Bit	INL	-1	±0.5	1	counts
8	C	Absolute Error[2]	8-Bit	AE	-1.5	±1	1.5	counts