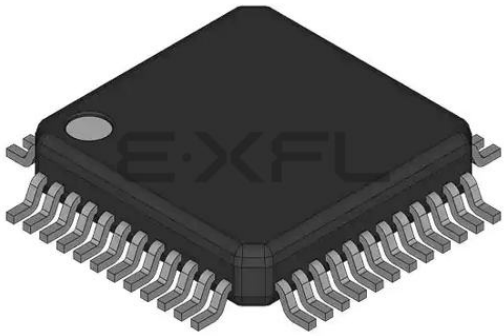

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Program Memory Type	FLASH
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1.7.3.1 VDDX[3:1]/VDDX, VSSX[3:1]/VSSX— Power and Ground Pins for I/O Drivers

External power and ground for I/O drivers. Bypass requirements depend on how heavily the MCU pins are loaded. All VDDX pins are connected together internally. All VSSX pins are connected together internally.

NOTE

Not all VDDX[3:1]/VDDX and VSSX[3:1]VSSX pins are available on all packages. Refer to section 1.8 Device Pinouts for further details.

1.7.3.2 VDDR — Power Pin for Internal Voltage Regulator

Power supply input to the internal voltage regulator.

NOTE

On some packages VDDR is bonded to VDDX and the pin is named VDDXR. Refer to section 1.8 Device Pinouts for further details.

1.7.3.3 VSS — Core Ground Pin

The voltage supply of nominally 1.8V is derived from the internal voltage regulator. The return current path is through the VSS pin.

1.7.3.4 VDDA, VSSA — Power Supply Pins for DAC,ACMP, RVA, ADC and Voltage Regulator

These are the power supply and ground input pins for the digital-to-analog converter, the analog comparator, the reference voltage attenuator, the analog-to-digital converter and the voltage regulator.

NOTE

On some packages VDDA is connected with VDDXR and the common pin is named VDDXRA.
On some packages the VSSA is connected to VSSX and the common pin is named VSSXA. See section Section 1.8, “Device Pinouts” for further details.

1.7.3.5 VRH — Reference Voltage Input Pin

V_{RH} is the reference voltage input pin for the digital-to-analog converter and the analog-to-digital converter. Refer to Section 1.18, “ADC VRH/VRL Signal Connection” for further details.

On some packages VRH is tied to VDDA or VDDXRA. Refer to section 1.8 Device Pinouts for further details.

Table 1-11. 48-Pin LQFP/QFN Pinout for S12GNA16 and S12GNA32

	Function <----lowest-----PRIORITY-----highest---->					Power Supply	Internal Pull Resistor	
Package Pin	Pin	2nd Func.	3rd Func.	4th Func	5th Func		CTRL	Reset State
2	VDDXR	—	—	—	—	—	—	—
3	VSSX	—	—	—	—	—	—	—
4	PE0[1]	EXTAL	—	—	—	V_{DDX}	PUCR/PDPEE	Down
5	VSS	—	—	—	—	—	—	—
6	PE1[1]	XTAL	—	—	—	V_{DDX}	PUCR/PDPEE	Down
7	TEST	—	—	—	—	N.A.	$\overline{\text{RESET}}$ pin	Down
8	PJ0	KWJ0	—	—	—	V_{DDX}	PERJ/PPSJ	Up
9	PJ1	KWJ1	—	—	—	V_{DDX}	PERJ/PPSJ	Up
10	PJ2	KWJ2	—	—	—	V_{DDX}	PERJ/PPSJ	Up
11	PJ3	KWJ3	—	—	—	V_{DDX}	PERJ/PPSJ	Up
12	BKGD	MODC	—	—	—	V_{DDX}	PUCR/BKPUE	Up
13	PP0	KWP0	ETRIG0	API_EXTCLK	PWM0	V_{DDX}	PERP/PPSP	Disabled
14	PP1	KWP1	ETRIG1	ECLKX2	PWM1	V_{DDX}	PERP/PPSP	Disabled
15	PP2	KWP2	ETRIG2	PWM2	—	V_{DDX}	PERP/PPSP	Disabled
16	PP3	KWP3	ETRIG3	PWM3	—	V_{DDX}	PERP/PPSP	Disabled
17	PP4	KWP4	PWM4	—	—	V_{DDX}	PERP/PPSP	Disabled
18	PP5	KWP5	PWM5	—	—	V_{DDX}	PERP/PPSP	Disabled
19	PT5	IOC5	—	—	—	V_{DDX}	PERT/PPST	Disabled
20	PT4	IOC4	—	—	—	V_{DDX}	PERT/PPST	Disabled
21	PT3	IOC3	—	—	—	V_{DDX}	PERT/PPST	Disabled
22	PT2	IOC2	—	—	—	V_{DDX}	PERT/PPST	Disabled
23	PT1	IOC1	$\overline{\text{IRQ}}$	—	—	V_{DDX}	PERT/PPST	Disabled
24	PT0	IOC0	$\overline{\text{XIRQ}}$	—	—	V_{DDX}	PERT/PPST	Disabled
25	PAD0	KWAD0	AN0	—	—	V_{DDA}	PER1AD/PPS1AD	Disabled
26	PAD8	KWAD8	—	—	—	V_{DDA}	PER0AD/PPS0AD	Disabled
27	PAD1	KWAD1	AN1	—	—	V_{DDA}	PER1AD/PPS1AD	Disabled
28	PAD9	KWAD9	ACMPO	—	—	V_{DDA}	PER0AD/PPS0AD	Disabled
29	PAD2	KWAD2	AN2	—	—	V_{DDA}	PER1AD/PPS1AD	Disabled

Table 1-22. 100-Pin LQFP Pinout for S12G96 and S12G128

	Function <----lowest-----PRIORITY-----highest---->				Power Supply	Internal Pull Resistor	
Package Pin	Pin	2nd Func.	3rd Func.	4th Func.		CTRL	Reset State
1	PJ6	KWJ6	SCK2	—	V_{DDX}	PERJ/PPSJ	Up
2	PJ5	KWJ5	MOSI2	—	V_{DDX}	PERJ/PPSJ	Up
3	PJ4	KWJ4	MISO2	—	V_{DDX}	PERJ/PPSJ	Up
4	PA0	—	—	—	V_{DDX}	PUCR/PUPAE	Disabled
5	PA1	—	—	—	V_{DDX}	PUCR/PUPAE	Disabled
6	PA2	—	—	—	V_{DDX}	PUCR/PUPAE	Disabled
7	PA3	—	—	—	V_{DDX}	PUCR/PUPAE	Disabled
8	RESET	—	—	—	V_{DDX}	PULLUP	
9	VDDX1	—	—	—	—	—	—
10	VDDR	—	—	—	—	—	—
11	VSSX1	—	—	—	—	—	—
12	PE0[1]	EXTAL	—	—	V_{DDX}	PUCR/PDPEE	Down
13	VSS	—	—	—	—	—	—
14	PE1[1]	XTAL	—	—	V_{DDX}	PUCR/PDPEE	Down
15	TEST	—	—	—	N.A.	$\overline{\text{RESET}}$ pin	Down
16	PA4	—	—	—	V_{DDX}	PUCR/PUPAE	Disabled
17	PA5	—	—	—	V_{DDX}	PUCR/PUPAE	Disabled
18	PA6	—	—	—	V_{DDX}	PUCR/PUPAE	Disabled
19	PA7	—	—	—	V_{DDX}	PUCR/PUPAE	Disabled
20	PJ0	KWJ0	MISO1	—	V_{DDX}	PERJ/PPSJ	Up
21	PJ1	KWJ1	MOSI1	—	V_{DDX}	PERJ/PPSJ	Up
22	PJ2	KWJ2	SCK1	—	V_{DDX}	PERJ/PPSJ	Up
23	PJ3	KWJ3	$\overline{\text{SS1}}$	—	V_{DDX}	PERJ/PPSJ	Up
24	BKGD	MODC	—	—	V_{DDX}	PUCR/BKPUE	Up
25	PB0	ECLK	—	—	V_{DDX}	PUCR/PUPBE	Disabled
26	PB1	API_EXTCLK	—	—	V_{DDX}	PUCR/PUPBE	Disabled
27	PB2	ECLKX2	—	—	V_{DDX}	PUCR/PUPBE	Disabled

Table 1-25. 100-Pin LQFP Pinout for S12GA96 and S12GA128

	Function <----lowest-----PRIORITY-----highest---->				Power Supply	Internal Pull Resistor	
Package Pin	Pin	2nd Func.	3rd Func.	4th Func.		CTRL	Reset State
1	PJ6	KWJ6	SCK2	—	V_{DDX}	PERJ/PPSJ	Up
2	PJ5	KWJ5	MOSI2	—	V_{DDX}	PERJ/PPSJ	Up
3	PJ4	KWJ4	MISO2	—	V_{DDX}	PERJ/PPSJ	Up
4	PA0	—	—	—	V_{DDX}	PUCR/PUPAE	Disabled
5	PA1	—	—	—	V_{DDX}	PUCR/PUPAE	Disabled
6	PA2	—	—	—	V_{DDX}	PUCR/PUPAE	Disabled
7	PA3	—	—	—	V_{DDX}	PUCR/PUPAE	Disabled
8	RESET	—	—	—	V_{DDX}	PULLUP	
9	VDDX1	—	—	—	—	—	—
10	VDDR	—	—	—	—	—	—
11	VSSX1	—	—	—	—	—	—
12	PE0[1]	EXTAL	—	—	V_{DDX}	PUCR/PDPEE	Down
13	VSS	—	—	—	—	—	—
14	PE1[1]	XTAL	—	—	V_{DDX}	PUCR/PDPEE	Down
15	TEST	—	—	—	N.A.	$\overline{\text{RESET}}$ pin	Down
16	PA4	—	—	—	V_{DDX}	PUCR/PUPAE	Disabled
17	PA5	—	—	—	V_{DDX}	PUCR/PUPAE	Disabled
18	PA6	—	—	—	V_{DDX}	PUCR/PUPAE	Disabled
19	PA7	—	—	—	V_{DDX}	PUCR/PUPAE	Disabled
20	PJ0	KWJ0	MISO1	—	V_{DDX}	PERJ/PPSJ	Up
21	PJ1	KWJ1	MOSI1	—	V_{DDX}	PERJ/PPSJ	Up
22	PJ2	KWJ2	SCK1	—	V_{DDX}	PERJ/PPSJ	Up
23	PJ3	KWJ3	$\overline{\text{SS1}}$	—	V_{DDX}	PERJ/PPSJ	Up
24	BKGD	MODC	—	—	V_{DDX}	PUCR/BKPUE	Up
25	PB0	ECLK	—	—	V_{DDX}	PUCR/PUPBE	Disabled
26	PB1	API_EXTCLK	—	—	V_{DDX}	PUCR/PUPBE	Disabled
27	PB2	ECLKX2	—	—	V_{DDX}	PUCR/PUPBE	Disabled

Table 1-31. 100-Pin LQFP Pinout for S12GA192 and S12GA240

	Function <----lowest-----PRIORITY-----highest---->				Power Supply	Internal Pull Resistor	
Package Pin	Pin	2nd Func.	3rd Func.	4th Func.		CTRL	Reset State
28	PB3	—	—	—	V_{DDX}	PUCR/PUPBE	Disabled
29	PP0	KWP0	ETRIG0	PWM0	V_{DDX}	PERP/PPSP	Disabled
30	PP1	KWP1	ETRIG1	PWM1	V_{DDX}	PERP/PPSP	Disabled
31	PP2	KWP2	ETRIG2	PWM2	V_{DDX}	PERP/PPSP	Disabled
32	PP3	KWP3	ETRIG3	PWM3	V_{DDX}	PERP/PPSP	Disabled
33	PP4	KWP4	PWM4	—	V_{DDX}	PERP/PPSP	Disabled
34	PP5	KWP5	PWM5	—	V_{DDX}	PERP/PPSP	Disabled
35	PP6	KWP6	PWM6	—	V_{DDX}	PERP/PPSP	Disabled
36	PP7	KWP7	PWM7	—	V_{DDX}	PERP/PPSP	Disabled
37	VDDX3	—	—	—	—	—	—
38	VSSX3	—	—	—	—	—	—
39	PT7	IOC7	—	—	V_{DDX}	PERT/PPST	Disabled
40	PT6	IOC6	—	—	V_{DDX}	PERT/PPST	Disabled
41	PT5	IOC5	—	—	V_{DDX}	PERT/PPST	Disabled
42	PT4	IOC4	—	—	V_{DDX}	PERT/PPST	Disabled
43	PT3	IOC3	—	—	V_{DDX}	PERT/PPST	Disabled
44	PT2	IOC2	—	—	V_{DDX}	PERT/PPST	Disabled
45	PT1	IOC1	—	—	V_{DDX}	PERT/PPST	Disabled
46	PT0	IOC0	—	—	V_{DDX}	PERT/PPST	Disabled
47	PB4	$\overline{\text{IRQ}}$	—	—	V_{DDX}	PUCR/PUPBE	Disabled
48	PB5	$\overline{\text{XIRQ}}$	—	—	V_{DDX}	PUCR/PUPBE	Disabled
49	PB6	—	—	—	V_{DDX}	PUCR/PUPBE	Disabled
50	PB7	—	—	—	V_{DDX}	PUCR/PUPBE	Disabled
51	PC0	—	—	—	V_{DDA}	PUCR/PUPCE	Disabled
52	PC1	—	—	—	V_{DDA}	PUCR/PUPCE	Disabled
53	PC2	—	—	—	V_{DDA}	PUCR/PUPCE	Disabled
54	PC3	—	—	—	V_{DDA}	PUCR/PUPCE	Disabled
55	PAD0	KWAD0	AN0	—	V_{DDA}	PER1AD/PPS1AD	Disabled
56	PAD8	KWAD8	AN8	—	V_{DDA}	PER0AD/PPS0AD	Disabled

5.3.2.4 Program Page Index Register (PPAGE)

Address: 0x0015

	7	6	5	4	3	2	1	0
R	0	0	0	0	PIX3	PIX2	PIX1	PIX0
W								
Reset	0	0	0	0	1	1	1	0

Figure 5-8. Program Page Index Register (PPAGE)

Read: Anytime

Write: Anytime

The four index bits of the PPAGE register select a 16K page in the global memory map (Figure 5-11). The selected 16K page is mapped into the paging window ranging from local address 0x8000 to 0xBFFF. Figure 5-9 illustrates the translation from local to global addresses for accesses to the paging window. The CPU has special access to read and write this register directly during execution of CALL and RTC instructions.

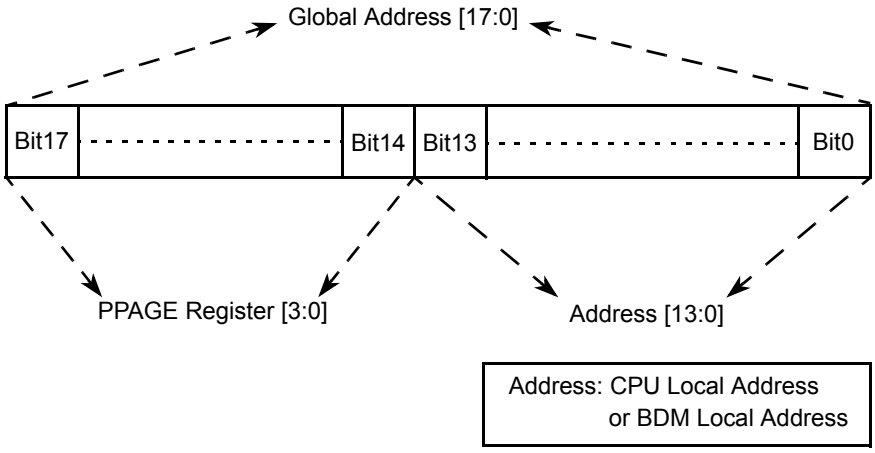


Figure 5-9. PPAGE Address Mapping

NOTE

Writes to this register using the special access of the CALL and RTC instructions will be complete before the end of the instruction execution.

Table 5-7. PPAGE Field Descriptions

Field	Description
3–0 PIX[3:0]	**Program Page Index Bits 3–0** — These page index bits are used to select which of the 256 flash array pages is to be accessed in the Program Page Window.

The fixed 16KB page from 0x0000 to 0x3FFF is the page number 0xC. Parts of this page are covered by Registers, EEPROM and RAM space. See SoC Guide for details.

The fixed 16KB page from 0x4000–0x7FFF is the page number 0xD.

Table 5-8. Global Address Ranges

	S12GN16	S12GN32	S12G48, S12GN48	S12G64	S12G96	S12G128	S12G192	S12G240
0x04000-0x07FFF (NVMRES=1)	Internal NVM Resources (for details refer to section FTMRG)							
0x04000-0x07FFF (NVMRES=0)	Unimplemented						Reserved	Flash
0x08000-0x0FFFF								
0x08000-0x1FFFF								
0x20000-0x27FFF					Reserved			
0x28000-0x2FFFF								
0x30000-0x33FFF			Reserved					
0x34000-0x37FFF								
0x38000-0x3BFFF	Reserved							
0x3C000-0x3FFFF	16k	32k	48k	64k	96k	128k	192k	240k

5.4.4 Prioritization of Memory Accesses

On S12G devices, the CPU and the BDM are not able to access the memory in parallel. An arbitration occurs whenever both modules attempt a memory access at the same time. CPU accesses are handled with higher priority than BDM accesses unless the BDM module has been stalled for more then 128 bus cycles. In this case the pending BDM access will be processed immediately.

5.4.5 Interrupts

The S12GMMC does not generate any interrupts.

Write: All modes through BDM operation when not secured

NOTE

When BDM is made active, the CPU stores the content of its CCR register in the BDMCCR register. However, out of special single-chip reset, the BDMCCR is set to 0xD8 and not 0xD0 which is the reset value of the CCR register in this CPU mode. Out of reset in all other modes the BDMCCR register is read zero.

When entering background debug mode, the BDM CCR holding register is used to save the condition code register of the user's program. It is also used for temporary storage in the standard BDM firmware mode. The BDM CCR holding register can be written to modify the CCR value.

7.3.2.2 BDM Program Page Index Register (BDMPPR)

Register Global Address 0x3_FF08

	7	6	5	4	3	2	1	0
R	BPAE	0	0	0	BPP3	BPP2	BPP1	BPP0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented, Reserved

Figure 7-5. BDM Program Page Register (BDMPPR)

Read: All modes through BDM operation when not secured

Write: All modes through BDM operation when not secured

Table 7-4. BDMPPR Field Descriptions

Field	Description
7 BPAE	**BDM Program Page Access Enable Bit** — BPAE enables program page access for BDM hardware and firmware read/write instructions The BDM hardware commands used to access the BDM registers (READ_BD and WRITE_BD) can not be used for program page accesses even if the BPAE bit is set. 0 BDM Program Paging disabled 1 BDM Program Paging enabled
3–0 BPP[3:0]	**BDM Program Page Index Bits 3–0** — These bits define the selected program page. For more detailed information regarding the program page window scheme, please refer to the S12S_MMC Block Guide.

7.3.3 Family ID Assignment

The family ID is an 8-bit value located in the BDM ROM in active BDM (at global address: 0x3_FF0F). The read-only value is a unique family ID which is 0xC2 for devices with an HCS12S core.

7.4 Functional Description

The BDM receives and executes commands from a host via a single wire serial interface. There are two types of BDM commands: hardware and firmware commands.

Table 8-16. State1 Sequencer Next State Selection

SC[3:0]	Description (Unspecified matches have no effect)
1010	Reserved
1011	Reserved
1100	Reserved
1101	Either Match0 or Match2 to Final State.....Match1 to State2
1110	Reserved
1111	Reserved

The priorities described in Table 8-36 dictate that in the case of simultaneous matches, a match leading to final state has priority followed by the match on the lower channel number (0,1,2). Thus with SC[3:0]=1101 a simultaneous match0/match1 transitions to final state.

8.3.2.7.2 Debug State Control Register 2 (DBGSCR2)

Address: 0x0027

	7	6	5	4	3	2	1	0
R	0	0	0	0	SC3	SC2	SC1	SC0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 8-10. Debug State Control Register 2 (DBGSCR2)

Read: If COMRV[1:0] = 01

Write: If COMRV[1:0] = 01 and DBG is not armed.

This register is visible at 0x0027 only with COMRV[1:0] = 01. The state control register 2 selects the targeted next state whilst in State2. The matches refer to the match channels of the comparator match control logic as depicted in Figure 8-1 and described in Section 8.3.2.8.1, “Debug Comparator Control Register (DBGXCTL). Comparators must be enabled by setting the comparator enable bit in the associated DBGXCTL control register.

Table 8-17. DBGSCR2 Field Descriptions

Field	Description
3–0 SC[3:0]	These bits select the targeted next state whilst in State2, based upon the match event.

Table 8-18. State2 —Sequencer Next State Selection

SC[3:0]	Description (Unspecified matches have no effect)
0000	Match0 to State1..... Match2 to State3.
0001	Match1 to State3
0010	Match2 to State3
0011	Match1 to State3..... Match0 Final State
0100	Match1 to State1..... Match2 to State3.

10.5 Resets

10.5.1 General

All reset sources are listed in Table 10-26. Refer to MCU specification for related vector addresses and priorities.

Table 10-26. Reset Summary

Reset Source	Local Enable
Power-On Reset (POR)	None
Low Voltage Reset (LVR)	None
External pin $\overline{\text{RESET}}$	None
Illegal Address Reset	None
Clock Monitor Reset	OSCE Bit in CPMUOSC register
COP Reset	CR[2:0] in CPMUCOP register

10.5.2 Description of Reset Operation

Upon detection of any reset of Table 10-26, an internal circuit drives the $\overline{\text{RESET}}$ pin low for 512 PLLCLK cycles. After 512 PLLCLK cycles the $\overline{\text{RESET}}$ pin is released. The reset generator of the S12CPMU waits for additional 256 PLLCLK cycles and then samples the $\overline{\text{RESET}}$ pin to determine the originating source. Table 10-27 shows which vector will be fetched.

Table 10-27. Reset Vector Selection

Sampled $\overline{\text{RESET}}$ Pin (256 cycles after release)	Oscillator monitor fail pending	COP time out pending	Vector Fetch
1	0	0	POR LVR Illegal Address Reset External pin $\overline{\text{RESET}}$
1	1	X	Clock Monitor Reset
1	0	1	COP Reset
0	X	X	POR LVR Illegal Address Reset External pin $\overline{\text{RESET}}$

NOTE

While System Reset is asserted the PLLCLK runs with the frequency f_{VCORST}.

13.1 Introduction

The ADC10B12C is a 12-channel, 10-bit, multiplexed input successive approximation analog-to-digital converter. Refer to device electrical specifications for ATD accuracy.

13.1.1 Features

- 8-, 10-bit resolution.
- Automatic return to low power after conversion sequence
- Automatic compare with interrupt for higher than or less/equal than programmable value
- Programmable sample time.
- Left/right justified result data.
- External trigger control.
- Sequence complete interrupt.
- Analog input multiplexer for 8 analog input channels.
- Special conversions for VRH, VRL, (VRL+VRH)/2.
- 1-to-12 conversion sequence lengths.
- Continuous conversion mode.
- Multiple channel scans.
- Configurable external trigger functionality on any AD channel or any of four additional trigger inputs. The four additional trigger inputs can be chip external or internal. Refer to device specification for availability and connectivity.
- Configurable location for channel wrap around (when converting multiple channels in a sequence).

edge or level sensitive with polarity control. Table 14-23 gives a brief description of the different combinations of control bits and their effect on the external trigger function.

In order to avoid maybe false trigger events please enable the external digital input via ATDDIEN register first and in the following enable the external trigger mode by bit ETRIGE.

Table 14-23. External Trigger Control Bits

ETRIGLE	ETRIGP	ETRIGE	SCAN	Description
X	X	0	0	Ignores external trigger. Performs one conversion sequence and stops.
X	X	0	1	Ignores external trigger. Performs continuous conversion sequences.
0	0	1	X	Trigger falling edge sensitive. Performs one conversion sequence per trigger.
0	1	1	X	Trigger rising edge sensitive. Performs one conversion sequence per trigger.
1	0	1	X	Trigger low level sensitive. Performs continuous conversions while trigger level is active.
1	1	1	X	Trigger high level sensitive. Performs continuous conversions while trigger level is active.

In either level or edge sensitive modes, the first conversion begins when the trigger is received.

Once ETRIGE is enabled a conversion must be triggered externally after writing to ATDCTL5 register.

During a conversion in edge sensitive mode, if additional trigger events are detected the overrun error flag ETORF is set.

If level sensitive mode is active and the external trigger de-asserts and later asserts again during a conversion sequence, this does not constitute an overrun. Therefore, the flag is not set. If the trigger is left active in level sensitive mode when a sequence is about to complete, another sequence will be triggered immediately.

14.4.2.2 General-Purpose Digital Port Operation

Each ATD input pin can be switched between analog or digital input functionality. An analog multiplexer makes each ATD input pin selected as analog input available to the A/D converter.

The pad of the ATD input pin is always connected to the analog input channel of the analog mulitplexer.

Each pad input signal is buffered to the digital port register.

This buffer can be turned on or off with the ATDDIEN register for each ATD input pin.
This is important so that the buffer does not draw excess current when an ATD input pin is selected as analog input to the ADC12B12C.

Table 15-9. Examples of ideal decimal ATD Results

Input Signal VRL = 0 Volts VRH = 5.12 Volts	8-Bit Codes (resolution=20mV)	10-Bit Codes (resolution=5mV)	Reserved
5.120 Volts	255	1023	Reserved
...	...	...	
0.022	1	4	
0.020	1	4	
0.018	1	4	
0.016	1	3	
0.014	1	3	
0.012	1	2	
0.010	1	2	
0.008	0	2	
0.006	0	1	
0.004	0	1	
0.003	0	1	
0.002	0	0	
0.000	0	0	

Table 15-10. Conversion Sequence Length Coding

S8C	S4C	S2C	S1C	Number of Conversions per Sequence
0	0	0	0	16
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15

Table 15-11. ATD Behavior in Freeze Mode (Breakpoint)

FRZ1	FRZ0	Behavior in Freeze Mode
0	0	Continue conversion

The configuration registers provide all required control bits for the DAC resistor network and for the operational amplifier.

The DAC resistor network generates the desired analog output voltage. The unbuffered voltage from the DAC resistor network output can be routed to the external DACU pin. When enabled, the buffered voltage from the operational amplifier output is available on the external AMP pin.

The operational amplifier is also stand alone usable.

Figure 17-1 shows the block diagram of the DAC_8B5V module.

17.2.1 Features

The DAC_8B5V module includes these distinctive features:

- 1 digital-analog converter channel with:
  - 8 bit resolution
  - full and reduced output voltage range
  - buffered or unbuffered analog output voltage usable
- operational amplifier stand alone usable

17.2.2 Modes of Operation

The DAC_8B5V module behaves as follows in the system power modes:

1. CPU run mode

   The functionality of the DAC_8B5V module is available.

2. CPU stop mode

   Independent from the mode settings, the operational amplifier is disabled, switch S1 and S2 are open.

   If the “Unbuffered DAC” mode was used before entering stop mode, then the DACU pin will reach VRH voltage level during stop mode.

   The content of the configuration registers is unchanged.

NOTE

After enabling and after return from CPU stop mode, the DAC_8B5V module needs a settling time to get fully operational, see Settling time specification of dac_8b5V_analog_ll18.

Table 20-4. SCICR1 Field Descriptions

Field	Description
7 LOOPS	**Loop Select Bit** — LOOPS enables loop operation. In loop operation, the RXD pin is disconnected from the SCI and the transmitter output is internally connected to the receiver input. Both the transmitter and the receiver must be enabled to use the loop function. 0 Normal operation enabled 1 Loop operation enabled The receiver input is determined by the RSRC bit.
6 SCISWAI	**SCI Stop in Wait Mode Bit** — SCISWAI disables the SCI in wait mode. 0 SCI enabled in wait mode 1 SCI disabled in wait mode
5 RSRC	**Receiver Source Bit** — When LOOPS = 1, the RSRC bit determines the source for the receiver shift register input. See Table 20-5. 0 Receiver input internally connected to transmitter output 1 Receiver input connected externally to transmitter
4 M	**Data Format Mode Bit** — MODE determines whether data characters are eight or nine bits long. 0 One start bit, eight data bits, one stop bit 1 One start bit, nine data bits, one stop bit
3 WAKE	**Wakeup Condition Bit** — WAKE determines which condition wakes up the SCI: a logic 1 (address mark) in the most significant bit position of a received data character or an idle condition on the RXD pin. 0 Idle line wakeup 1 Address mark wakeup
2 ILT	**Idle Line Type Bit** — ILT determines when the receiver starts counting logic 1s as idle character bits. The counting begins either after the start bit or after the stop bit. If the count begins after the start bit, then a string of logic 1s preceding the stop bit may cause false recognition of an idle character. Beginning the count after the stop bit avoids false idle character recognition, but requires properly synchronized transmissions. 0 Idle character bit count begins after start bit 1 Idle character bit count begins after stop bit
1 PE	**Parity Enable Bit** — PE enables the parity function. When enabled, the parity function inserts a parity bit in the most significant bit position. 0 Parity function disabled 1 Parity function enabled
0 PT	**Parity Type Bit** — PT determines whether the SCI generates and checks for even parity or odd parity. With even parity, an even number of 1s clears the parity bit and an odd number of 1s sets the parity bit. With odd parity, an odd number of 1s clears the parity bit and an even number of 1s sets the parity bit. 0 Even parity 1 Odd parity

Table 20-5. Loop Functions

LOOPS	RSRC	Function
0	x	Normal operation
1	0	Loop mode with transmitter output internally connected to receiver input
1	1	Single-wire mode with TXD pin connected to receiver input

Offset Module Base + 0x0012

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 24-23. Flash Reserved6 Register (FRSV6)

All bits in the FRSV6 register read 0 and are not writable.

24.3.2.19 Flash Reserved7 Register (FRSV7)

This Flash register is reserved for factory testing.

Offset Module Base + 0x0013

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 24-24. Flash Reserved7 Register (FRSV7)

All bits in the FRSV7 register read 0 and are not writable.

Table 28-19. P-Flash Protection Higher Address Range

FPHS[1:0]	Global Address Range	Protected Size
00	0x3_F800–0x3_FFFF	2 Kbytes
01	0x3_F000–0x3_FFFF	4 Kbytes
10	0x3_E000–0x3_FFFF	8 Kbytes
11	0x3_C000–0x3_FFFF	16 Kbytes

Table 28-20. P-Flash Protection Lower Address Range

FPLS[1:0]	Global Address Range	Protected Size
00	0x3_8000–0x3_83FF	1 Kbyte
01	0x3_8000–0x3_87FF	2 Kbytes
10	0x3_8000–0x3_8FFF	4 Kbytes
11	0x3_8000–0x3_9FFF	8 Kbytes

All possible P-Flash protection scenarios are shown in Figure 28-14 . Although the protection scheme is loaded from the Flash memory at global address 0x3_FF0C during the reset sequence, it can be changed by the user. The P-Flash protection scheme can be used by applications requiring reprogramming in single chip mode while providing as much protection as possible if reprogramming is not required.

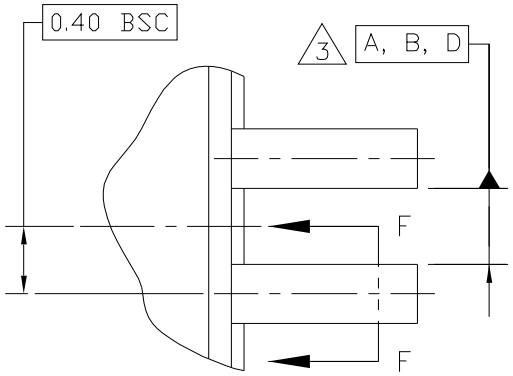
Table A-4. Operating Conditions

Rating	Symbol	Min	Typ	Max	Unit
Temperature Option V Operating ambient temperature range[1] Operating junction temperature range	 T_A T_J	 –40 –40	 27 —	 105 125	°C
Temperature Option M Operating ambient temperature range[1] Operating junction temperature range	 T_A T_J	 –40 –40	 27 —	 125 150	°C
Temperature Option W Operating ambient temperature range[1] Operating junction temperature range	 T_A T_J	 –40 –40	 27 —	 150 160	°C

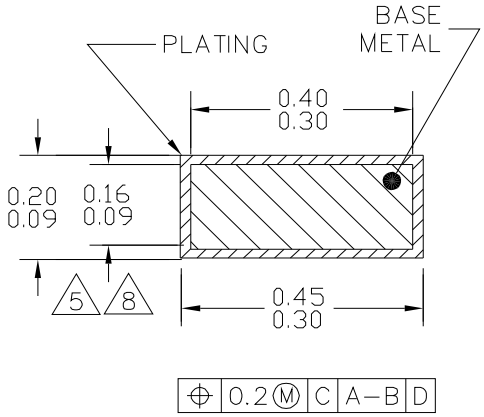
1 Please refer to Section A.1.8, “Power Dissipation and Thermal Characteristics” for more details about the relation between ambient temperature T_A and device junction temperature T_J.

NOTE

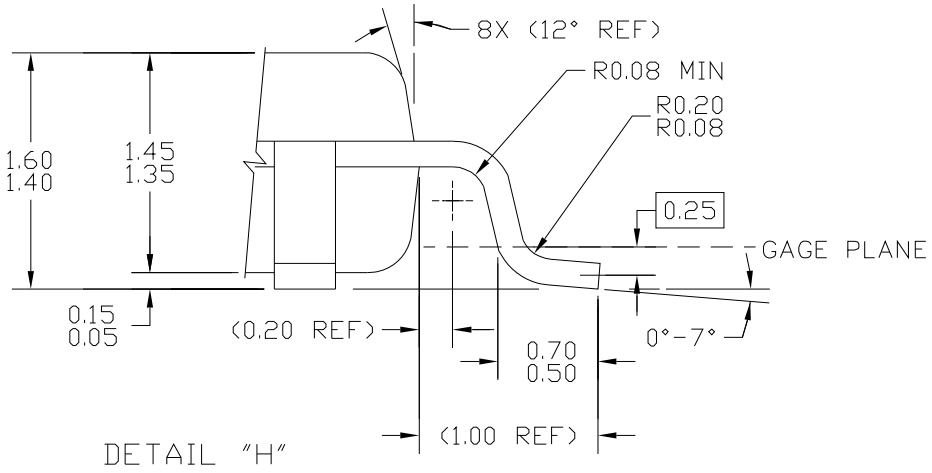
Operation is guaranteed when powering down until low voltage reset assertion.



DETAIL G



SECTION F–F
ROTATED 90°CW
32 PLACES



DETAIL "H"

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