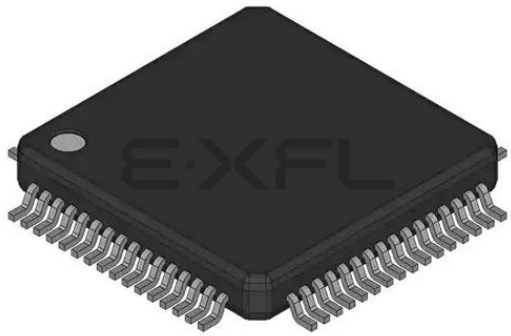

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Details	
Product Status	Active
Core Processor	12V1
Core Size	16-Bit
Speed	25MHz
Connectivity	IrDA, LINbus, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	54
Program Memory Size	48KB (48K x 8)
Program Memory Type	FLASH
EEPROM Size	1.5K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3.13V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=s9s12gn48f0clh

Appendix B
Detailed Register Address Map

Appendix C
Ordering and Shipping Information

Appendix D
Package and Die Information

1.3.8 System Integrity Support

- Power-on reset (POR)
- System reset generation
- Illegal address detection with reset
- Low-voltage detection with interrupt or reset
- Real time interrupt (RTI)
- Computer operating properly (COP) watchdog
  - — Configurable as window COP for enhanced failure detection
  - — Initialized out of reset using option bits located in flash memory
- Clock monitor supervising the correct function of the oscillator

1.3.9 Timer (TIM)

- Up to eight x 16-bit channels for input capture or output compare
- 16-bit free-running counter with 7-bit precision prescaler
- In case of eight channel timer Version an additional 16-bit pulse accumulator is available

1.3.10 Pulse Width Modulation Module (PWM)

- Up to eight channel x 8-bit or up to four channel x 16-bit pulse width modulator
  - — Programmable period and duty cycle per channel
  - — Center-aligned or left-aligned outputs
  - — Programmable clock select logic with a wide range of frequencies

1.3.11 Controller Area Network Module (MSCAN)

- 1 Mbit per second, CAN 2.0 A, B software compatible
  - — Standard and extended data frames
  - — 0–8 bytes data length
  - — Programmable bit rate up to 1 Mbps
- Five receive buffers with FIFO storage scheme
- Three transmit buffers with internal prioritization
- Flexible identifier acceptance filter programmable as:
  - — 2 x 32-bit
  - — 4 x 16-bit
  - — 8 x 8-bit
- Wakeup with integrated low pass filter option
- Loop back for self test
- Listen-only mode to monitor CAN bus

Table 1-21. 64-Pin LQFP Pinout for S12G96 and S12G128

	Function <----lowest-----PRIORITY-----highest---->					Power Supply	Internal Pull Resistor	
Package Pin	Pin	2nd Func.	3rd Func.	4th Func	5th Func		CTRL	Reset State
1	PJ6	KWJ6	SCK2	—	—	V_{DDX}	PERJ/PPSJ	Up
2	PJ5	KWJ5	MOSI2	—	—	V_{DDX}	PERJ/PPSJ	Up
3	PJ4	KWJ4	MISO2	—	—	V_{DDX}	PERJ/PPSJ	Up
4	RESET	—	—	—	—	V_{DDX}	PULLUP	
5	VDDX	—	—	—	—	—	—	—
6	VDDR	—	—	—	—	—	—	—
7	VSSX	—	—	—	—	—	—	—
8	PE0[1]	EXTAL	—	—	—	V_{DDX}	PUCR/PDPEE	Down
9	VSS	—	—	—	—	—	—	—
10	PE1[1]	XTAL	—	—	—	V_{DDX}	PUCR/PDPEE	Down
11	TEST	—	—	—	—	N.A.	$\overline{\text{RESET}}$ pin	Down
12	PJ0	KWJ0	MISO1	—	—	V_{DDX}	PERJ/PPSJ	Up
13	PJ1	KWJ1	MOSI1	—	—	V_{DDX}	PERJ/PPSJ	Up
14	PJ2	KWJ2	SCK1	—	—	V_{DDX}	PERJ/PPSJ	Up
15	PJ3	KWJ3	$\overline{\text{SS1}}$	—	—	V_{DDX}	PERJ/PPSJ	Up
16	BKGD	MODC	—	—	—	V_{DDX}	PUCR/BKPUE	Up
17	PP0	KWP0	ETRIG0	API_EXTCLK	PWM0	V_{DDX}	PERP/PPSP	Disabled
18	PP1	KWP1	ETRIG1	ECLKX2	PWM1	V_{DDX}	PERP/PPSP	Disabled
19	PP2	KWP2	ETRIG2	PWM2	—	V_{DDX}	PERP/PPSP	Disabled
20	PP3	KWP3	ETRIG3	PWM3	—	V_{DDX}	PERP/PPSP	Disabled
21	PP4	KWP4	PWM4	—	—	V_{DDX}	PERP/PPSP	Disabled
22	PP5	KWP5	PWM5	—	—	V_{DDX}	PERP/PPSP	Disabled
23	PP6	KWP6	PWM6	—	—	V_{DDX}	PERP/PPSP	Disabled
24	PP7	KWP7	PWM7	—	—	V_{DDX}	PERP/PPSP	Disabled
25	PT7	IOC7	—	—	—	V_{DDX}	PERT/PPST	Disabled
26	PT6	IOC6	—	—	—	V_{DDX}	PERT/PPST	Disabled
27	PT5	IOC5	—	—	—	V_{DDX}	PERT/PPST	Disabled

Table 1-22. 100-Pin LQFP Pinout for S12G96 and S12G128

	Function <----lowest-----PRIORITY-----highest---->				Power Supply	Internal Pull Resistor	
Package Pin	Pin	2nd Func.	3rd Func.	4th Func.		CTRL	Reset State
57	PAD1	KWAD1	AN1	—	V_{DDA}	PER1AD/PPS1AD	Disabled
58	PAD9	KWAD9	AN9	—	V_{DDA}	PER0AD/PPS0AD	Disabled
59	PAD2	KWAD2	AN2	—	V_{DDA}	PER1AD/PPS1AD	Disabled
60	PAD10	KWAD10	AN10	—	V_{DDA}	PER0AD/PPS0AD	Disabled
61	PAD3	KWAD3	AN3	—	V_{DDA}	PER1AD/PPS1AD	Disabled
62	PAD11	KWAD11	AN11	—	V_{DDA}	PER0AD/PPS0AD	Disabled
63	PAD4	KWAD4	AN4	—	V_{DDA}	PER1AD/PPS1AD	Disabled
64	PAD12	KWAD12	—	—	V_{DDA}	PER0AD/PPS0AD	Disabled
65	PAD5	KWAD5	AN5	—	V_{DDA}	PER1AD/PPS1AD	Disabled
66	PAD13	KWAD13	—	—	V_{DDA}	PER0AD/PPS0AD	Disabled
67	PAD6	KWAD6	AN6	—	V_{DDA}	PER1AD/PPS1AD	Disabled
68	PAD14	KWAD14	—	—	V_{DDA}	PER0AD/PPS0AD	Disabled
69	PAD7	KWAD7	AN7	—	V_{DDA}	PER1AD/PPS1AD	Disabled
70	PAD15	KWAD15	—	—	V_{DDA}	PER0AD/PPS0AD	Disabled
71	PC4	—	—	—	V_{DDA}	PUCR/PUPCE	Disabled
72	PC5		—	—	V_{DDA}	PUCR/PUPCE	Disabled
73	PC6		—	—	V_{DDA}	PUCR/PUPCE	Disabled
74	PC7		—	—	V_{DDA}	PUCR/PUPCE	Disabled
75	VRH	—	—	—	—	—	—
76	VDDA	—	—	—	—	—	—
77	VSSA	—	—	—	—	—	—
78	PD0	—	—	—	V_{DDX}	PUCR/PUPDE	Disabled
79	PD1	—	—	—	V_{DDX}	PUCR/PUPDE	Disabled
80	PD2	—	—	—	V_{DDX}	PUCR/PUPDE	Disabled
81	PD3	—	—	—	V_{DDX}	PUCR/PUPDE	Disabled
82	PS0	RXD0	—	—	V_{DDX}	PERS/PPSS	Up
83	PS1	TXD0	—	—	V_{DDX}	PERS/PPSS	Up
84	PS2	RXD1	—	—	V_{DDX}	PERS/PPSS	Up
85	PS3	TXD1	—	—	V_{DDX}	PERS/PPSS	Up

1.8.8.3 Pinout 100-Pin LQFP

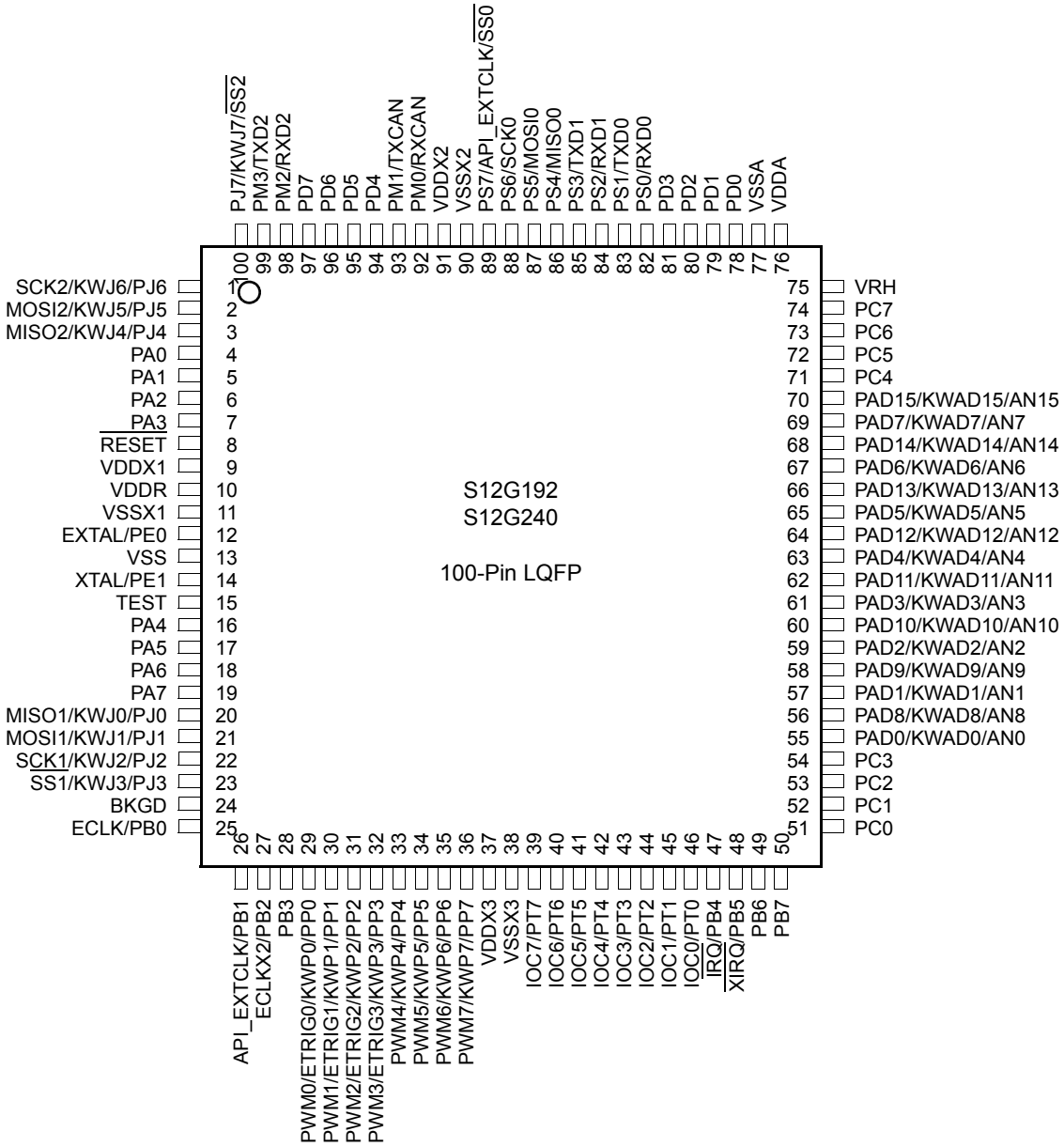

Figure 1-23. 100-Pin LQFP Pinout for S12G192 and S12G240

Table 2-4. Signals and Priorities

Legend	
?	Signal available on pin
?	Routing option on pin
?	Routing reset location
	Not available on pin

Port	Pin	Signal	Signals per Device and Package (signal priority on pin from top to bottom)																				I/O	Description
			GA240 / GA192	G240 / G192	G128 / GA128 / G96 / GA96	GA240 / GA192	G240 / G192	G128 / GA128 / G96 / GA96	G64 / GA64 / G48 / GA48	GN48	GA240 / GA192	G240 / G192	G128 / GA128 / G96 / GA96	G64 / GA64 / G48 / GA48	GN48	GN32 / GNA32	GN16 / GNA16	G64 / G48	GN48	GN32	GN16	GN32	GN16		
			100			64					48							32				20			
S	PS7	$\overline{SS0}$	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	I/O	SPI slave select
		TXD0																				?	?	I/O	SCI transmit
		PWM5																?	?	?	?			O	PWM channel
		PWM3																				?	?	O	PWM channel
		ECLK				?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	O	Free-running clock
		API_EXTCLK	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	O	API Clock
		ETRIG3																				?	?	I	ADC external trigger
		[PTS7]	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	I/O	GPIO
	PS6	SCK0	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	I/O	SPI serial clock
		IOC5																?	?	?	?			I/O	Timer channel
		IOC3																				?	?	I/O	Timer channel
		[PTS6]	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	I/O	GPIO
	PS5	MOSI0	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	I/O	SPI master out/slave in
		IOC4																?	?	?	?			I/O	Timer channel
		IOC2																				?	?	I/O	Timer channel
		[PTS5]	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	I/O	GPIO
	PS4	MISO0	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	I/O	SPI master in/slave out
		RXD0																				?	?	I	SCI receive pin
		PWM4																?	?	?	?			O	PWM channel
		PWM2																				?	?	O	PWM channel
		ETRIG2																				?	?	I	ADC external trigger
		[PTS4]	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	I/O	GPIO
	PS3	TXD1	?	?	?	?	?	?	?	?	?	?	?	?	?									I/O	SCI transmit
		[PTS3]	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?							I/O	GPIO
	PS2	RXD1	?	?	?	?	?	?	?	?	?	?	?	?	?									I	SCI receive
		[PTS2]	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?							I/O	GPIO
	PS1	TXD0	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?			I/O	SCI transmit
		[PTS1]	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?			I/O	GPIO
	PS0	RXD0	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?			I	SCI receive
		[PTS0]	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?			I/O	GPIO

2.5.2.6 Wired-Or Mode Register (WOMx)

If the pin is used as an output this register turns off the active-high drive. This allows wired-or type connections of outputs.

2.5.2.7 Interrupt Enable Register (PIEx)

If the pin is used as an interrupt input this register serves as a mask to the interrupt flag to enable/disable the interrupt.

2.5.2.8 Interrupt Flag Register (PIFx)

If the pin is used as an interrupt input this register holds the interrupt flag after a valid pin event.

2.5.2.9 Pin Routing Register (PRRx)

This register allows software re-configuration of the pinouts for specific peripherals in the 20 TSSOP package only.

2.5.2.10 Package Code Register (PKGCR)

This register determines the package in use. Pre programmed by factory.

2.5.3 Pin Configuration Summary

The following table summarizes the effect of the various configuration bits, that is data direction (DDR), output level (IO), pull enable (PE), pull select (PS) on the pin function and pull device [1].

The configuration bit PS is used for two purposes:

1. Configure the sensitive interrupt edge (rising or falling), if interrupt is enabled.
2. Select either a pullup or pulldown device if PE is active.

1.

8.3.2.8.7 Debug Comparator Data High Mask Register (DBGADHM)

Address: 0x002E

	7	6	5	4	3	2	1	0
R W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Reset	0	0	0	0	0	0	0	0

Figure 8-21. Debug Comparator Data High Mask Register (DBGADHM)

Read: If COMRV[1:0] = 00

Write: If COMRV[1:0] = 00 and DBG not armed.

Table 8-30. DBGADHM Field Descriptions

Field	Description
7–0 Bits[15:8]	**Comparator Data High Mask Bits** — The Comparator data high mask bits control whether the selected comparator compares the data bus bits [15:8] to the corresponding comparator data compare bits. Data bus comparisons are only performed if the TAG bit in DBGACTL is clear 0 Do not compare corresponding data bit Any value of corresponding data bit allows match. 1 Compare corresponding data bit

8.3.2.8.8 Debug Comparator Data Low Mask Register (DBGADLM)

Address: 0x002F

	7	6	5	4	3	2	1	0
R W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reset	0	0	0	0	0	0	0	0

Figure 8-22. Debug Comparator Data Low Mask Register (DBGADLM)

Read: If COMRV[1:0] = 00

Write: If COMRV[1:0] = 00 and DBG not armed.

Table 8-31. DBGADLM Field Descriptions

Field	Description
7–0 Bits[7:0]	**Comparator Data Low Mask Bits** — The Comparator data low mask bits control whether the selected comparator compares the data bus bits [7:0] to the corresponding comparator data compare bits. Data bus comparisons are only performed if the TAG bit in DBGACTL is clear 0 Do not compare corresponding data bit. Any value of corresponding data bit allows match 1 Compare corresponding data bit

8.4 Functional Description

This section provides a complete functional description of the DBG module. If the part is in secure mode, the DBG module can generate breakpoints but tracing is not possible.

10.1.3 S12CPMU Block Diagram

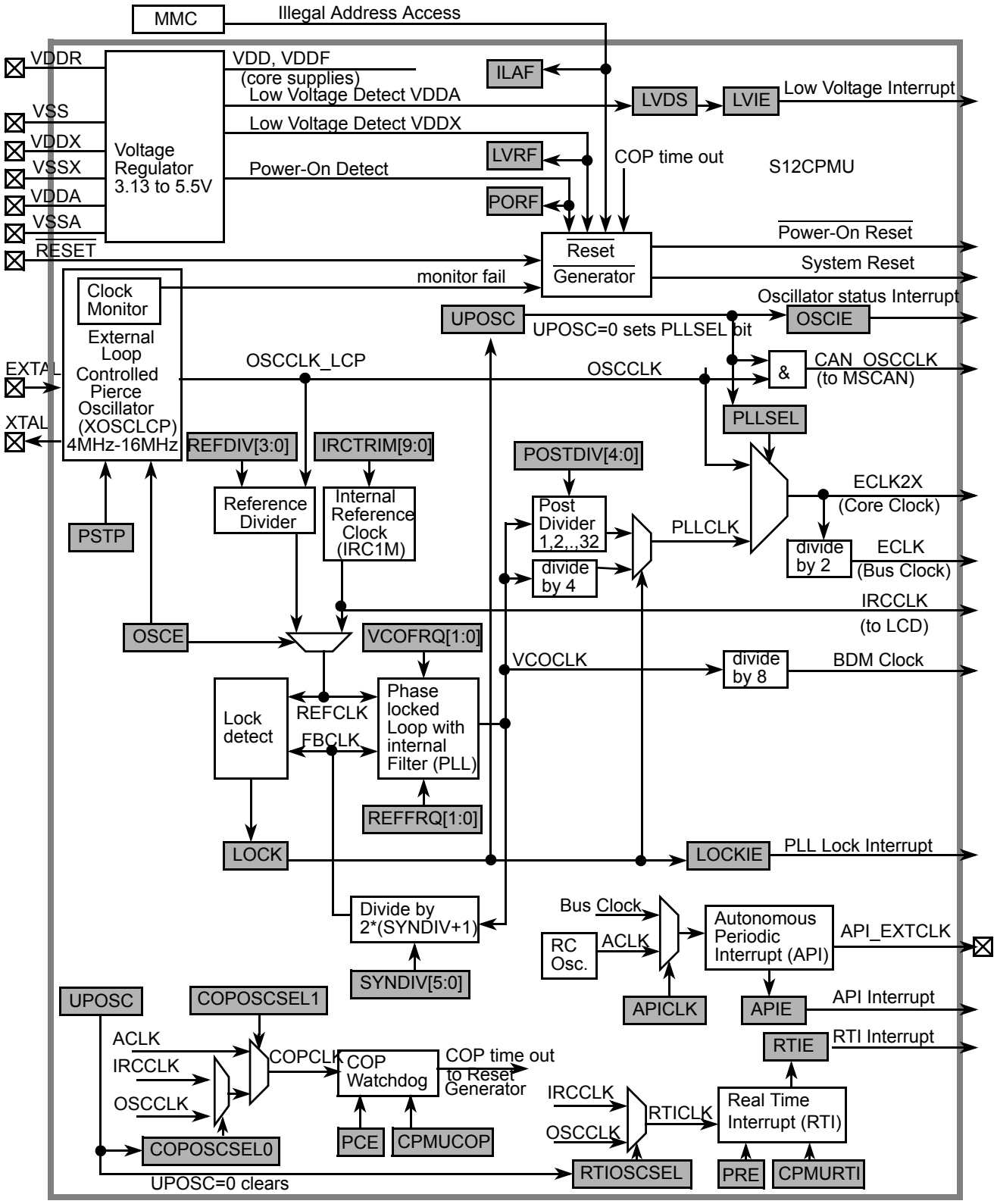

Figure 10-1. Block diagram of S12CPMU

Table 18-15. CANTARQ Register Field Descriptions

Field	Description
2-0 ABTRQ[2:0]	**Abort Request** — The CPU sets the ABTRQx bit to request that a scheduled message buffer (TXEx = 0) be aborted. The MSCAN grants the request if the message has not already started transmission, or if the transmission is not successful (lost arbitration or error). When a message is aborted, the associated TXE (see Section 18.3.2.7, “MSCAN Transmitter Flag Register (CANTFLG)”) and abort acknowledge flags (ABTAK, see Section 18.3.2.10, “MSCAN Transmitter Message Abort Acknowledge Register (CANTAAK)”) are set and a transmit interrupt occurs if enabled. The CPU cannot reset ABTRQx. ABTRQx is reset whenever the associated TXE flag is set. 0 No abort request 1 Abort request pending

18.3.2.10 MSCAN Transmitter Message Abort Acknowledge Register (CANTAAK)

The CANTAAK register indicates the successful abort of a queued message, if requested by the appropriate bits in the CANTARQ register.

Module Base + 0x0009 Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	ABTAK2	ABTAK1	ABTAK0
W								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 18-13. MSCAN Transmitter Message Abort Acknowledge Register (CANTAAK)

[1] Read: Anytime
Write: Unimplemented

NOTE

The CANTAAK register is held in the reset state when the initialization mode is active (INITRQ = 1 and INITAK = 1).

Table 18-16. CANTAAK Register Field Descriptions

Field	Description
2-0 ABTAK[2:0]	**Abort Acknowledge** — This flag acknowledges that a message was aborted due to a pending abort request from the CPU. After a particular message buffer is flagged empty, this flag can be used by the application software to identify whether the message was aborted successfully or was sent anyway. The ABTAKx flag is cleared whenever the corresponding TXE flag is cleared. 0 The message was not aborted. 1 The message was aborted.

18.3.2.11 MSCAN Transmit Buffer Selection Register (CANTBSEL)

The CANTBSEL register allows the selection of the actual transmit message buffer, which then will be accessible in the CANTXFG register space.

Table 24-21. EEPROM Protection Address Range

DPS[4:0]	Global Address Range	Protected Size
00000	0x0_0400 – 0x0_041F	32 bytes
00001	0x0_0400 – 0x0_043F	64 bytes
00010	0x0_0400 – 0x0_045F	96 bytes
00011	0x0_0400 – 0x0_047F	128 bytes
00100	0x0_0400 – 0x0_049F	160 bytes
00101	0x0_0400 – 0x0_04BF	192 bytes
The Protection Size goes on enlarging in step of 32 bytes, for each DPS value increasing of one. . . .		
01111 - to - 11111	0x0_0400 – 0x0_05FF	512 bytes

24.3.2.11 Flash Common Command Object Register (FCCOB)

The FCCOB is an array of six words addressed via the CCOBIX index found in the FCCOBIX register. Byte wide reads and writes are allowed to the FCCOB register.

Offset Module Base + 0x000A

	7	6	5	4	3	2	1	0
R W	CCOB[15:8]							
Reset	0	0	0	0	0	0	0	0

Figure 24-15. Flash Common Command Object High Register (FCCOBHI)

Offset Module Base + 0x000B

	7	6	5	4	3	2	1	0
R W	CCOB[7:0]							
Reset	0	0	0	0	0	0	0	0

Figure 24-16. Flash Common Command Object Low Register (FCCOBLO)

24.3.2.11.1 FCCOB - NVM Command Mode

NVM command mode uses the indexed FCCOB register to provide a command code and its relevant parameters to the Memory Controller. The user first sets up all required FCCOB fields and then initiates

The FPROT register, described in Section 25.3.2.9, can be set to protect regions in the Flash memory from accidental program or erase. Three separate memory regions, one growing upward from global address 0x3_8000 in the Flash memory (called the lower region), one growing downward from global address 0x3_FFFF in the Flash memory (called the higher region), and the remaining addresses in the Flash memory, can be activated for protection. The Flash memory addresses covered by these protectable regions are shown in the P-Flash memory map. The higher address region is mainly targeted to hold the boot loader code since it covers the vector space. Default protection settings as well as security information that allows the MCU to restrict access to the Flash module are stored in the Flash configuration field as described in Table 25-4.

Table 25-4. Flash Configuration Field

Global Address	Size (Bytes)	Description
0x3_FF00-0x3_FF07	8	Backdoor Comparison Key Refer to Section 25.4.6.11, “Verify Backdoor Access Key Command,” and Section 25.5.1, “Unsecuring the MCU using Backdoor Key Access”
0x3_FF08-0x3_FF0B[1]	4	Reserved
0x3_FF0C[1]	1	P-Flash Protection byte. Refer to Section 25.3.2.9, “P-Flash Protection Register (FPROT)”
0x3_FF0D[1]	1	EEPROM Protection byte. Refer to Section 25.3.2.10, “EEPROM Protection Register (EEPROT)”
0x3_FF0E[1]	1	Flash Nonvolatile byte Refer to Section 25.3.2.16, “Flash Option Register (FOPT)”
0x3_FF0F[1]	1	Flash Security byte Refer to Section 25.3.2.2, “Flash Security Register (FSEC)”

1 0x3FF08-0x3_FF0F form a Flash phrase and must be programmed in a single command write sequence. Each byte in the 0x3_FF08 - 0x3_FF0B reserved field should be programmed to 0xFF.

CAUTION

The FCLKDIV register should never be written while a Flash command is executing (CCIF=0).

Table 25-7. FCLKDIV Field Descriptions

Field	Description
7 FDIVLD	Clock Divider Loaded 0 FCLKDIV register has not been written since the last reset 1 FCLKDIV register has been written since the last reset
6 FDIVLCK	Clock Divider Locked 0 FDIV field is open for writing 1 FDIV value is locked and cannot be changed. Once the lock bit is set high, only reset can clear this bit and restore writability to the FDIV field in normal mode.
5–0 FDIV[5:0]	**Clock Divider Bits** — FDIV[5:0] must be set to effectively divide BUSCLK down to 1 MHz to control timed events during Flash program and erase algorithms. Table 25-8 shows recommended values for FDIV[5:0] based on the BUSCLK frequency. Please refer to Section 25.4.4, “Flash Command Operations,” for more information.

Table 25-8. FDIV values for various BUSCLK Frequencies

BUSCLK Frequency (MHz)		FDIV[5:0]	BUSCLK Frequency (MHz)		FDIV[5:0]
MIN[1]	MAX[2]		MIN[1]	MAX[2]	
1.0	1.6	0x00	16.6	17.6	0x10
1.6	2.6	0x01	17.6	18.6	0x11
2.6	3.6	0x02	18.6	19.6	0x12
3.6	4.6	0x03	19.6	20.6	0x13
4.6	5.6	0x04	20.6	21.6	0x14
5.6	6.6	0x05	21.6	22.6	0x15
6.6	7.6	0x06	22.6	23.6	0x16
7.6	8.6	0x07	23.6	24.6	0x17
8.6	9.6	0x08	24.6	25.6	0x18
9.6	10.6	0x09			
10.6	11.6	0x0A			
11.6	12.6	0x0B			
12.6	13.6	0x0C			
13.6	14.6	0x0D			
14.6	15.6	0x0E			
15.6	16.6	0x0F			

1 BUSCLK is Greater Than this value.

2 BUSCLK is Less Than or Equal to this value.

Table 26-15. FSTAT Field Descriptions

Field	Description
7 CCIF	**Command Complete Interrupt Flag** — The CCIF flag indicates that a Flash command has completed. The CCIF flag is cleared by writing a 1 to CCIF to launch a command and CCIF will stay low until command completion or command violation. 0 Flash command in progress 1 Flash command has completed
5 ACCERR	**Flash Access Error Flag** — The ACCERR bit indicates an illegal access has occurred to the Flash memory caused by either a violation of the command write sequence (see Section 26.4.4.2) or issuing an illegal Flash command. While ACCERR is set, the CCIF flag cannot be cleared to launch a command. The ACCERR bit is cleared by writing a 1 to ACCERR. Writing a 0 to the ACCERR bit has no effect on ACCERR. 0 No access error detected 1 Access error detected
4 FPVIOL	**Flash Protection Violation Flag** —The FPVIOL bit indicates an attempt was made to program or erase an address in a protected area of P-Flash or EEPROM memory during a command write sequence. The FPVIOL bit is cleared by writing a 1 to FPVIOL. Writing a 0 to the FPVIOL bit has no effect on FPVIOL. While FPVIOL is set, it is not possible to launch a command or start a command write sequence. 0 No protection violation detected 1 Protection violation detected
3 MGBUSY	**Memory Controller Busy Flag** — The MGBUSY flag reflects the active state of the Memory Controller. 0 Memory Controller is idle 1 Memory Controller is busy executing a Flash command (CCIF = 0)
2 RSVD	**Reserved Bit** — This bit is reserved and always reads 0.
1–0 MGSTAT[1:0]	**Memory Controller Command Completion Status Flag** — One or more MGSTAT flag bits are set if an error is detected during execution of a Flash command or during the Flash reset sequence. See Section 26.4.6, “Flash Command Description,” and Section 26.6, “Initialization” for details.

26.3.2.8 Flash Error Status Register (FERSTAT)

The FERSTAT register reflects the error status of internal Flash operations.

Offset Module Base + 0x0007

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	DFDIF	SFDIF
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 26-12. Flash Error Status Register (FERSTAT)

All flags in the FERSTAT register are readable and only writable to clear the flag.

CAUTION

The FCLKDIV register should never be written while a Flash command is executing (CCIF=0).

Table 27-7. FCLKDIV Field Descriptions

Field	Description
7 FDIVLD	Clock Divider Loaded 0 FCLKDIV register has not been written since the last reset 1 FCLKDIV register has been written since the last reset
6 FDIVLCK	Clock Divider Locked 0 FDIV field is open for writing 1 FDIV value is locked and cannot be changed. Once the lock bit is set high, only reset can clear this bit and restore writability to the FDIV field in normal mode.
5–0 FDIV[5:0]	**Clock Divider Bits** — FDIV[5:0] must be set to effectively divide BUSCLK down to 1 MHz to control timed events during Flash program and erase algorithms. Table 27-8 shows recommended values for FDIV[5:0] based on the BUSCLK frequency. Please refer to Section 27.4.4, “Flash Command Operations,” for more information.

Table 27-8. FDIV values for various BUSCLK Frequencies

BUSCLK Frequency (MHz)		FDIV[5:0]	BUSCLK Frequency (MHz)		FDIV[5:0]
MIN[1]	MAX[2]		MIN[1]	MAX[2]	
1.0	1.6	0x00	16.6	17.6	0x10
1.6	2.6	0x01	17.6	18.6	0x11
2.6	3.6	0x02	18.6	19.6	0x12
3.6	4.6	0x03	19.6	20.6	0x13
4.6	5.6	0x04	20.6	21.6	0x14
5.6	6.6	0x05	21.6	22.6	0x15
6.6	7.6	0x06	22.6	23.6	0x16
7.6	8.6	0x07	23.6	24.6	0x17
8.6	9.6	0x08	24.6	25.6	0x18
9.6	10.6	0x09			
10.6	11.6	0x0A			
11.6	12.6	0x0B			
12.6	13.6	0x0C			
13.6	14.6	0x0D			
14.6	15.6	0x0E			
15.6	16.6	0x0F			

1 BUSCLK is Greater Than this value.

2 BUSCLK is Less Than or Equal to this value.

27.3.2.11 Flash Common Command Object Register (FCCOB)

The FCCOB is an array of six words addressed via the CCOBIX index found in the FCCOBIX register. Byte wide reads and writes are allowed to the FCCOB register.

Offset Module Base + 0x000A

	7	6	5	4	3	2	1	0
R W	CCOB[15:8]							
Reset	0	0	0	0	0	0	0	0

Figure 27-16. Flash Common Command Object High Register (FCCOBHI)

Offset Module Base + 0x000B

	7	6	5	4	3	2	1	0
R W	CCOB[7:0]							
Reset	0	0	0	0	0	0	0	0

Figure 27-17. Flash Common Command Object Low Register (FCCOBLO)

27.3.2.11.1 FCCOB - NVM Command Mode

NVM command mode uses the indexed FCCOB register to provide a command code and its relevant parameters to the Memory Controller. The user first sets up all required FCCOB fields and then initiates the command's execution by writing a 1 to the CCIF bit in the FSTAT register (a 1 written by the user clears the CCIF command completion flag to 0). When the user clears the CCIF bit in the FSTAT register all FCCOB parameter fields are locked and cannot be changed by the user until the command completes (as evidenced by the Memory Controller returning CCIF to 1). Some commands return information to the FCCOB register array.

The generic format for the FCCOB parameter fields in NVM command mode is shown in Table 27-24. The return values are available for reading after the CCIF flag in the FSTAT register has been returned to 1 by the Memory Controller. Writes to the unimplemented parameter fields (CCOBIX = 110 and CCOBIX = 111) are ignored with reads from these fields returning 0x0000.

Table 27-24 shows the generic Flash command format. The high byte of the first word in the CCOB array contains the command code, followed by the parameters for this specific Flash command. For details on the FCCOB settings required by each command, see the Flash command descriptions in Section 27.4.6.

Table 27-24. FCCOB - NVM Command Mode (Typical Usage)

CCOBIX[2:0]	Byte	FCCOB Parameter Fields (NVM Command Mode)
000	HI	FCMD[7:0] defining Flash command
	LO	6'h0, Global address [17:16]
001	HI	Global address [15:8]
	LO	Global address [7:0]

Table 27-4). The Verify Backdoor Access Key command must not be executed from the Flash block containing the backdoor comparison key to avoid code runaway.

Table 27-52. Verify Backdoor Access Key Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x0C	Not required
001	Key 0	
010	Key 1	
011	Key 2	
100	Key 3	

Upon clearing CCIF to launch the Verify Backdoor Access Key command, the Memory Controller will check the FSEC KEYEN bits to verify that this command is enabled. If not enabled, the Memory Controller sets the ACCERR bit in the FSTAT register and terminates. If the command is enabled, the Memory Controller compares the key provided in FCCOB to the backdoor comparison key in the Flash configuration field with Key 0 compared to 0x3_FF00, etc. If the backdoor keys match, security will be released. If the backdoor keys do not match, security is not released and all future attempts to execute the Verify Backdoor Access Key command are aborted (set ACCERR) until a reset occurs. The CCIF flag is set after the Verify Backdoor Access Key operation has completed.

Table 27-53. Verify Backdoor Access Key Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 100 at command launch
		Set if an incorrect backdoor key is supplied
		Set if backdoor key access has not been enabled (KEYEN[1:0] != 10, see Section 27.3.2.2)
		Set if the backdoor key has mismatched since the last reset
	FPVIOL	None
	MGSTAT1	None
	MGSTAT0	None

27.4.6.12 Set User Margin Level Command

The Set User Margin Level command causes the Memory Controller to set the margin level for future read operations of the P-Flash or EEPROM block.

Table 27-54. Set User Margin Level Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x0D	Flash block selection code [1:0]. See Table 27-34
001	Margin level setting.	

28.4.8 Wait Mode

The Flash module is not affected if the MCU enters wait mode. The Flash module can recover the MCU from wait via the CCIF interrupt (see Section 28.4.7, “Interrupts”).

28.4.9 Stop Mode

If a Flash command is active (CCIF = 0) when the MCU requests stop mode, the current Flash operation will be completed before the MCU is allowed to enter stop mode.

28.5 Security

The Flash module provides security information to the MCU. The Flash security state is defined by the SEC bits of the FSEC register (see Table 28-11). During reset, the Flash module initializes the FSEC register using data read from the security byte of the Flash configuration field at global address 0x3_FF0F. The security state out of reset can be permanently changed by programming the security byte assuming that the MCU is starting from a mode where the necessary P-Flash erase and program commands are available and that the upper region of the P-Flash is unprotected. If the Flash security byte is successfully programmed, its new value will take affect after the next MCU reset.

The following subsections describe these security-related subjects:

- Unsecuring the MCU using Backdoor Key Access
- Unsecuring the MCU in Special Single Chip Mode using BDM
- Mode and Security Effects on Flash Command Availability

28.5.1 Unsecuring the MCU using Backdoor Key Access

The MCU may be unsecured by using the backdoor key access feature which requires knowledge of the contents of the backdoor keys (four 16-bit words programmed at addresses 0x3_FF00-0x3_FF07). If the KEYEN[1:0] bits are in the enabled state (see Section 28.3.2.2), the Verify Backdoor Access Key command (see Section 28.4.6.11) allows the user to present four prospective keys for comparison to the keys stored in the Flash memory via the Memory Controller. If the keys presented in the Verify Backdoor Access Key command match the backdoor keys stored in the Flash memory, the SEC bits in the FSEC register (see Table 28-11) will be changed to unsecure the MCU. Key values of 0x0000 and 0xFFFF are not permitted as backdoor keys. While the Verify Backdoor Access Key command is active, P-Flash memory and EEPROM memory will not be available for read access and will return invalid data.

30.3.2.11 Flash Common Command Object Register (FCCOB)

The FCCOB is an array of six words addressed via the CCOBIX index found in the FCCOBIX register. Byte wide reads and writes are allowed to the FCCOB register.

Offset Module Base + 0x000A

	7	6	5	4	3	2	1	0
R W	CCOB[15:8]							
Reset	0	0	0	0	0	0	0	0

Figure 30-16. Flash Common Command Object High Register (FCCOBHI)

Offset Module Base + 0x000B

	7	6	5	4	3	2	1	0
R W	CCOB[7:0]							
Reset	0	0	0	0	0	0	0	0

Figure 30-17. Flash Common Command Object Low Register (FCCOBLO)

30.3.2.11.1 FCCOB - NVM Command Mode

NVM command mode uses the indexed FCCOB register to provide a command code and its relevant parameters to the Memory Controller. The user first sets up all required FCCOB fields and then initiates the command's execution by writing a 1 to the CCIF bit in the FSTAT register (a 1 written by the user clears the CCIF command completion flag to 0). When the user clears the CCIF bit in the FSTAT register all FCCOB parameter fields are locked and cannot be changed by the user until the command completes (as evidenced by the Memory Controller returning CCIF to 1). Some commands return information to the FCCOB register array.

The generic format for the FCCOB parameter fields in NVM command mode is shown in Table 30-24. The return values are available for reading after the CCIF flag in the FSTAT register has been returned to 1 by the Memory Controller. Writes to the unimplemented parameter fields (CCOBIX = 110 and CCOBIX = 111) are ignored with reads from these fields returning 0x0000.

Table 30-24 shows the generic Flash command format. The high byte of the first word in the CCOB array contains the command code, followed by the parameters for this specific Flash command. For details on the FCCOB settings required by each command, see the Flash command descriptions in Section 30.4.6.

Table 30-24. FCCOB - NVM Command Mode (Typical Usage)

CCOBIX[2:0]	Byte	FCCOB Parameter Fields (NVM Command Mode)
000	HI	FCMD[7:0] defining Flash command
	LO	6'h0, Global address [17:16]
001	HI	Global address [15:8]
	LO	Global address [7:0]

Table A-7. 3.3-V I/O Characteristics (Junction Temperature From +150°C To +160°C)

Conditions are 3.15 V < V_{DD35} < 3.6 V junction temperature from +150°C to +160°C, unless otherwise noted I/O Characteristics for all I/O pins except EXTAL, XTAL,TEST and supply pins.							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	M	Input high voltage	V_{IH}	0.65*V_{DD35}	—	—	V
2	T	Input high voltage	V_{IH}	—	—	V_{DD35}+0.3	V
3	M	Input low voltage	V_{IL}	—	—	0.35*V_{DD35}	V
4	T	Input low voltage	V_{IL}	V_{SS35} – 0.3	—	—	V
5	C	Input hysteresis	V_{HYS}	0.06*V_{DD35}	—	0.3*V_{DD35}	mV
6	M	Input leakage current (pins in high impedance input mode)[1] V_{in} = V_{DD35} or V_{SS35}	I_{in}	-1	—	1	µA
7	P	Output high voltage (pins in output mode) I_{OH} = –1.75 mA	V_{OH}	V_{DD35}-0.4	—	—	V
8	C	Output low voltage (pins in output mode) I_{OL} = +1.75 mA	V_{OL}	—	—	0.4	V
9	M	Internal pull up device current V_{IH} min > input voltage > V_{IL} max	I_{PUL}	-1	—	–70	µA
10	M	Internal pull down device current V_{IH} min > input voltage > V_{IL} max	I_{PDH}	1	—	70	µA
11	D	Input capacitance	C_{in}	—	7	—	pF
12	T	Injection current[2] Single pin limit Total device limit, sum of all injected currents	 I_{ICS} I_{ICP}	 –2.5 –25	—	 2.5 25	mA

1 Maximum leakage current occurs at maximum operating temperature. Current decreases by approximately one-half for each 8°°C to 12°C° in the temperature range from 50°C to 125°C.

2 Refer to Section A.1.4, “Current Injection” for more details