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Details

Product Status	Active
Core Processor	12V1
Core Size	16-Bit
Speed	25MHz
Connectivity	IrDA, LINbus, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	40
Program Memory Size	48KB (48K x 8)
Program Memory Type	FLASH
EEPROM Size	1.5K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3.13V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s9s12gn48f0vlf

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	Function <lowestpriorityhighest></lowestpriorityhighest>					Power	Internal P Resisto	rull r
Package Pin	Pin	2nd Func.	3rd Func.	4th Func	5th Func	Supply	CTRL	Reset State
30	PAD10	KWAD10	AN10			V _{DDA}	PER0AD/PPS0AD	Disabled
31	PAD3	KWAD3	AN3	—	—	V _{DDA}	PER1AD/PPS1AD	Disabled
32	PAD11	KWAD11	AN11	—	—	V _{DDA}	PER0AD/PPS0AD	Disabled
33	PAD4	KWAD4	AN4	—	—	V _{DDA}	PER1AD/PPS1AD	Disabled
34	PAD5	KWAD5	AN5	—	—	V _{DDA}	PER1AD/PPS0AD	Disabled
35	PAD6	KWAD6	AN6	—	—	V _{DDA}	PER1AD/PPS1AD	Disabled
36	PAD7	KWAD7	AN7	—	—	V _{DDA}	PER1AD/PPS1AD	Disabled
37	VDDA	VRH	—	—	—	_	_	_
38	VSSA	—	—	—	—	_	_	_
39	PS0	RXD0	—	—	—	V _{DDX}	PERS/PPSS	Up
40	PS1	TXD0	—	—	—	V _{DDX}	PERS/PPSS	Up
41	PS2	RXD1	—	—	—	V _{DDX}	PERS/PPSS	Up
42	PS3	TXD1	—	—	—	V _{DDX}	PERS/PPSS	Up
43	PS4	MISO0	—	—	—	V _{DDX}	PERS/PPSS	Up
44	PS5	MOSI0	—	—	—	V _{DDX}	PERS/PPSS	Up
45	PS6	SCK0	—	—	—	V _{DDX}	PERS/PPSS	Up
46	PS7	API_EXTC LK	ECLK	SS0	_	V _{DDX}	PERS/PPSS	Up
47	PM0	RXD2	RXCAN	—	—	V _{DDX}	PERM/PPSM	Disabled
48	PM1	TXD2	TXCAN	_	_	V _{DDX}	PERM/PPSM	Disabled

Table 1-23.	48-Pin LQFP	Pinout for	S12GA96	and S12GA128
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¹ The regular I/O characteristics (see Section A.2, "I/O Characteristics") apply if the EXTAL/XTAL function is disabled

1.8.9.3 Pinout 100-Pin LQFP



Figure 1-26. 100-Pin LQFP Pinout for S12GA192 and S12GA240

Chapter 5 S12G Memory Map Controller (S12GMMCV1)

Table	5-1.	Revision	History	Table
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Rev. No.	Date	Sections	Substantial Change(s)
(Item No.)	(Submitted By)	Affected	
01.02	20-May 2010		Updates for S12VR48 and S12VR64

5.1 Introduction

The S12GMMC module controls the access to all internal memories and peripherals for the CPU12 and S12SBDM module. It regulates access priorities and determines the address mapping of the on-chip resources. Figure 5-1 shows a block diagram of the S12GMMC module.

5.1.1 Glossary

Term	Definition
Local Addresses	Address within the CPU12's Local Address Map (Figure 5-11)
Global Address	Address within the Global Address Map (Figure 5-11)
Aligned Bus Access	Bus access to an even address.
Misaligned Bus Access	Bus access to an odd address.
NS	Normal Single-Chip Mode
SS	Special Single-Chip Mode
Unimplemented Address Ranges	Address ranges which are not mapped to any on-chip resource.
NVM	Non-volatile Memory; Flash or EEPROM
IFR	NVM Information Row. Refer to FTMRG Block Guide

Table 5-2. Glossary Of Terms

5.1.2 Overview

The S12GMMC connects the CPU12's and the S12SBDM's bus interfaces to the MCU's on-chip resources (memories and peripherals). It arbitrates the bus accesses and determines all of the MCU's memory maps. Furthermore, the S12GMMC is responsible for constraining memory accesses on secured devices and for selecting the MCU's functional mode.

Chapter 10 S12 Clock, Reset and Power Management Unit (S12CPMU) Revision History

Version Number	Revision Date	Effective Date	Author	Description of Changes
V04.03	29 Jan 10	29 Jan 10		Added Note in section 10.3.2.16/10-380 to precise description of API behavior after feature enable for the first time-out period.
V04.04	03 Mar 10	03 Mar 10		Corrected typos.
V04.05	23. Mar 10	23 Mar 10		Corrected typos.
V04.06	13 Apr 10	13 Apr 10		Corrected typo in Table 10-6
V04.07	28 Apr 10	28 Apr 10		Major rework fixing typos, figures and tables and improved description of Adaptive Oscillator Filter.
V04.08	03 May 10	03 Mail 10		Improved pin description in Section 10.2, "Signal Description
V04.09	22 Jun 10	22 Jun 10		Changed IP-Name from OSCLCP to XOSCLCP, added OSCCLK_LCP clock name intoFigure 10-1 and Figure 10-2 updated description of Section 10.2.2, "EXTAL and XTAL.
V04.10	01 Jul 10	01 Jul 10		Added TC trimming to feature list
V04.11	23 Aug 10	23 Aug 10		Removed feature of adaptive oscillator filter. Register bits 6 and 4to 0in the CPMUOSC register are marked reserved and do not alter.
V04.12	27 April 12	27 April 12		Corrected wording for API interrupt flag Changed notation of IRC trim values for 0x00000 to 0b00000
V04.13	6 Mar 13	6 Mar 13		Table 10-19. correction: substituted f _{ACLK} by ACLK Clock Period

10.1 Introduction

This specification describes the function of the Clock, Reset and Power Management Unit (S12CPMU).

- The Pierce oscillator (XOSCLCP) provides a robust, low-noise and low-power external clock source. It is designed for optimal start-up margin with typical quartz crystals and ceramic resonators.
- The Voltage regulator (IVREG) operates from the range 3.13V to 5.5V. It provides all the required chip internal voltages and voltage monitors.
- The Phase Locked Loop (PLL) provides a highly accurate frequency multiplier with internal filter.

Table 10-3. CPMUFLG Field Descriptions (continued)

Field	Description
1 OSCIF	 Oscillator Interrupt Flag — OSCIF is set to 1 when UPOSC status bit changes. This flag can only be cleared by writing a 1. Writing a 0 has no effect. If enabled (OSCIE=1), OSCIF causes an interrupt request. 0 No change in UPOSC bit. 1 UPOSC bit has changed.
0 UPOSC	 Oscillator Status Bit — UPOSC reflects the status of the oscillator. Writes have no effect. While UPOSC=0 the OSCCLK going to the MSCAN module is off. Entering Full Stop Mode UPOSC is cleared. 0 The oscillator is off or oscillation is not qualified by the PLL. 1 The oscillator is qualified by the PLL.

10.3.2.5 S12CPMU Interrupt Enable Register (CPMUINT)

This register enables S12CPMU interrupt requests.

0x0038





Read: Anytime

Write: Anytime

Field	Description
7 RTIE	Real Time Interrupt Enable Bit 0 Interrupt requests from RTI are disabled. 1 Interrupt will be requested whenever RTIF is set.
4 LOCKIE	PLL Lock Interrupt Enable Bit 0 PLL LOCK interrupt requests are disabled. 1 Interrupt will be requested whenever LOCKIF is set.
1 OSCIE	Oscillator Corrupt Interrupt Enable Bit 0 Oscillator Corrupt interrupt requests are disabled. 1 Interrupt will be requested whenever OSCIF is set.

10.3.2.6 S12CPMU Clock Select Register (CPMUCLKS)

This register controls S12CPMU clock selection.

Analog-to-Digital Converter (ADC10B12CV2)

FRZ1	FRZ0	Behavior in Freeze Mode
0	1	Reserved
1	0	Finish current conversion, then freeze
1	1	Freeze Immediately

Table 13-11. ATD Behavior in Freeze Mode (Breakpoint)

13.3.2.5 ATD Control Register 4 (ATDCTL4)

Writes to this register will abort current conversion sequence.

Module Base + 0x0004



Read: Anytime

Write: Anytime

Table 13-12. ATDCTL4 Field Descriptions

Field	Description
7–5 SMP[2:0]	Sample Time Select — These three bits select the length of the sample time in units of ATD conversion clock cycles. Note that the ATD conversion clock period is itself a function of the prescaler value (bits PRS4-0). Table 13-13 lists the available sample time lengths.
4–0 PRS[4:0]	ATD Clock Prescaler — These 5 bits are the binary prescaler value PRS. The ATD conversion clock frequency is calculated as follows:
	$f_{ATDCLK} = \frac{f_{BUS}}{2 \times (PRS + 1)}$
	Refer to Device Specification for allowed frequency range of f _{ATDCLK} .

Table 13-13. Sample Time Select

SMP2	SMP1	SMP0	Sample Time in Number of ATD Clock Cycles
0	0	0	4
0	0	1	6
0	1	0	8
0	1	1	10
1	0	0	12
1	0	1	16
1	1	0	20
1	1	1	24

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Field	Description
3–0 CC[3:0]	Conversion Counter — These 4 read-only bits are the binary value of the conversion counter. The conversion counter points to the result register that will receive the result of the current conversion. E.g. CC3=0, CC2=1, CC1=1, CC0=0 indicates that the result of the current conversion will be in ATD Result Register 6. If in non-FIFO mode (FIFO=0) the conversion counter is initialized to zero at the beginning and end of the conversion sequence. If in FIFO mode (FIFO=1) the register counter is not initialized. The conversion counter wraps around when its maximum value is reached. Aborting a conversion or starting a new conversion clears the conversion counter even if FIFO=1.

13.3.2.8 ATD Compare Enable Register (ATDCMPE)

Writes to this register will abort current conversion sequence.

Read: Anytime

Write: Anytime

Module Base + 0x0008





Table 13-17. ATDCMPE Field Descriptions

Field	Description
11–0 CMPE[11:0]	Compare Enable for Conversion Number <i>n</i> (<i>n</i> = 11, 10, 9, 8, 7, 6, 5, 4, 3, 2, 1, 0) of a Sequence (<i>n</i> conversion <i>number</i> , <i>NOT channel number</i> !) — These bits enable automatic compare of conversion results individually for conversions of a sequence. The sense of each comparison is determined by the CMPHT[<i>n</i>] bit in the ATDCMPHT register.
	For each conversion number with CMPE[<i>n</i>]=1 do the following: 1) Write compare value to ATDDR <i>n</i> result register 2) Write compare operator with CMPHT[<i>n</i>] in ATDCPMHT register
	 CCF[<i>n</i>] in ATDSTAT2 register will flag individual success of any comparison. 0 No automatic compare 1 Automatic compare of results for conversion <i>n</i> of a sequence is enabled.

14.4 Functional Description

The ADC12B12C consists of an analog sub-block and a digital sub-block.

14.4.1 Analog Sub-Block

The analog sub-block contains all analog electronics required to perform a single conversion. Separate power supplies VDDA and VSSA allow to isolate noise of other MCU circuitry from the analog sub-block.

14.4.1.1 Sample and Hold Machine

The Sample and Hold Machine controls the storage and charge of the sample capacitor to the voltage level of the analog signal at the selected ADC input channel.

During the sample process the analog input connects directly to the storage node.

The input analog signals are unipolar and must be within the potential range of VSSA to VDDA.

During the hold process the analog input is disconnected from the storage node.

14.4.1.2 Analog Input Multiplexer

The analog input multiplexer connects one of the 12 external analog input channels to the sample and hold machine.

14.4.1.3 Analog-to-Digital (A/D) Machine

The A/D Machine performs analog to digital conversions. The resolution is program selectable to be either 8 or 10 or 12 bits. The A/D machine uses a successive approximation architecture. It functions by comparing the sampled and stored analog voltage with a series of binary coded discrete voltages. By following a binary search algorithm, the A/D machine identifies the discrete voltage that is nearest to the sampled and stored voltage.

When not converting the A/D machine is automatically powered down.

Only analog input signals within the potential range of VRL to VRH (A/D reference potentials) will result in a non-railed digital output code.

14.4.2 Digital Sub-Block

This subsection describes some of the digital features in more detail. See Section 14.3.2, "Register Descriptions" for all details.

14.4.2.1 External Trigger Input

The external trigger feature allows the user to synchronize ATD conversions to an external event rather than relying only on software to trigger the ATD module when a conversions is about to take place. The external trigger signal (out of reset ATD channel 11, configurable in ATDCTL1) is programmable to be

Pulse-Width Modulator (S12PWM8B8CV2)

Clock A is used as an input to an 8-bit down counter. This down counter loads a user programmable scale value from the scale register (PWMSCLA). When the down counter reaches one, a pulse is output and the 8-bit counter is re-loaded. The output signal from this circuit is further divided by two. This gives a greater range with only a slight reduction in granularity. Clock SA equals clock A divided by two times the value in the PWMSCLA register.

NOTE

Clock SA = Clock A / (2 * PWMSCLA)

When PWMSCLA = 00, PWMSCLA value is considered a full scale value of 256. Clock A is thus divided by 512.

Similarly, clock B is used as an input to an 8-bit down counter followed by a divide by two producing clock SB. Thus, clock SB equals clock B divided by two times the value in the PWMSCLB register.

NOTE

Clock SB = Clock B / (2 * PWMSCLB)

When PWMSCLB = 00, PWMSCLB value is considered a full scale value of 256. Clock B is thus divided by 512.

As an example, consider the case in which the user writes \$FF into the PWMSCLA register. Clock A for this case will be E (bus clock) divided by 4. A pulse will occur at a rate of once every 255x4 E cycles. Passing this through the divide by two circuit produces a clock signal at an E divided by 2040 rate. Similarly, a value of \$01 in the PWMSCLA register when clock A is E divided by 4 will produce a clock at an E divided by 8 rate.

Writing to PWMSCLA or PWMSCLB causes the associated 8-bit down counter to be re-loaded. Otherwise, when changing rates the counter would have to count down to \$01 before counting at the proper rate. Forcing the associated counter to re-load the scale register value every time PWMSCLA or PWMSCLB is written prevents this.

NOTE

Writing to the scale registers while channels are operating can cause irregularities in the PWM outputs.

19.4.1.3 Clock Select

Each PWM channel has the capability of selecting one of four clocks, clock A, clock SA, clock B or clock SB. The clock selection is done with the PCLKx control bits in the PWMCLK register and PCLKABx control bits in PWMCLKAB register. For backward compatibility consideration, the reset value of PWMCLK and PWMCLKAB configures following default clock selection.

For channels 0, 1, 4, and 5 the clock choices are clock A.

For channels 2, 3, 6, and 7 the clock choices are clock B.

NOTE

Changing clock control bits while channels are operating can cause irregularities in the PWM outputs.

Field	Description
1 FE	 Framing Error Flag — FE is set when a logic 0 is accepted as the stop bit. FE bit is set during the same cycle as the RDRF flag but does not get set in the case of an overrun. FE inhibits further data reception until it is cleared. Clear FE by reading SCI status register 1 (SCISR1) with FE set and then reading the SCI data register low (SCIDRL). 0 No framing error 1 Framing error
0 PF	 Parity Error Flag — PF is set when the parity enable bit (PE) is set and the parity of the received data does not match the parity type bit (PT). PF bit is set during the same cycle as the RDRF flag but does not get set in the case of an overrun. Clear PF by reading SCI status register 1 (SCISR1), and then reading SCI data register low (SCIDRL). 0 No parity error 1 Parity error

20.3.2.8 SCI Status Register 2 (SCISR2)

Module Base + 0x0005



Figure 20-11. SCI Status Register 2 (SCISR2)

Read: Anytime

Write: Anytime

Table 20-12. SCISR2 Field Descriptions

Field	Description
7 AMAP	Alternative Map — This bit controls which registers sharing the same address space are accessible. In the reset condition the SCI behaves as previous versions. Setting AMAP=1 allows the access to another set of control and status registers and hides the baud rate and SCI control Register 1. 0 The registers labelled SCIBDH (0x0000),SCIBDL (0x0001), SCICR1 (0x0002) are accessible 1 The registers labelled SCIASR1 (0x0000),SCIACR1 (0x0001), SCIACR2 (0x00002) are accessible
4 TXPOL	 Transmit Polarity — This bit control the polarity of the transmitted data. In NRZ format, a one is represented by a mark and a zero is represented by a space for normal polarity, and the opposite for inverted polarity. In IrDA format, a zero is represented by short high pulse in the middle of a bit time remaining idle low for a one for normal polarity, and a zero is represented by short low pulse in the middle of a bit time remaining idle high for a one for inverted polarity. 0 Normal polarity 1 Inverted polarity



Figure 22-2. Interrupt Flag Setting

22.2 External Signal Description

The TIM16B6CV3 module has a selected number of external pins. Refer to device specification for exact number.

22.2.1 IOC5 - IOC0 — Input Capture and Output Compare Channel 5-0

Those pins serve as input capture or output compare for TIM16B6CV3 channel.

NOTE

For the description of interrupts see Section 22.6, "Interrupts".

22.3 Memory Map and Register Definition

This section provides a detailed description of all memory and registers.

22.3.1 Module Memory Map

The memory map for the TIM16B6CV3 module is given below in Figure 22-3. The address listed for each register is the address offset. The total address for each register is the sum of the base address for the TIM16B6CV3 module and the address offset for each register.

22.3.2 Register Descriptions

This section consists of register descriptions in address order. Each description includes a standard register diagram with an associated figure number. Details of register bit and field function follow the register diagrams, in bit order.



Figure 24-3. Memory Controller Resource Memory Map (NVMRES=1)

24.3.2 Register Descriptions

The Flash module contains a set of 20 control and status registers located between Flash module base + 0x0000 and 0x0013.

In the case of the writable registers, the write accesses are forbidden during Fash command execution (for more detail, see Caution note in Section 24.3).

A summary of the Flash module registers is given in Figure 24-4 with detailed descriptions in the following subsections.



Figure 24-4. FTMRG16K1 Register Summary

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16 KByte Flash Module (S12FTMRG16K1V1)

The security function in the Flash module is described in Section 24.5.

24.3.2.3 Flash CCOB Index Register (FCCOBIX)

The FCCOBIX register is used to index the FCCOB register for Flash memory operations.



Figure 24-7. FCCOB Index Register (FCCOBIX)

CCOBIX bits are readable and writable while remaining bits read 0 and are not writable.

Table 24-12. FCCOBIX Field Descriptions

Field	Description
2–0 CCOBIX[1:0]	Common Command Register Index — The CCOBIX bits are used to select which word of the FCCOB register array is being read or written to. See 24.3.2.11 Flash Common Command Object Register (FCCOB)," for more details.

24.3.2.4 Flash Reserved0 Register (FRSV0)

This Flash register is reserved for factory testing.

Offset Module Base + 0x000C



Figure 24-8. Flash Reserved0 Register (FRSV0)

All bits in the FRSV0 register read 0 and are not writable.

24.3.2.5 Flash Configuration Register (FCNFG)

The FCNFG register enables the Flash command complete interrupt and forces ECC faults on Flash array read access from the CPU.

- Fast sector erase and phrase program operation
- Ability to read the P-Flash memory while programming a word in the EEPROM memory
- Flexible protection scheme to prevent accidental program or erase of P-Flash memory

26.1.2.2 EEPROM Features

- 1.5Kbytes of EEPROM memory composed of one 1.5Kbyte Flash block divided into 384 sectors of 4 bytes
- Single bit fault correction and double bit fault detection within a word during read operations
- Automated program and erase algorithm with verify and generation of ECC parity bits
- Fast sector erase and word program operation
- Protection scheme to prevent accidental program or erase of EEPROM memory
- Ability to program up to four words in a burst sequence

26.1.2.3 Other Flash Module Features

- No external high-voltage power supply required for Flash memory program and erase operations
- Interrupt generation on Flash command completion and Flash error detection
- Security mechanism to prevent unauthorized access to the Flash memory

Register	Error Bit	Error Condition	
FSTAT	ACCERR	Set if CCOBIX[2:0] != 101 at command launch	
		Set if command not available in current mode (see Table 29-27)	
		Set if an invalid global address [17:0] is supplied (see Table 29-3)	
		Set if a misaligned phrase address is supplied (global address [2:0] != 000)	
	FPVIOL	Set if the global address [17:0] points to a protected area	
	MGSTAT1	Set if any errors have been encountered during the verify operation	
	MGSTAT0	Set if any non-correctable errors have been encountered during the verify operation	

Table 29-41. Program P-Flash Command Error Handling

29.4.6.6 Program Once Command

The Program Once command restricts programming to a reserved 64 byte field (8 phrases) in the nonvolatile information register located in P-Flash. The Program Once reserved field can be read using the Read Once command as described in Section 29.4.6.4. The Program Once command must only be issued once since the nonvolatile information register in P-Flash cannot be erased. The Program Once command must not be executed from the Flash block containing the Program Once reserved field to avoid code runaway.

CCOBIX[2:0]	FCCOB Parameters		
000	0x07	Not Required	
001	Program Once phrase index (0x0000 - 0x0007)		
010	Program Once word 0 value		
011	Program Once word 1 value		
100	Program Once word 2 value		
101	Program Once word 3 value		

Table 29-42. Program Once Command FCCOB Requirements

Upon clearing CCIF to launch the Program Once command, the Memory Controller first verifies that the selected phrase is erased. If erased, then the selected phrase will be programmed and then verified with read back. The CCIF flag will remain clear, setting only after the Program Once operation has completed.

The reserved nonvolatile information register accessed by the Program Once command cannot be erased and any attempt to program one of these phrases a second time will not be allowed. Valid phrase index values for the Program Once command range from 0x0000 to 0x0007. During execution of the Program Once command, any attempt to read addresses within P-Flash will return invalid data.

Field	Description	
3 MGBUSY	 Memory Controller Busy Flag — The MGBUSY flag reflects the active state of the Memory Controller. 0 Memory Controller is idle 1 Memory Controller is busy executing a Flash command (CCIF = 0) 	
2 RSVD	Reserved Bit — This bit is reserved and always reads 0.	
1–0 MGSTAT[1:0]	Memory Controller Command Completion Status Flag — One or more MGSTAT flag bits are set if an error is detected during execution of a Flash command or during the Flash reset sequence. See Section 30.4.6, "Flash Command Description," and Section 30.6, "Initialization" for details.	

Table 30-15. FSTAT Field Descriptions (continued)

30.3.2.8 Flash Error Status Register (FERSTAT)

Offset Module Base + 0x0007

The FERSTAT register reflects the error status of internal Flash operations.



Figure 30-12. Flash Error Status Register (FERSTAT)

All flags in the FERSTAT register are readable and only writable to clear the flag.

Table 30-16. FERSTAT Field Descriptions

Field	Description
1 DFDIF	 Double Bit Fault Detect Interrupt Flag — The setting of the DFDIF flag indicates that a double bit fault was detected in the stored parity and data bits during a Flash array read operation or that a Flash array read operation returning invalid data was attempted on a Flash block that was under a Flash command operation.¹ The DFDIF flag is cleared by writing a 1 to DFDIF. Writing a 0 to DFDIF has no effect on DFDIF.² 0 No double bit fault detected 1 Double bit fault detected or a Flash array read operation returning invalid data was attempted while command running
0 SFDIF	 Single Bit Fault Detect Interrupt Flag — With the IGNSF bit in the FCNFG register clear, the SFDIF flag indicates that a single bit fault was detected in the stored parity and data bits during a Flash array read operation or that a Flash array read operation returning invalid data was attempted on a Flash block that was under a Flash command operation.¹ The SFDIF flag is cleared by writing a 1 to SFDIF. Writing a 0 to SFDIF has no effect on SFDIF. 0 No single bit fault detected 1 Single bit fault detected and corrected or a Flash array read operation returning invalid data was attempted operation returning invalid data was attempted operation.
1 The single	hit fault and double hit fault flags are mutually evolusive for parity errors (an ECC fault accurrence can be either

The single bit fault and double bit fault flags are mutually exclusive for parity errors (an ECC fault occurrence can be either single fault or double fault but never both). A simultaneous access collision (Flash array read operation returning invalid data attempted while command running) is indicated when both SFDIF and DFDIF flags are high.

² There is a one cycle delay in storing the ECC DFDIF and SFDIF fault flags in this register. At least one NOP is required after a flash memory read before checking FERSTAT for the occurrence of ECC errors.

Upon clearing CCIF to launch the Set User Margin Level command, the Memory Controller will set the user margin level for the targeted block and then set the CCIF flag.

NOTE

When the EEPROM block is targeted, the EEPROM user margin levels are applied only to the EEPROM reads. However, when the P-Flash block is targeted, the P-Flash user margin levels are applied to both P-Flash and EEPROM reads. It is not possible to apply user margin levels to the P-Flash block only.

Valid margin level settings for the Set User Margin Level command are defined in Table 30-55.

CCOB (CCOBIX=001)	Level Description	
0x0000	Return to Normal Level	
0x0001	User Margin-1 Level ¹	
0x0002	User Margin-0 Level ²	

Table 30-55. Valid Set User Margin Level Settings

¹ Read margin to the erased state

² Read margin to the programmed state

Table 30-56. Set User Margin Level Command Error Handling

Register	Error Bit	Error Condition			
	ACCERR	Set if CCOBIX[2:0] != 001 at command launch.			
		Set if command not available in current mode (see Table 30-27).			
ESTAT		Set if an invalid margin level setting is supplied.			
FSIAI	FPVIOL	None			
	MGSTAT1	None			
	MGSTAT0	None			

NOTE

User margin levels can be used to check that Flash memory contents have adequate margin for normal level read operations. If unexpected results are encountered when checking Flash memory contents at user margin levels, a potential loss of information has been detected.

30.4.6.13 Set Field Margin Level Command

The Set Field Margin Level command, valid in special modes only, causes the Memory Controller to set the margin level specified for future read operations of the P-Flash or EEPROM block.

240 KByte Flash Module (S12FTMRG240K2V1)

Table 31-4). The Verify Backdoor Access Key command must not be executed from the Flash block containing the backdoor comparison key to avoid code runaway.

CCOBIX[2:0]	FCCOB Parameters			
000	0x0C	Not required		
001	Key 0			
010	Key 1			
011	Ke	y 2		
100	Ke	у З		

Table 31-52. Verify Backdoor Access Key Command FCCOB Requirements

Upon clearing CCIF to launch the Verify Backdoor Access Key command, the Memory Controller will check the FSEC KEYEN bits to verify that this command is enabled. If not enabled, the Memory Controller sets the ACCERR bit in the FSTAT register and terminates. If the command is enabled, the Memory Controller compares the key provided in FCCOB to the backdoor comparison key in the Flash configuration field with Key 0 compared to 0x3_FF00, etc. If the backdoor keys match, security will be released. If the backdoor keys do not match, security is not released and all future attempts to execute the Verify Backdoor Access Key command are aborted (set ACCERR) until a reset occurs. The CCIF flag is set after the Verify Backdoor Access Key operation has completed.

Table 31-53. Verify Backdoor Access Key Command Error Handling

Register	Error Bit	Error Condition			
	ACCERR	Set if CCOBIX[2:0] != 100 at command launch			
		Set if an incorrect backdoor key is supplied			
		Set if backdoor key access has not been enabled (KEYEN[1:0] != 10, see Section 31.3.2.2)			
FSTAT		Set if the backdoor key has mismatched since the last reset			
	FPVIOL	None			
	MGSTAT1	None			
	MGSTAT0	None			

31.4.6.12 Set User Margin Level Command

The Set User Margin Level command causes the Memory Controller to set the margin level for future read operations of the P-Flash or EEPROM block.

Table 31-54. Set User Margin Level Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters			
000	0x0D	Flash block selection code [1:0]. See Table 31-34		
001	Margin level setting.			

Conditions are 4.5 V < V_{DD35} < 5.5 V junction temperature from –40°C to +150°C, unless otherwise noted I/O Characteristics for all I/O pins except EXTAL, XTAL, TEST and supply pins.							
Num	С	Rating	Symbol	Min	Тур	Мах	Unit
1	Ρ	Input high voltage	V _{IH}	0.65*V _{DD35}	_	—	V
2	Т	Input high voltage	V _{IH}	—	_	V _{DD35} +0.3	V
3	Ρ	Input low voltage	V _{IL}	—	—	0.35*V _{DD35}	V
4	Т	Input low voltage	V _{IL}	V _{SSRX} -0.3	—	—	V
5	С	Input hysteresis	V _{HYS}	0.06*V _{DD35}	—	0.3*V _{DD35}	mV
6	Ρ	Input leakage current (pins in high impedance input mode) ¹ V _{in} = V _{DD35} or V _{SS35} +125°C to < T_J < 150°C +105°C to < T_J < 125° -40°C to < T_J < 105°C	l _{in}	-1 -0.5 -0.4		1 0.5 0.4	μΑ
7	Р	Output high voltage (pins in output mode) I _{OH} = -4 mA	V _{OH}	V _{DD35} – 0.8	_	—	V
8	Ρ	Output low voltage (pins in output mode) I _{OL} = +4mA	V _{OL}	—	—	0.8	V
9	Ρ	Internal pull up current V _{IH} min > input voltage > V _{IL} max	I _{PUL}	-10	—	-130	μA
10	Ρ	Internal pull down current V _{IH} min > input voltage > V _{IL} max	I _{PDH}	10	—	130	μA
11	D	Input capacitance	C _{in}	—	7	—	pF
12	Т	Injection current ² Single pin limit Total device Limit, sum of all injected currents	I _{ICS} I _{ICP}	2.5 25	_	2.5 25	mA

Table A-8. 5-V I/O Characteristics (Junction Temperature From –40°C To +150°C)

¹ Maximum leakage current occurs at maximum operating temperature. Current decreases by approximately one-half for each 8°°C to 12°C° in the temperature range from 50°C to 125°C.

² Refer to Section A.1.4, "Current Injection" for more details



