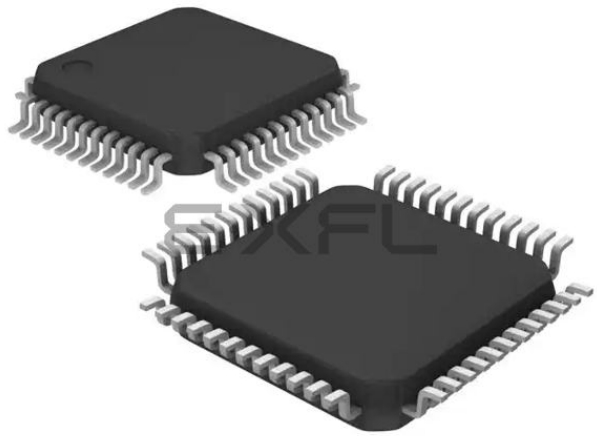

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	12V1
Core Size	16-Bit
Speed	25MHz
Connectivity	IrDA, LINbus, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	40
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3.13V ~ 5.5V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 150°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s9s12gna32f0wlf

Chapter 9
Security (S12XS9SECV2)

Chapter 10
S12 Clock, Reset and Power Management Unit (S12CPMU)

Table 1-9. 32-Pin LQFP OPinout for S12GN16 and S12GN32

	Function <----lowest-----PRIORITY-----highest---->					Power Supply	Internal Pull Resistor	
Package Pin	Pin	2nd Func.	3rd Func.	4th Func	5th Func		CTRL	Reset State
4	PE0[1]	EXTAL	—	—	—	—	PUCR/PDPEE	Down
5	VSS	—	—	—	—	—	—	—
6	PE1[1]	XTAL	—	—	—	—	PUCR/PDPEE	Down
7	TEST	—	—	—	—	N.A.	$\overline{\text{RESET}}$ pin	Down
8	BKGD	MODC	—	—	—	V_{DDX}	PUCR/BKPUE	Up
9	PP0	KWP0	ETRIG0	API_EXTCLK	PWM0	V_{DDX}	PERP/PPSP	Disabled
10	PP1	KWP1	ETRIG1	ECLKX2	PWM1	V_{DDX}	PERP/PPSP	Disabled
11	PP2	KWP2	ETRIG2	PWM2	—	V_{DDX}	PERP/PPSP	Disabled
12	PP3	KWP3	ETRIG3	PWM3	—	V_{DDX}	PERP/PPSP	Disabled
13	PT3	IOC3	—	—	—	V_{DDX}	PERT/PPST	Disabled
14	PT2	IOC2	—	—	—	V_{DDX}	PERT/PPST	Disabled
15	PT1	IOC1	$\overline{\text{IRQ}}$	—	—	V_{DDX}	PERT/PPST	Disabled
16	PT0	IOC0	$\overline{\text{XIRQ}}$	—	—	V_{DDX}	PERT/PPST	Disabled
17	PAD0	KWAD0	AN0	—	—	V_{DDA}	PER1AD/PPS1AD	Disabled
18	PAD1	KWAD1	AN1	—	—	V_{DDA}	PER1AD/PPS1AD	Disabled
19	PAD2	KWAD2	AN2	—	—	V_{DDA}	PER1AD/PPS1AD	Disabled
20	PAD3	KWAD3	AN3	—	—	V_{DDA}	PER1AD/PPS1AD	Disabled
21	PAD4	KWAD4	AN4	—	—	V_{DDA}	PER1AD/PPS1AD	Disabled
22	PAD5	KWAD5	AN5	ACMPO	—	V_{DDA}	PER1AD/PPS1AD	Disabled
23	PAD6	KWAD6	AN6	ACMPP	—	V_{DDA}	PER1AD/PPS1AD	Disabled
24	PAD7	KWAD7	AN7	ACMPM	—	V_{DDA}	PER1AD/PPS1AD	Disabled
25	PS0	RXD0	—	—	—	V_{DDX}	PERS/PPSS	Up
26	PS1	TXD0	—	—	—	V_{DDX}	PERS/PPSS	Up
27	PS4	PWM4	MISO0	—	—	V_{DDX}	PERS/PPSS	Up
28	PS5	IOC4	MOSI0	—	—	V_{DDX}	PERS/PPSS	Up
29	PS6	IOC5	SCK0	—	—	V_{DDX}	PERS/PPSS	Up
30	PS7	API_EXTCLK	ECLK	PWM5	$\overline{\text{SS0}}$	V_{DDX}	PERS/PPSS	Up
31	PM0	—	—	—	—	V_{DDX}	PERM/PPSM	Disabled

Table 1-21. 64-Pin LQFP Pinout for S12G96 and S12G128

	Function <----lowest-----PRIORITY-----highest---->					Power Supply	Internal Pull Resistor	
Package Pin	Pin	2nd Func.	3rd Func.	4th Func	5th Func		CTRL	Reset State
1	PJ6	KWJ6	SCK2	—	—	V_{DDX}	PERJ/PPSJ	Up
2	PJ5	KWJ5	MOSI2	—	—	V_{DDX}	PERJ/PPSJ	Up
3	PJ4	KWJ4	MISO2	—	—	V_{DDX}	PERJ/PPSJ	Up
4	RESET	—	—	—	—	V_{DDX}	PULLUP	
5	VDDX	—	—	—	—	—	—	—
6	VDDR	—	—	—	—	—	—	—
7	VSSX	—	—	—	—	—	—	—
8	PE0[1]	EXTAL	—	—	—	V_{DDX}	PUCR/PDPEE	Down
9	VSS	—	—	—	—	—	—	—
10	PE1[1]	XTAL	—	—	—	V_{DDX}	PUCR/PDPEE	Down
11	TEST	—	—	—	—	N.A.	$\overline{\text{RESET}}$ pin	Down
12	PJ0	KWJ0	MISO1	—	—	V_{DDX}	PERJ/PPSJ	Up
13	PJ1	KWJ1	MOSI1	—	—	V_{DDX}	PERJ/PPSJ	Up
14	PJ2	KWJ2	SCK1	—	—	V_{DDX}	PERJ/PPSJ	Up
15	PJ3	KWJ3	$\overline{\text{SS1}}$	—	—	V_{DDX}	PERJ/PPSJ	Up
16	BKGD	MODC	—	—	—	V_{DDX}	PUCR/BKPUE	Up
17	PP0	KWP0	ETRIG0	API_EXTCLK	PWM0	V_{DDX}	PERP/PPSP	Disabled
18	PP1	KWP1	ETRIG1	ECLKX2	PWM1	V_{DDX}	PERP/PPSP	Disabled
19	PP2	KWP2	ETRIG2	PWM2	—	V_{DDX}	PERP/PPSP	Disabled
20	PP3	KWP3	ETRIG3	PWM3	—	V_{DDX}	PERP/PPSP	Disabled
21	PP4	KWP4	PWM4	—	—	V_{DDX}	PERP/PPSP	Disabled
22	PP5	KWP5	PWM5	—	—	V_{DDX}	PERP/PPSP	Disabled
23	PP6	KWP6	PWM6	—	—	V_{DDX}	PERP/PPSP	Disabled
24	PP7	KWP7	PWM7	—	—	V_{DDX}	PERP/PPSP	Disabled
25	PT7	IOC7	—	—	—	V_{DDX}	PERT/PPST	Disabled
26	PT6	IOC6	—	—	—	V_{DDX}	PERT/PPST	Disabled
27	PT5	IOC5	—	—	—	V_{DDX}	PERT/PPST	Disabled

Table 1-25. 100-Pin LQFP Pinout for S12GA96 and S12GA128

	Function <----lowest-----PRIORITY-----highest---->				Power Supply	Internal Pull Resistor	
Package Pin	Pin	2nd Func.	3rd Func.	4th Func.		CTRL	Reset State
86	PS4	MISO0	—	—	V_{DDX}	PERS/PPSS	Up
87	PS5	MOSI0	—	—	V_{DDX}	PERS/PPSS	Up
88	PS6	SCK0	—	—	V_{DDX}	PERS/PPSS	Up
89	PS7	API_EXTCLK	$\overline{SS0}$	—	V_{DDX}	PERS/PPSS	Up
90	VSSX2	—	—	—	—	—	—
91	VDDX2	—	—	—	—	—	—
92	PM0	RXCAN	—	—	V_{DDX}	PERM/PPSM	Disabled
93	PM1	TXCAN	—	—	V_{DDX}	PERM/PPSM	Disabled
94	PD4	—	—	—	V_{DDX}	PUCR/PUPDE	Disabled
95	PD5	—	—	—	V_{DDX}	PUCR/PUPDE	Disabled
96	PD6	—	—	—	V_{DDX}	PUCR/PUPDE	Disabled
97	PD7	—	—	—	V_{DDX}	PUCR/PUPDE	Disabled
98	PM2	RXD2	—	—	V_{DDX}	PERM/PPSM	Disabled
99	PM3	TXD2	—	—	V_{DDX}	PERM/PPSM	Disabled
100	PJ7	KWJ7	$\overline{SS2}$	—	V_{DDX}	PERJ/PPSJ	Up

[1] The regular I/O characteristics (see Section A.2, “I/O Characteristics”) apply if the EXTAL/XTAL function is disabled

2.4.3.15 Port T Data Register (PTT)

Address 0x0240 (G1, G2) Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	PTT7	PTT6	PTT5	PTT4	PTT3	PTT2	PTT1	PTT0
W								
Reset	0	0	0	0	0	0	0	0

Address 0x0240 (G3) Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	0	0	PTT5	PTT4	PTT3	PTT2	PTT1	PTT0
W								
Reset	0	0	0	0	0	0	0	0

Figure 2-16. Port T Data Register (PTT)

[1] Read: Anytime. The data source is depending on the data direction value.
Write: Anytime

Table 2-35. PTT Register Field Descriptions

Field	Description
7-0 PTT	**Port T general-purpose input/output data**—Data Register When not used with an alternative signal, the associated pin can be used as general-purpose I/O. In general-purpose output mode the port data register bit value is driven to the pin. If the associated data direction bit is set to 1, a read returns the value of the port data register bit, otherwise the buffered pin input state is read.

2.4.3.16 Port T Input Register (PTIT)

Address 0x0241 (G1, G2) Access: User read only[1]

	7	6	5	4	3	2	1	0
R	PTIT7	PTIT6	PTIT5	PTIT4	PTIT3	PTIT2	PTIT1	PTIT0
W								
Reset	0	0	0	0	0	0	0	0

Address 0x0241 (G3) Access: User read only[1]

	7	6	5	4	3	2	1	0
R	0	0	PTIT5	PTIT4	PTIT3	PTIT2	PTIT1	PTIT0
W								
Reset	0	0	0	0	0	0	0	0

Figure 2-17. Port T Input Register (PTIT)

[1] Read: Anytime
Write:Never

Table 2-36. PTIT Register Field Descriptions

Field	Description
7-0 PTIT	**Port T input data—** A read always returns the buffered input state of the associated pin. It can be used to detect overload or short circuit conditions on output pins.

2.4.3.17 Port T Data Direction Register (DDRT)

Address 0x0242 (G1, G2) Access: User read/write[1]

	7	6	5	4	3	2	1	0
R W	DDRT7	DDRT6	DDRT5	DDRT4	DDRT3	DDRT2	DDRT1	DDRT0
Reset	0	0	0	0	0	0	0	0

Address 0x0242 (G3) Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	0	0	DDRT5	DDRT4	DDRT3	DDRT2	DDRT1	DDRT0
W								
Reset	0	0	0	0	0	0	0	0

Figure 2-18. Port T Data Direction Register (DDRT)

[1] Read: Anytime
Write: Anytime

Table 2-37. DDRT Register Field Descriptions

Field	Description
7-0 DDRT	**Port T data direction—** This bit determines whether the pin is a general-purpose input or output. 1 Associated pin configured as output 0 Associated pin configured as input

to erase the EEPROM and Flash memory without giving access to their contents. After erasing both Flash memory and EEPROM, another reset into special single chip mode will cause the blank check to succeed and the options/security byte can be programmed to “unsecured” state via BDM.

While the BDM is executing the blank check, the BDM interface is completely blocked, which means that all BDM commands are temporarily blocked.

9.1.5 Unsecuring the Microcontroller

Unsecuring the microcontroller can be done by three different methods:

1. Backdoor key access
2. Reprogramming the security bits
3. Complete memory erase (special modes)

9.1.5.1 Unsecuring the MCU Using the Backdoor Key Access

In normal modes (single chip and expanded), security can be temporarily disabled using the backdoor key access method. This method requires that:

- The backdoor key at 0xFF00–0xFF07 (= global addresses 0x3_FF00–0x3_FF07) has been programmed to a valid value.
- The KEYEN[1:0] bits within the Flash options/security byte select ‘enabled’.
- In single chip mode, the application program programmed into the microcontroller must be designed to have the capability to write to the backdoor key locations.

The backdoor key values themselves would not normally be stored within the application data, which means the application program would have to be designed to receive the backdoor key values from an external source (e.g. through a serial port).

The backdoor key access method allows debugging of a secured microcontroller without having to erase the Flash. This is particularly useful for failure analysis.

NOTE

No word of the backdoor key is allowed to have the value 0x0000 or 0xFFFF.

9.1.6 Reprogramming the Security Bits

In normal single chip mode (NS), security can also be disabled by erasing and reprogramming the security bits within Flash options/security byte to the unsecured value. Because the erase operation will erase the entire sector from 0xFE00–0xFFFF (0x7F_FE00–0x7F_FFFF), the backdoor key and the interrupt vectors will also be erased; this method is not recommended for normal single chip mode. The application software can only erase and program the Flash options/security byte if the Flash sector containing the Flash options/security byte is not protected (see Flash protection). Thus Flash protection is a useful means of preventing this method. The microcontroller will enter the unsecured state after the next reset following the programming of the security bits to the unsecured value.

Table 10-14. COP Watchdog Rates if COPOSCSEL1=1

CR2	CR1	CR0	COPCLK Cycles to Time-out (COPCLK is ACLK - internal RC-Oscillator clock)
0	0	0	COP disabled
0	0	1	2^7
0	1	0	2^9
0	1	1	2^{11}
1	0	0	2^{13}
1	0	1	2^{15}
1	1	0	2^{16}
1	1	1	2^{17}

10.3.2.10 Reserved Register CPMUTEST0

NOTE

This reserved register is designed for factory test purposes only, and is not intended for general user access. Writing to this register when in Special Mode can alter the S12CPMU's functionality.

0x003D

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 10-13. Reserved Register (CPMUTEST0)

Read: Anytime

Write: Only in Special Mode

10.3.2.11 Reserved Register CPMUTEST1

NOTE

This reserved register is designed for factory test purposes only, and is not intended for general user access. Writing to this register when in Special Mode can alter the S12CPMU's functionality.

11.2 Signal Description

This section lists all inputs to the ADC10B8C block.

11.2.1 Detailed Signal Descriptions

11.2.1.1 AN*x* (*x* = 7, 6, 5, 4, 3, 2, 1, 0)

This pin serves as the analog input Channel *x*. It can also be configured as digital port or external trigger for the ATD conversion.

11.2.1.2 ETRIG3, ETRIG2, ETRIG1, ETRIG0

These inputs can be configured to serve as an external trigger for the ATD conversion.

Refer to device specification for availability and connectivity of these inputs!

11.2.1.3 VRH, VRL

VRH is the high reference voltage, VRL is the low reference voltage for ATD conversion.

11.2.1.4 VDDA, VSSA

These pins are the power supplies for the analog circuitry of the ADC10B8C block.

11.3 Memory Map and Register Definition

This section provides a detailed description of all registers accessible in the ADC10B8C.

11.3.1 Module Memory Map

Figure 11-2 gives an overview on all ADC10B8C registers.

NOTE

Register Address = Base Address + Address Offset, where the Base Address is defined at the MCU level and the Address Offset is defined at the module level.

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0000	ATDCTL0	R W	Reserved	0	0	0	WRAP3	WRAP2	WRAP1	WRAP0
0x0001	ATDCTL1	R W	ETRIGSEL	SRES1	SRES0	SMP_DIS	ETRIGCH3	ETRIGCH2	ETRIGCH1	ETRIGCH0
0x0002	ATDCTL2	R W	0	AFFC	Reserved	ETRIGLE	ETRIGP	ETRIGE	ASCIE	ACMPIE

= Unimplemented or Reserved

Figure 11-2. ADC10B8C Register Summary (Sheet 1 of 2)

Table 18-12. CANRIER Register Field Descriptions

Field	Description
7 WUPIE[1]	**Wake-Up Interrupt Enable** 0 No interrupt request is generated from this event. 1 A wake-up event causes a Wake-Up interrupt request.
6 CSCIE	**CAN Status Change Interrupt Enable** 0 No interrupt request is generated from this event. 1 A CAN Status Change event causes an error interrupt request.
5-4 RSTATE[1:0]	**Receiver Status Change Enable** — These RSTAT enable bits control the sensitivity level in which receiver state changes are causing CSCIF interrupts. Independent of the chosen sensitivity level the RSTAT flags continue to indicate the actual receiver state and are only updated if no CSCIF interrupt is pending. 00 Do not generate any CSCIF interrupt caused by receiver state changes. 01 Generate CSCIF interrupt only if the receiver enters or leaves “bus-off” state. Discard other receiver state changes for generating CSCIF interrupt. 10 Generate CSCIF interrupt only if the receiver enters or leaves “RxErr” or “bus-off”[2] state. Discard other receiver state changes for generating CSCIF interrupt. 11 Generate CSCIF interrupt on all state changes.
3-2 TSTATE[1:0]	**Transmitter Status Change Enable** — These TSTAT enable bits control the sensitivity level in which transmitter state changes are causing CSCIF interrupts. Independent of the chosen sensitivity level, the TSTAT flags continue to indicate the actual transmitter state and are only updated if no CSCIF interrupt is pending. 00 Do not generate any CSCIF interrupt caused by transmitter state changes. 01 Generate CSCIF interrupt only if the transmitter enters or leaves “bus-off” state. Discard other transmitter state changes for generating CSCIF interrupt. 10 Generate CSCIF interrupt only if the transmitter enters or leaves “TxErr” or “bus-off” state. Discard other transmitter state changes for generating CSCIF interrupt. 11 Generate CSCIF interrupt on all state changes.
1 OVRIE	**Overrun Interrupt Enable** 0 No interrupt request is generated from this event. 1 An overrun event causes an error interrupt request.
0 RXFIE	**Receiver Full Interrupt Enable** 0 No interrupt request is generated from this event. 1 A receive buffer full (successful message reception) event causes a receiver interrupt request.

1 WUPIE and WUPE (see Section 18.3.2.1, “MSCAN Control Register 0 (CANCTL0)”) must both be enabled if the recovery mechanism from stop or wait is required.

2 Bus-off state is only defined for transmitters by the CAN standard (see Bosch CAN 2.0A/B protocol specification). Because the only possible state change for the transmitter from bus-off to TxOK also forces the receiver to skip its current state to RxOK, the coding of the RXSTAT[1:0] flags define an additional bus-off state for the receiver (see Section 18.3.2.5, “MSCAN Receiver Flag Register (CANRFLG)”).

18.3.2.7 MSCAN Transmitter Flag Register (CANTFLG)

The transmit buffer empty flags each have an associated interrupt enable bit in the CANTIER register.

18.3.2.15 MSCAN Receive Error Counter (CANRXERR)

This register reflects the status of the MSCAN receive error counter.

Module Base + 0x000E — Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	RXERR7	RXERR6	RXERR5	RXERR4	RXERR3	RXERR2	RXERR1	RXERR0
W								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 18-18. MSCAN Receive Error Counter (CANRXERR)

[1] Read: Only when in sleep mode (SLPRQ = 1 and SLPAK = 1) or initialization mode (INITRQ = 1 and INITAK = 1)
Write: Unimplemented

NOTE

Reading this register when in any other mode other than sleep or initialization mode may return an incorrect value. For MCUs with dual CPUs, this may result in a CPU fault condition.

18.3.2.16 MSCAN Transmit Error Counter (CANTXERR)

This register reflects the status of the MSCAN transmit error counter.

Module Base + 0x000F — Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	TXERR7	TXERR6	TXERR5	TXERR4	TXERR3	TXERR2	TXERR1	TXERR0
W								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 18-19. MSCAN Transmit Error Counter (CANTXERR)

[1] Read: Only when in sleep mode (SLPRQ = 1 and SLPAK = 1) or initialization mode (INITRQ = 1 and INITAK = 1)
Write: Unimplemented

NOTE

Reading this register when in any other mode other than sleep or initialization mode, may return an incorrect value. For MCUs with dual CPUs, this may result in a CPU fault condition.

For microcontrollers without a clock and reset generator (CRG), CANCLK is driven from the crystal oscillator (oscillator clock).

A programmable prescaler generates the time quanta (Tq) clock from CANCLK. A time quantum is the atomic unit of time handled by the MSCAN.

Eqn. 18-2

$$\Gamma q = \frac{f_{CANCLK}}{(Prescaler\ \ value}$$

A bit time is subdivided into three segments as described in the Bosch CAN 2.0A/B specification. (see Figure 18-44):

- SYNC_SEG: This segment has a fixed length of one time quantum. Signal edges are expected to happen within this section.
- Time Segment 1: This segment includes the PROP_SEG and the PHASE_SEG1 of the CAN standard. It can be programmed by setting the parameter TSEG1 to consist of 4 to 16 time quanta.
- Time Segment 2: This segment represents the PHASE_SEG2 of the CAN standard. It can be programmed by setting the TSEG2 parameter to be 2 to 8 time quanta long.

Eqn. 18-3

$$Bit\ \ Rate = \frac{f_{Tq}}{(number\ \ of\ \ Time\ \ Quanta)}$$

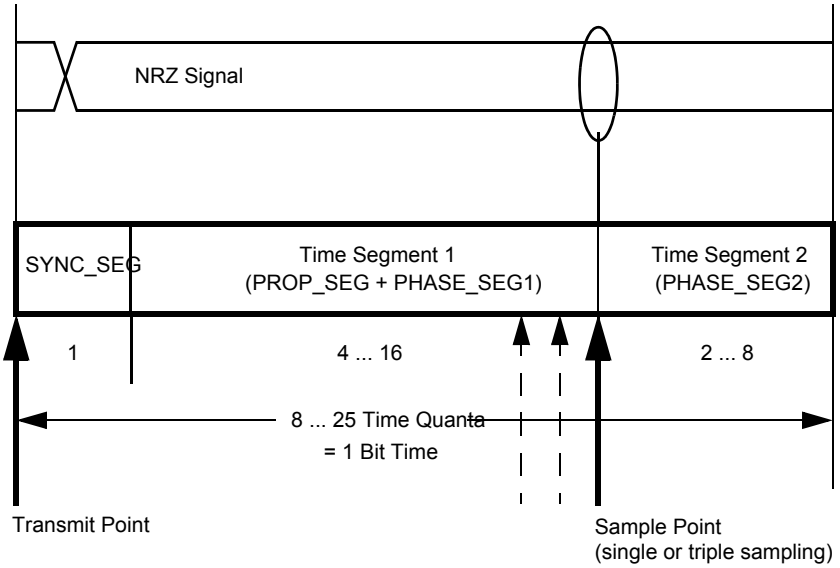


Figure 18-44. Segments within the Bit Time

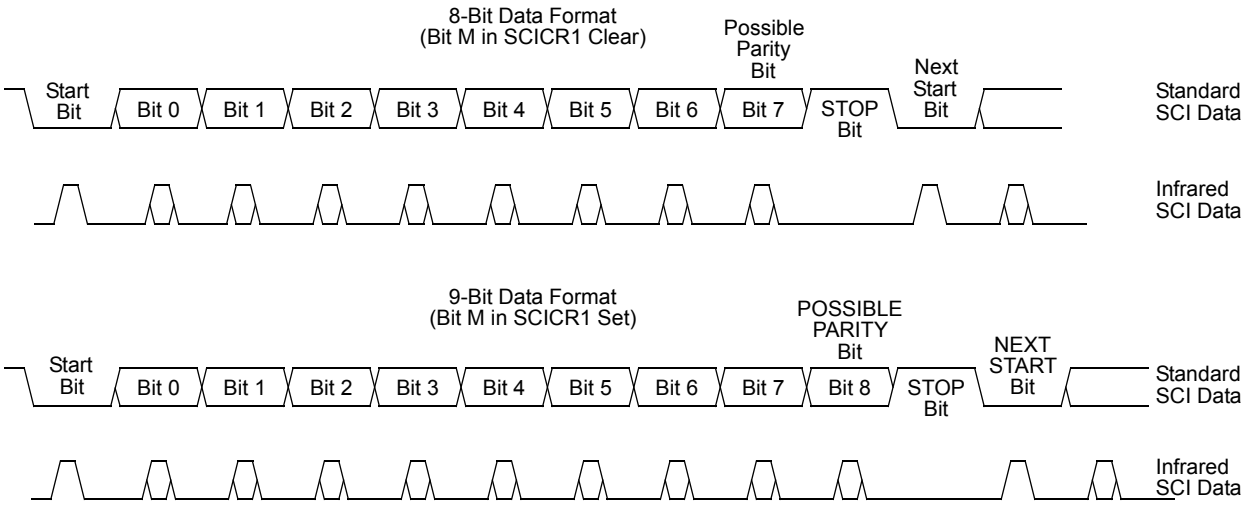


Figure 20-15. SCI Data Formats

Each data character is contained in a frame that includes a start bit, eight or nine data bits, and a stop bit. Clearing the M bit in SCI control register 1 configures the SCI for 8-bit data characters. A frame with eight data bits has a total of 10 bits. Setting the M bit configures the SCI for nine-bit data characters. A frame with nine data bits has a total of 11 bits.

Table 20-14. Example of 8-Bit Data Formats

Start Bit	Data Bits	Address Bits	Parity Bits	Stop Bit
1	8	0	0	1
1	7	0	1	1
1	7	1[1]	0	1

1 The address bit identifies the frame as an address character. See Section 20.4.6.6, “Receiver Wakeup”.

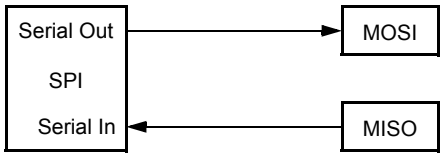
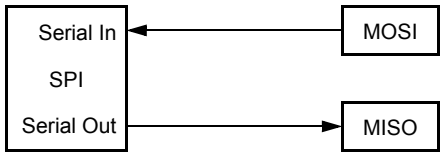
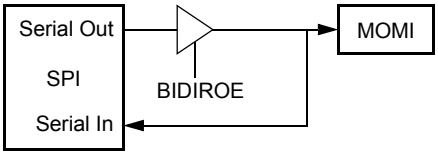
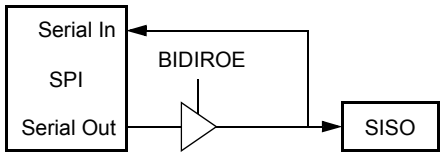
When the SCI is configured for 9-bit data characters, the ninth data bit is the T8 bit in SCI data register high (SCIDRH). It remains unchanged after transmission and can be used repeatedly without rewriting it. A frame with nine data bits has a total of 11 bits.

Table 20-15. Example of 9-Bit Data Formats

Start Bit	Data Bits	Address Bits	Parity Bits	Stop Bit
1	9	0	0	1
1	8	0	1	1
1	8	1[1]	0	1

1 The address bit identifies the frame as an address character. See Section 20.4.6.6, “Receiver Wakeup”.

Table 21-10. Normal Mode and Bidirectional Mode

When SPE = 1	Master Mode MSTR = 1	Slave Mode MSTR = 0
Normal Mode SPC0 = 0		
Bidirectional Mode SPC0 = 1		

The direction of each serial I/O pin depends on the BIDIROE bit. If the pin is configured as an output, serial data from the shift register is driven out on the pin. The same pin is also the serial input to the shift register.

- The SCK is output for the master mode and input for the slave mode.
- The $\overline{SS}$ is the input or output for the master mode, and it is always the input for the slave mode.
- The bidirectional mode does not affect SCK and $\overline{SS}$ functions.

NOTE

In bidirectional master mode, with mode fault enabled, both data pins MISO and MOSI can be occupied by the SPI, though MOSI is normally used for transmissions in bidirectional mode and MISO is not used by the SPI. If a mode fault occurs, the SPI is automatically switched to slave mode. In this case MISO becomes occupied by the SPI and MOSI is not used. This must be considered, if the MISO pin is used for another purpose.

21.4.6 Error Conditions

The SPI has one error condition:

- Mode fault error

21.4.6.1 Mode Fault Error

If the $\overline{SS}$ input becomes low while the SPI is configured as a master, it indicates a system error where more than one master may be trying to drive the MOSI and SCK lines simultaneously. This condition is not permitted in normal operation, the MODF bit in the SPI status register is set automatically, provided the MODFEN bit is set.

In the special case where the SPI is in master mode and MODFEN bit is cleared, the $\overline{SS}$ pin is not used by the SPI. In this special case, the mode fault error function is inhibited and MODF remains cleared. In case

Table 24-47. Erase P-Flash Sector Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 001 at command launch
		Set if command not available in current mode (see Table 24-25)
		Set if an invalid global address [17:16] is supplied see Table 24-3)[1]
		Set if a misaligned phrase address is supplied (global address [2:0] != 000)
	FPVIOL	Set if the selected P-Flash sector is protected
	MGSTAT1	Set if any errors have been encountered during the verify operation
	MGSTAT0	Set if any non-correctable errors have been encountered during the verify operation

1 As defined by the memory map for FTMRG32K1.

24.4.6.10 Unsecure Flash Command

The Unsecure Flash command will erase the entire P-Flash and EEPROM memory space and, if the erase is successful, will release security.

Table 24-48. Unsecure Flash Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x0B	Not required

Upon clearing CCIF to launch the Unsecure Flash command, the Memory Controller will erase the entire P-Flash and EEPROM memory space and verify that it is erased. If the Memory Controller verifies that the entire Flash memory space was properly erased, security will be released. If the erase verify is not successful, the Unsecure Flash operation sets MGSTAT1 and terminates without changing the security state. During the execution of this command (CCIF=0) the user must not write to any Flash module register. The CCIF flag is set after the Unsecure Flash operation has completed.

Table 24-49. Unsecure Flash Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 000 at command launch
		Set if command not available in current mode (see Table 24-25)
	FPVIOL	Set if any area of the P-Flash or EEPROM memory is protected
	MGSTAT1	Set if any errors have been encountered during the verify operation[1]
	MGSTAT0	Set if any non-correctable errors have been encountered during the verify operation[1]

1 As found in the memory map for FTMRG32K1.

The user code stored in the P-Flash memory must have a method of receiving the backdoor keys from an external stimulus. This external stimulus would typically be through one of the on-chip serial ports.

If the KEYEN[1:0] bits are in the enabled state (see Section 25.3.2.2), the MCU can be unsecured by the backdoor key access sequence described below:

1. Follow the command sequence for the Verify Backdoor Access Key command as explained in Section 25.4.6.11
2. If the Verify Backdoor Access Key command is successful, the MCU is unsecured and the SEC[1:0] bits in the FSEC register are forced to the unsecure state of 10

The Verify Backdoor Access Key command is monitored by the Memory Controller and an illegal key will prohibit future use of the Verify Backdoor Access Key command. A reset of the MCU is the only method to re-enable the Verify Backdoor Access Key command. The security as defined in the Flash security byte (0x3_FF0F) is not changed by using the Verify Backdoor Access Key command sequence. The backdoor keys stored in addresses 0x3_FF00-0x3_FF07 are unaffected by the Verify Backdoor Access Key command sequence. The Verify Backdoor Access Key command sequence has no effect on the program and erase protections defined in the Flash protection register, FPROT.

After the backdoor keys have been correctly matched, the MCU will be unsecured. After the MCU is unsecured, the sector containing the Flash security byte can be erased and the Flash security byte can be reprogrammed to the unsecure state, if desired. In the unsecure state, the user has full control of the contents of the backdoor keys by programming addresses 0x3_FF00-0x3_FF07 in the Flash configuration field.

25.5.2 Unsecuring the MCU in Special Single Chip Mode using BDM

A secured MCU can be unsecured in special single chip mode by using the following method to erase the P-Flash and EEPROM memory:

1. Reset the MCU into special single chip mode
2. Delay while the BDM executes the Erase Verify All Blocks command write sequence to check if the P-Flash and EEPROM memories are erased
3. Send BDM commands to disable protection in the P-Flash and EEPROM memory
4. Execute the Erase All Blocks command write sequence to erase the P-Flash and EEPROM memory. Alternatively the Unsecure Flash command can be executed, if so the steps 5 and 6 below are skeeped.
5. After the CCIF flag sets to indicate that the Erase All Blocks operation has completed, reset the MCU into special single chip mode
6. Delay while the BDM executes the Erase Verify All Blocks command write sequence to verify that the P-Flash and EEPROM memory are erased

If the P-Flash and EEPROM memory are verified as erased, the MCU will be unsecured. All BDM commands will now be enabled and the Flash security byte may be programmed to the unsecure state by continuing with the following steps:

7. Send BDM commands to execute the Program P-Flash command write sequence to program the Flash security byte to the unsecured state

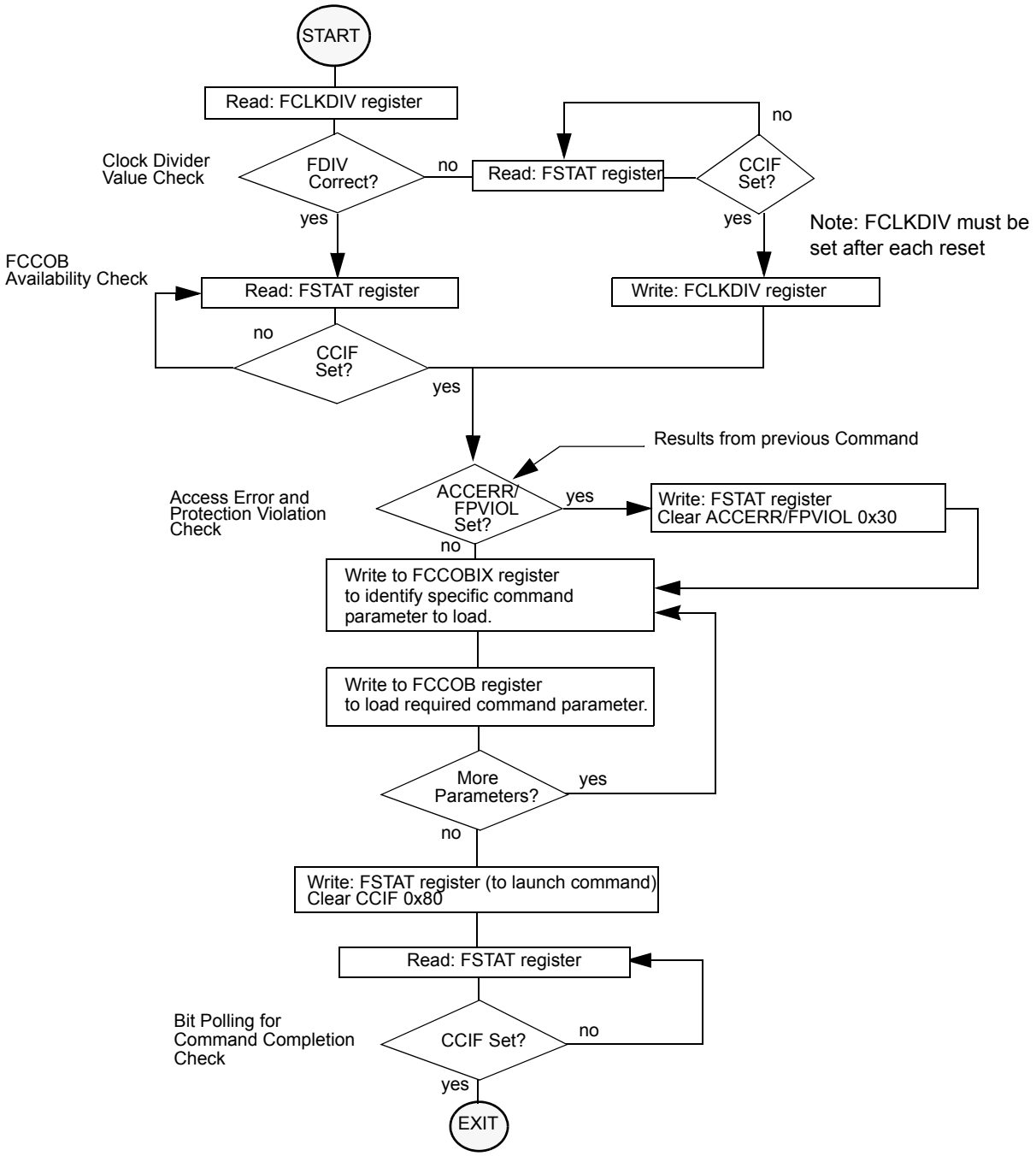


Figure 26-26. Generic Flash Command Write Sequence Flowchart

Table 29-4). The Verify Backdoor Access Key command must not be executed from the Flash block containing the backdoor comparison key to avoid code runaway.

Table 29-52. Verify Backdoor Access Key Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x0C	Not required
001	Key 0	
010	Key 1	
011	Key 2	
100	Key 3	

Upon clearing CCIF to launch the Verify Backdoor Access Key command, the Memory Controller will check the FSEC KEYEN bits to verify that this command is enabled. If not enabled, the Memory Controller sets the ACCERR bit in the FSTAT register and terminates. If the command is enabled, the Memory Controller compares the key provided in FCCOB to the backdoor comparison key in the Flash configuration field with Key 0 compared to 0x3_FF00, etc. If the backdoor keys match, security will be released. If the backdoor keys do not match, security is not released and all future attempts to execute the Verify Backdoor Access Key command are aborted (set ACCERR) until a reset occurs. The CCIF flag is set after the Verify Backdoor Access Key operation has completed.

Table 29-53. Verify Backdoor Access Key Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 100 at command launch
		Set if an incorrect backdoor key is supplied
		Set if backdoor key access has not been enabled (KEYEN[1:0] != 10, see Section 29.3.2.2)
		Set if the backdoor key has mismatched since the last reset
	FPVIOL	None
	MGSTAT1	None
	MGSTAT0	None

29.4.6.12 Set User Margin Level Command

The Set User Margin Level command causes the Memory Controller to set the margin level for future read operations of the P-Flash or EEPROM block.

Table 29-54. Set User Margin Level Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x0D	Flash block selection code [1:0]. See Table 29-34
001	Margin level setting.	

Table A-21. ADC Conversion Performance 5V range (Junction Temperature From –40°C To +150°C)

S12GNA16, S12GNA32, S12GAS48, S12GA64, S12GA96, S12GA128, S12GA192 and S12GA240								
Supply voltage 4.5V < V_{DDA} < 5.5 V, -40°C < T_J < 150°C, V_{REF} = V_{RH} - V_{RL} = V_{DDA}, f_{ADCCLK} = 8.0MHz The values are tested to be valid with no port AD output drivers switching simultaneous with conversions.								
Num	**C**	**Rating**[1]		**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	P	Resolution	12-Bit	LSB		1.25		mV
2	P	Differential Nonlinearity	12-Bit	DNL	-4	±2	4	counts
3	P	Integral Nonlinearity	12-Bit	INL	-5	±2.5	5	counts
4	P	Absolute Error[2]	12-Bit	AE	-7	±4	7	counts
5	C	Resolution	10-Bit	LSB		5		mV
6	C	Differential Nonlinearity	10-Bit	DNL	-1	±0.5	1	counts
7	C	Integral Nonlinearity	10-Bit	INL	-2	±1	2	counts
8	C	Absolute Error[2]	10-Bit	AE	-3	±2	3	counts
9	C	Resolution	8-Bit	LSB		20		mV
10	C	Differential Nonlinearity	8-Bit	DNL	-0.5	±0.3	0.5	counts
11	C	Integral Nonlinearity	8-Bit	INL	-1	±0.5	1	counts
12	C	Absolute Error[2]	8-Bit	AE	-1.5	±1	1.5	counts

1 The 8-bit and 10-bit mode operation is structurally tested in production test. Absolute values are tested in 12-bit mode.

2 These values include the quantization error which is inherently 1/2 count for any A/D converter.

Table A-37. NVM Timing Characteristics)

S12G96, S12GA96, S12G128, S12GA128									
Num	**Command**	**f_{NVMOP} cycle**	**f_{NVMBUS} cycle**	**Symbol**	**Min[1]**	**Typ[2]**	**Max[3]**	**Lfmax[4]**	**Unit**
1	Erase Verify All Blocks[5,6]	0	35345	t_{RD1ALL}	1.41	1.41	2.83	70.69	ms
2	Erase Verify Block (Pflash)[5]	0	33308	t_{RD1BLK_P}	1.33	1.33	2.66	66.62	ms
3	Erase Verify Block (EEPROM)[6]	0	2536	t_{RD1BLK_D}	0.1	0.1	0.2	5.07	ms
4	Erase Verify P-Flash Section	0	476	t_{RD1SEC}	19.04	19.04	38.08	952	ms
5	Read Once	0	445	t_{RDONCE}	17.8	17.8	17.8	445	µs
6	Program P-Flash (4 Word)	164	2925	t_{PGM_4}	0.27	0.28	0.63	11.91	ms
7	Program Once	164	2888	$t_{PGMONCE}$	0.27	0.28	0.28	3.09	ms
8	Erase All Blocks[5,6]	100066	35681	t_{ERSALL}	96.73	101.49	102.92	196.44	ms
9	Erase Flash Block (Pflash)[5]	100060	33541	t_{ERSBLK_P}	96.64	101.4	102.74	192.16	ms
10	Erase Flash Block (EEPROM)[6]	100060	2832	t_{ERSBLK_D}	95.41	100.17	100.29	130.74	ms
11	Erase P-Flash Sector	20015	865	t_{ERSPG}	19.1	20.05	20.08	26.75	ms
12	Unsecure Flash	100066	35759	t_{UNSECU}	96.73	101.5	102.93	196.6	ms
13	Verify Backdoor Access Key	0	481	t_{VFYKEY}	19.24	19.24	19.24	481	µs
14	Set User Margin Level	0	399	t_{MLOADU}	15.96	15.96	15.96	399	µs
15	Set Factory Margin Level	0	408	t_{MLOADF}	16.32	16.32	16.32	408	µs
16	Erase Verify EEPROM Section	0	546	$t_{DRD1SEC}$	0.02	0.02	0.04	1.09	ms
17	Program EEPROM (1 Word)	68	1565	t_{DPGM_1}	0.13	0.13	0.32	6.35	ms
18	Program EEPROM (2 Word)	136	2512	t_{DPGM_2}	0.23	0.24	0.54	10.22	ms
19	Program EEPROM (3 Word)	204	3459	t_{DPGM_3}	0.33	0.34	0.76	14.09	ms
20	Program EEPROM (4 Word)	272	4406	t_{DPGM_4}	0.44	0.45	0.98	17.96	ms
21	Erase EEPROM Sector	5015	753	t_{DERSPG}	4.81	5.05	20.57	37.88	ms

1 Minimum times are based on maximum f_{NVMOP} and maximum f_{NVMBUS}

2 Typical times are based on typical f_{NVMOP} and typical f_{NVMBUS}

3 Maximum times are based on typical f_{NVMOP} and typical f_{NVMBUS} plus aging

4 Lowest-frequency max times are based on minimum f_{NVMOP} and minimum f_{NVMBUS} plus aging

5 Affected by Pflash size

6 Affected by EEPROM size