Renesas Electronics America Inc - M30260F3AGP#U7A Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	M16C/60
Core Size	16-Bit
Speed	20MHz
Connectivity	I²C, IEBus, SIO, UART/USART
Peripherals	DMA, PWM, Voltage Detect, WDT
Number of I/O	39
Program Memory Size	24KB (24K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/m30260f3agp-u7a

2. Notation of Numbers and Symbols

The notation conventions for register names, bit names, numbers, and symbols used in this manual are described below.

(1) Register Names, Bit Names, and Pin Names

Registers, bits, and pins are referred to in the text by symbols. The symbol is accompanied by the word "register," "bit," or "pin" to distinguish the three categories.

Examples the PM03 bit in the PM0 register
P3_5 pin, VCC pin

(2) Notation of Numbers

The indication "$_2$" is appended to numeric values given in binary format. However, nothing is appended to the values of single bits. The indication "$_{16}$" is appended to numeric values given in hexadecimal format. Nothing is appended to numeric values given in decimal format.

Examples Binary: 11_2
Hexadecimal: $EFA0_{16}$
Decimal: 1234

Table 1.2. Performance outline of M16C/26A group (M16C/26A, M16C/26B) (42-pin package)

	Item	Performance
CPU	Basic instructions	91 instructions
	Minimun instruction execution time	41.7 ns (f(BCLK) = 24 MHz (3), VCC = 4.2 to 5.5 V (M16C/26B) 50 ns (f(BCLK) = 20 MHz, Vcc = 3.0 to 5.5 V) (M16C/26A, M16C/26B) 100 ns (f(BCLK) = 10 MHz, Vcc = 2.7 to 5.5 V) (M16C/26A, M16C/26B)
	Operation mode	Single-chip mode
	Address space	1M byte
	Memory capacity	ROM/RAM: See **1.4 Product Information**
Peripheral function	Port	33 I/O pins
	Multifunction timer	Timer A: 16 bits x 5 channels, Timer B: 16 bits x 3 channels Three-phase motor control timer
	Serial I/O	1 channel (UART, clock synchronous serial I/O) 1 channel (UART, clock synchronous, I^2C bus, or IEBus(1))
	A/D converter	10 bit A/D converter: 1 circuit, 10 channels
	DMAC	2 channels
	CRC calcuration circuit	1 circuits (CRC-CCITT and CRC-16) with MSB/LSB selectable
	Watchdog timer	15 bits x 1 channel (with prescaler)
	Interrupt	18 internal and 8 external sources, 4 software sources, Interrupt priority level: 7
	Clock generation circuit	4 circuits Main clock(*), Sub-clock(*) On-chip oscillator, PLL frequency synthesizer (*)Equipped with a built-in feedback resister.
	Oscillation stop detection	Main clock oscillation stop, re-oscillation detection function
	Voltage detection circuit	On-chip
Electrical Characteristics	Supply voltage	VCC = 4.2 to 5.5 V (f(BCLK) = 24 MHz)(3) (M16C/26B) VCC = 3.0 to 5.5 V (f(BCLK) = 20 MHz) (M16C/26A, M16C/26B) VCC = 2.7 to 5.5 V (f(BCLK) = 10 MHz)
	Power Consumption	20 mA (Vcc = 5 V, f(BCLK) = 24 MHz) (M16C/26B) 16 mA (Vcc = 5 V, f(BCLK) = 20 MHz) 25 μA (f(XCIN) = 32 KHz on RAM) 3 μA (Vcc = 3 V, f(XCIN) = 32 KHz, in wait mode) 0.7 μA (Vcc = 3 V, in stop mode)
Flash memory	Programming/erasure voltage	2.7 to 5.5 V
	Programming/erasure endurance	100 times (all area) or 1,000 times (block 0 to 3) / 10,000 times (block A, block B)(2)
Operating Ambient Temperature		-20 to 85°C / -40 to 85°C (2)
Package		42-pin plastic molded SSOP

NOTES:
1. IEBus is a trademark of NEC Electronics Corporation.
2. See **Tables 1.7 and 1.8 Product Code** for the program and erase endurance, and operating ambient temperature.
3. The PLL frequency synthesizer is used to run the M16C/26B at f(BCLK) = 24 MHz.

Table 4.4 SFR Information(4)(1)

Address	Register	Symbol	After reset
0340₁₆			
0341₁₆			
0342₁₆	Timer A1-1 register	TA11	XX₁₆
0343₁₆			XX₁₆
0344₁₆	Timer A2-1 register	TA21	XX₁₆
0345₁₆			XX₁₆
0346₁₆	Timer A4-1 register	TA41	XX₁₆
0347₁₆			XX₁₆
0348₁₆	Three phase PWM control register 0	INVC0	00₁₆
0349₁₆	Three phase PWM control register 1	INVC1	00₁₆
034A₁₆	Three phase output buffer register 0	IDB0	00111111₂
034B₁₆	Three phase output buffer register 1	IDB1	00111111₂
034C₁₆	Dead time timer	DTT	XX₁₆
034D₁₆	Timer B2 Interrupt occurrence frequency set counter	ICTB2	XX₁₆
034E₁₆	Position-data-retain function control register	PDRF	XXXX0000₂
034F₁₆			
0350₁₆			
0351₁₆			
0352₁₆			
0353₁₆			
0354₁₆			
0355₁₆			
0356₁₆			
0357₁₆			
0358₁₆	Port function control register	PFCR	00111111₂
0359₁₆			
035A₁₆			
035B₁₆			
035C₁₆			
035D₁₆			
035E₁₆	Interrupt request cause select register 2	IFSR2A	XXXXXXX0₂(2)
035F₁₆	Interrupt request cause select register	IFSR	00₁₆
0360₁₆			
0361₁₆			
0362₁₆			
0363₁₆			
0364₁₆			
0365₁₆			
0366₁₆			
0367₁₆			
0368₁₆			
0369₁₆			
036A₁₆			
036B₁₆			
036C₁₆			
036D₁₆			
036E₁₆			
036F₁₆			
0370₁₆			
0371₁₆			
0372₁₆			
0373₁₆			
0374₁₆	UART2 special mode register 4	U2SMR4	00₁₆
0375₁₆	UART2 special mode register 3	U2SMR3	000X0X0X₂
0376₁₆	UART2 special mode register 2	U2SMR2	X0000000₂
0377₁₆	UART2 special mode register	U2SMR	X0000000₂
0378₁₆	UART2 transmit/receive mode register	U2MR	00₁₆
0379₁₆	UART2 bit rate register	U2BRG	XX₁₆
037A₁₆	UART2 transmit buffer register	U2TB	XXXXXXXX₂
037B₁₆			XXXXXXXX₂
037C₁₆	UART2 transmit/receive control register 0	U2C0	00001000₂
037D₁₆	UART2 transmit/receive control register 1	U2C1	00000010₂
037E₁₆	UART2 receive buffer register	U2RB	XXXXXXXX₂
037F₁₆			XXXXXXXX₂

NOTE:
1. Blank spaces are reserved. No access is allowed.
2. Write "1" to bit 0 after reset.

X : Undefined

9.2 Interrupts and Interrupt Vector

One interrupt vector consists of 4 bytes. Set the start address of each interrupt routine in the respective interrupt vectors. When an interrupt request is accepted, the CPU branches to the address set in the corresponding interrupt vector. Figure 9.2.1 shows the interrupt vector.

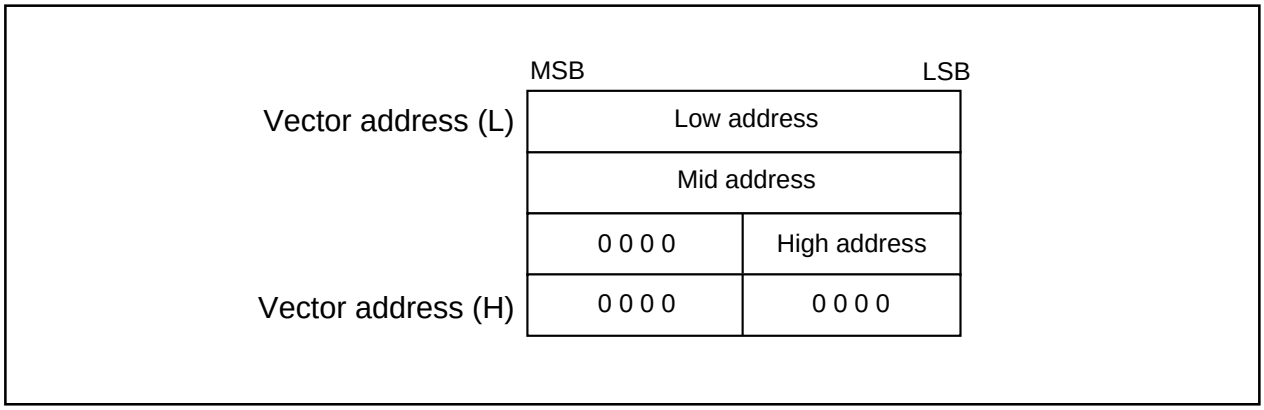


Figure 9.2.1. Interrupt Vector

9.2.1 Fixed Vector Tables

The fixed vector tables are allocated to the addresses from FFFDC16 to FFFFF16. Table 9.2.1.1 lists the fixed vector tables. In the flash memory version of microcomputer, the vector addresses (H) of fixed vectors are used by the ID code check function. For details, refer to the section **17.3 Flash Memory Rewrite Disabling Function**.

Table 9.2.1.1. Fixed Vector Tables

Interrupt source	Vector table addresses Address (L) to address (H)	Remarks	Reference
Undefined instruction	FFFDC16 to FFFDF16	Interrupt on UND instruction	M16C/60, M16C/20 serise software maual
Overflow	FFFE016 to FFFE316	Interrupt on INTO instruction	
BRK instruction	FFFE416 to FFFE716	If the contents of address FFFE716 is FF16, program execution starts from the address shown by the vector in the relocatable vector table.	
Address match	FFFE816 to FFFEB16		Address match interrupt
Single step (1)	FFFEC16 to FFFEF16		
Watchdog timer Oscillation stop and re-oscillation detection Voltage down detection	FFFF016 to FFFF316		Watchdog timer Clock generating circuit Voltage detection circuit
$\overline{\text{DBC}}$ (1)	FFFF416 to FFFF716		
$\overline{\text{NMI}}$	FFFF816 to FFFFB16		$\overline{\text{NMI}}$ interrupt
Reset (2)	FFFFC16 to FFFFF16		Reset

NOTES:

1. Do not normally use this interrupt because it is provided exclusively for use by development tools.
2. The b3 to b0 in address 0FFFFF16 are reserve bits. Set these bits to “11112”.

Watchdog Timer Control Register

b7	b6	b5	b4	b3	b2	b1	b0
	0	0					

Symbol: WDC
Address: $000F_{16}$
After Reset: $00XXXXXX_2$

Bit Symbol	Bit Name	Function	RW
(b4-b0)	High-order bit of watchdog timer		RO
(b6-b5)	Reserved bit	Set to “0”	RW
WDC7	Prescaler select bit	0: Divided by 16 1: Divided by 128	RW

Watchdog Timer Start Register

b7	b0

Symbol: WDTS
Address: $000E_{16}$
After Reset: Indeterminate

Function	RW
The watchdog timer is initialized and starts counting after a write instruction to this register. The watchdog timer value is always initialized to “7FFF $_{16}$” regardless of whatever value is written.	WO

Figure 10.2 WDC Register and WDTS Register

10.1 Count Source Protective Mode

In this mode, a on-chip oscillator clock is used for the watchdog timer count source. The watchdog timer can be kept being clocked even when CPU clock stops as a result of run-away.

Before this mode can be used, the following register settings are required:

(1) Set the PRC1 bit in the PRCR register to “1” (enable writes to PM1 and PM2 registers).

(2) Set the PM12 bit in the PM1 register to “1” (reset when the watchdog timer underflows).

(3) Set the PM22 bit in the PM2 register to “1” (on-chip oscillator clock used for the watchdog timer count source).

(4) Set the PRC1 bit in the PRCR register to “0” (disable writes to PM1 and PM2 registers).

(5) Write to the WDTS register (watchdog timer starts counting).

Setting the PM22 bit to “1” results in the following conditions

- The on-chip oscillator continues oscillating even if the CM21 bit in the CM2 register is set to "0" (main clock or PLL clock) (system clock of count source selected by the CM21 bit is valid)
- The on-chip oscillator starts oscillating, and the in-chip oscillator clock becomes the watchdog timer count source.

$$\text{Watchdog timer period} = \frac{\text{Watchdog timer count (32768)}}{\text{on-chip oscillator clock}}$$

- The CM10 bit in the CM1 register is disabled against write. (Writing a “1” has no effect, nor is stop mode entered.)
- The watchdog timer does not stop when in wait mode.

12.1.1. Timer Mode

In timer mode, the timer counts a count source generated internally (see Table 12.1.1.1). Figure 1.2.1.1.1 shows TAiMR register in timer mode.

Table 12.1.1.1. Specifications in Timer Mode

Item	Specification
Count source	f_1, f_2, f_8, f_{32}, f_{C32}
Count operation	• Down-count • When the timer underflows, it reloads the reload register contents and continues counting
Divide ratio	1/(n+1) n: set value of TAi register (i= 0 to 4) 0000_{16} to $FFFF_{16}$
Count start condition	Set TAiS bit in the TABSR register to “1” (= start counting)
Count stop condition	Set TAiS bit to “0” (= stop counting)
Interrupt request generation timing	Timer underflow
TAiIN pin function	I/O port or gate input
TAiOUT pin function	I/O port or pulse output
Read from timer	Count value can be read by reading TAi register
Write to timer	• When not counting and until the 1st count source is input after counting start Value written to TAi register is written to both reload register and counter • When counting (after 1st count source input) Value written to TAi register is written to only reload register (Transferred to counter when reloaded next)
Select function	• Gate function Counting can be started and stopped by an input signal to TAiIN pin • Pulse output function Whenever the timer underflows, the output polarity of TAiOUT pin is inverted. When not counting, the pin outputs a low.

Timer Ai mode register (i=0 to 4)

b7	b6	b5	b4	b3	b2	b1	b0
		0				0	0

Symbol	Address	After reset
TA0MR to TA4MR	0396_{16} to $039A_{16}$	00_{16}

Bit symbol	Bit name	Function	RW
TMOD0	Operation mode select bit	b1 b0 0 0 : Timer mode	RW
TMOD1			RW
MR0	Pulse output function select bit	0 : Pulse is not output (TAiOUT pin is a normal port pin) 1 : Pulse is output (TAiOUT pin is a pulse output pin)	RW
MR1	Gate function select bit	b4 b3 0 0 : 0 1 : } Gate function not available (TAiIN pin functions as I/O port) 1 0 : Counts while input on the TAiIN pin is low (1) 1 1 : Counts while input on the TAiIN pin is high (1)	RW
MR2			RW
MR3	Must be set to “0” in timer mode		RW
TCK0	Count source select bit	b7 b6 0 0 : f_1 or f_2 0 1 : f_8 1 0 : f_{32} 1 1 : f_{C32}	RW
TCK1			RW

NOTE:
1.The port direction bit for the TAiIN pin must be set to “0” (= input mode).

Figure 12.1.1.1. Timer Ai Mode Register in Timer Mode

12.1.2. Event Counter Mode

In event counter mode, the timer counts pulses from an external device or overflows and underflows of other timers. Timers A2, A3 and A4 can count two-phase external signals. Table 12.1.2.1 lists specifications in event counter mode (when not processing two-phase pulse signal). Table 12.1.2.2 lists specifications in event counter mode (when processing two-phase pulse signal with the timers A2, A3 and A4). Figure 12.1.2.1 shows TAiMR register in event counter mode (when not processing two-phase pulse signal). Figure 12.1.2.2 shows TA2MR to TA4MR registers in event counter mode (when processing two-phase pulse signal with the timers A2, A3 and A4).

Table 12.1.2.1. Specifications in Event Counter Mode (when not processing two-phase pulse signal)

Item	Specification
Count source	• External signals input to TAiIN pin (i=0 to 4) (effective edge can be selected in program) • Timer B2 overflows or underflows, timer Aj (j=i-1, except j=4 if i=0) overflows or underflows, timer Ak (k=i+1, except k=0 if i=4) overflows or underflows
Count operation	• Up-count or down-count can be selected by external signal or program • When the timer overflows or underflows, it reloads the reload register contents and continues counting. When operating in free-running mode, the timer continues counting without reloading.
Divided ratio	1/ ($FFFF_{16}$ - n + 1) for up-count 1/ (n + 1) for down-count n : set value of TAi register 0000_{16} to $FFFF_{16}$
Count start condition	Set TAiS bit in the TABSR register to “1” (= start counting)
Count stop condition	Set TAiS bit to “0” (= stop counting)
Interrupt request generation timing	Timer overflow or underflow
TAiIN pin function	I/O port or count source input
TAiOUT pin function	I/O port, pulse output, or up/down-count select input
Read from timer	Count value can be read by reading TAi register
Write to timer	• When not counting and until the 1st count source is input after counting start Value written to TAi register is written to both reload register and counter • When counting (after 1st count source input) Value written to TAi register is written to only reload register (Transferred to counter when reloaded next)
Select function	• Free-run count function Even when the timer overflows or underflows, the reload register content is not reloaded to it • Pulse output function Whenever the timer underflows or underflows, the output polarity of TAiOUT pin is inverted . When not counting, the pin outputs a low.

12.2.1 Timer Mode

In timer mode, the timer counts a count source generated internally (see Table 12.2.1.1). Figure 12.2.1.1 shows TBiMR register in timer mode.

Table 12.2.1.1 Specifications in Timer Mode

Item	Specification
Count source	f_1, f_2, f_8, f_{32}, f_{C32}
Count operation	• Down-count • When the timer underflows, it reloads the reload register contents and continues counting
Divide ratio	1/(n+1) n: set value of TBi register (i= 0 to 2) 0000_{16} to $FFFF_{16}$
Count start condition	Set TBiS bit(1) to “1” (= start counting)
Count stop condition	Set TBiS bit to “0” (= stop counting)
Interrupt request generation timing	Timer underflow
TBiIN pin function	I/O port
Read from timer	Count value can be read by reading TBi register
Write to timer	• When not counting and until the 1st count source is input after counting start Value written to TBi register is written to both reload register and counter • When counting (after 1st count source input) Value written to TBi register is written to only reload register (Transferred to counter when reloaded next)

NOTE:

1. The TB0S to TB2S bits are assigned to the bit 5 to bit 7 in the TABSR register.

Timer Bi mode register (i= 0 to 2)

b7	b6	b5	b4	b3	b2	b1	b0
						0	0

Symbol: TB0MR to TB2MR — Address: $039B_{16}$ to $039D_{16}$ — After reset: $00XX0000_2$

Bit symbol	Bit name	Function	RW
TMOD0	Operation mode select bit	b1 b0 0 0 : Timer mode or A/D trigger mode	RW
TMOD1			RW
MR0	Has no effect in timer mode Can be set to “0” or “1”		RW
MR1			RW
MR2	TB0MR register Must be set to “0” in timer mode		RW
	TB1MR, TB2MR registers Nothing is assigned. When write, set to “0”. When read, its content is indeterminate		—
MR3	When write in timer mode, set to “0”. When read in timer mode, its content is indeterminate.		RO
TCK0	Count source select bit	b7 b6 0 0 : f_1 or f_2 0 1 : f_8 1 0 : f_{32} 1 1 : f_{C32}	RW
TCK1			RW

Figure 12.2.1.1 TBiMR Register in Timer Mode

Timer Ai mode register

b7	b6	b5	b4	b3	b2	b1	b0
		0	1		0	1	0

Symbol	Address	After reset
TA1MR	039716	0016
TA2MR	039816	0016
TA4MR	$039A16$	0016

Bit symbol	Bit name	Function	RW
TMOD0	Operation mode select bit	Must set to "10_2" (one-shot timer mode) for the three-phase motor control timer function	RW
TMOD1			RW
MR0	Pulse output function select bit	Must set to "0" for the three-phase motor control timer function	—
MR1	External trigger select bit	Has no effect for the three-phase motor control timer function	RW
MR2	Trigger select bit	Must set to "1" (selected by event/trigger select register) for the three-phase motor control timer function	RW
MR3	Must set to "0" for the three-phase motor control timer function		RW
TCK0	Count source select bit	b7 b6 0 0 : f_1 or f_2 0 1 : f_8 1 0 : f_{32} 1 1 : fC_{32}	RW
TCK1			RW

Timer B2 mode register

b7	b6	b5	b4	b3	b2	b1	b0
			0			0	0

Symbol	Address	After reset
TB2MR	$039D16$	$00XX0000_2$

Bit symbol	Bit name	Function	RW
TMOD0	Operation mode select bit	Set to "00_2" (timer mode) for the three-phase motor control timer function	RW
TMOD1			RW
MR0	Has no effect for the three-phase motor control timer function. When write, set to "0". When read, its content is indeterminate.		RW
MR1			RW
MR2	Must set to "0" for the three-phase motor control timer function		RW
MR3	When write in three-phase motor control timer function, write "0". When read, its content is indeterminate.		RO
TCK0	Count source select bit	b7 b6 0 0 : f_1 or f_2 0 1 : f_8 1 0 : f_{32} 1 1 : fC_{32}	RW
TCK1			RW

Figure 12.3.8. TA1MR, TA2MR, TA4MR, and TB2MR Registers

UARTi transmit/receive mode register (i = 0, 1)

b7	b6	b5	b4	b3	b2	b1	b0

Symbol	Address	After reset
U0MR, U1MR	$03A0_{16}$, $03A8_{16}$	00_{16}

Bit symbol	Bit name	Function	RW
SMD0	Serial I/O mode select bit (2)	b2 b1 b0 0 0 0 : Serial I/O disabled 0 0 1 : Clock synchronous serial I/O mode 1 0 0 : UART mode transfer data 7 bits long 1 0 1 : UART mode transfer data 8 bits long 1 1 0 : UART mode transfer data 9 bits long Do not set value other than the above	RW
SMD1			RW
SMD2			RW
CKDIR	Internal/external clock select bit	0 : Internal clock 1 : External clock (1)	RW
STPS	Stop bit length select bit	0 : One stop bit 1 : Two stop bits	RW
PRY	Odd/even parity select bit	Effective when PRYE = 1 0 : Odd parity 1 : Even parity	RW
PRYE	Parity enable bit	0 : Parity disabled 1 : Parity enabled	RW
$\overline{\text{(b7)}}$	Reserve bit	Write to "0"	RW

NOTES:
1. Set the corresponding port direction bit for each CLKi pin to “0” (input mode).
2. To receive data, set the corresponding port direction bit for each RxDi pin to “0” (input mode).

UART2 transmit/receive mode register

b7	b6	b5	b4	b3	b2	b1	b0

Symbol	Address	After reset
U2MR	0378_{16}	00_{16}

Bit symbol	Bit name	Function	RW
SMD0	Serial I/O mode select bit (2)	b2 b1 b0 0 0 0 : Serial I/O disabled 0 0 1 : Clock synchronous serial I/O mode 0 1 0 : I^2C bus mode (3) 1 0 0 : UART mode transfer data 7 bits long 1 0 1 : UART mode transfer data 8 bits long 1 1 0 : UART mode transfer data 9 bits long Must not be set except above	RW
SMD1			RW
SMD2			RW
CKDIR	Internal/external clock select bit	0 : Internal clock 1 : External clock (1)	RW
STPS	Stop bit length select bit	0 : One stop bit 1 : Two stop bits	RW
PRY	Odd/even parity select bit	Effective when PRYE = 1 0 : Odd parity 1 : Even parity	RW
PRYE	Parity enable bit	0 : Parity disabled 1 : Parity enabled	RW
IOPOL	TxD, RxD I/O polarity reverse bit	0 : No reverse 1 : Reverse	RW

NOTES:
1. Set the corresponding port direction bit for each CLK2 pin to “0” (input mode).
2. To receive data, set the corresponding port direction bit for each RxD2 pin to “0” (input mode).
3. Set the corresponding port direction bit for SCL2 and SDA2 pins to “0” (input mode).

Figure 13.1.5. U0MR to U2MR registers

Table 13.1.2.3 lists the functions of the input/output pins during UART mode. Table 13.1.2.4 lists the $P6_4$ pin functions during UART mode. Note that for a period from when the UARTi operation mode is selected to when transfer starts, the TxDi pin outputs an “H”. (If the N-channel open-drain output is selected, this pin is in a high-impedance state.)

Table 13.1.2.3. I/O Pin Functions in UART mode(1)

Pin name	Function	Method of selection
TxDi (i = 0 to 2) ($P6_3$, $P6_7$, $P7_0$)	Serial data output	(Outputs "H" when performing reception only)
RxDi ($P6_2$, $P6_6$, $P7_1$)	Serial data input	PD6_2 bit, PD6_6 bit in the PD6 register and the PD7_1 bit in the PD7 register (Can be used as an input port when performing transmission only)
CLKi ($P6_1$, $P6_5$, $P7_2$)	Input/output port	Set the CKDIR bit in the UiMR register to "0"
	Transfer clock input	Set the CKDIR bit in the UiMR register to "1" Set the PD6_1 bit and PD6_5 bit in the PD6 register to "0", PD7_2 bit in the PD7 register to "0"
$\overline{CTS}i/\overline{RTS}i$ ($P6_0$, $P6_4$, $P7_3$)	$\overline{CTS}$ input	Set the CRD bit in the UiC0 register to "0" Set the CRS bit in the UiC0 register to "0" Set the PD6_0 bit and PD6_4 bit in the PD6 register to "0", the PD7_3 bit in the PD7 register "0"
	$\overline{RTS}$ output	Set the CRD bit in the UiC0 register to "0" Set the CRS bit in the UiC0 register to "1"
	Input/output port	Set the CRD bit in the UiC0 register "1"

NOTE:
1. When the U1MAP bit in PACR register is set to “1” ($P7_3$ to $P7_0$), UART1 pin is assgined to $P7_3$ to $P7_0$.

Table 13.1.2.4. $P6_4$ Pin Functions in UART mode(1)

Pin function	Bit set value				
	U1C0 register		UCON register		PD6 register
	CRD	CRS	RCSP	CLKMD1	PD6_4
$P6_4$	1	—	0	0	Input: 0, Output: 1
$\overline{CTS}_1$	0	0	0	0	0
$\overline{RTS}_1$	0	1	0	0	—
$\overline{CTS}_0$ (2)	0	0	1	0	0

NOTES:
1. When the U1MAP bit in PACR register is “1” ($P7_3$ to $P7_0$), this table lists the $P7_0$ functions.
2. In addition to this, set the CRD bit in the U0C0 register to “0” ($\overline{CTS}_0/\overline{RTS}_0$ enabled) and the CRS bit in the U0C0 register to “1” ($\overline{RTS}_0$ selected).

13.1.4.1 Clock Phase Setting Function

One of four combinations of transfer clock phases and polarities can be selected using the CKPH bit in the U2SMR3 register and the CKPOL bit in the U2C0 register.

Make sure the transfer clock polarity and phase are the same for the master and slave to communicate.

13.1.4.1.1 Master (Internal Clock)

Figure 13.1.4.1.1.1 shows the transmission and reception timing in master (internal clock).

13.1.4.1.2 Slave (External Clock)

Figure 13.1.4.1.2.1 shows the transmission and reception timing (CKPH=0) in slave (external clock) while Figure 13.1.4.1.2.2 shows the transmission and reception timing (CKPH=1) in slave (external clock).

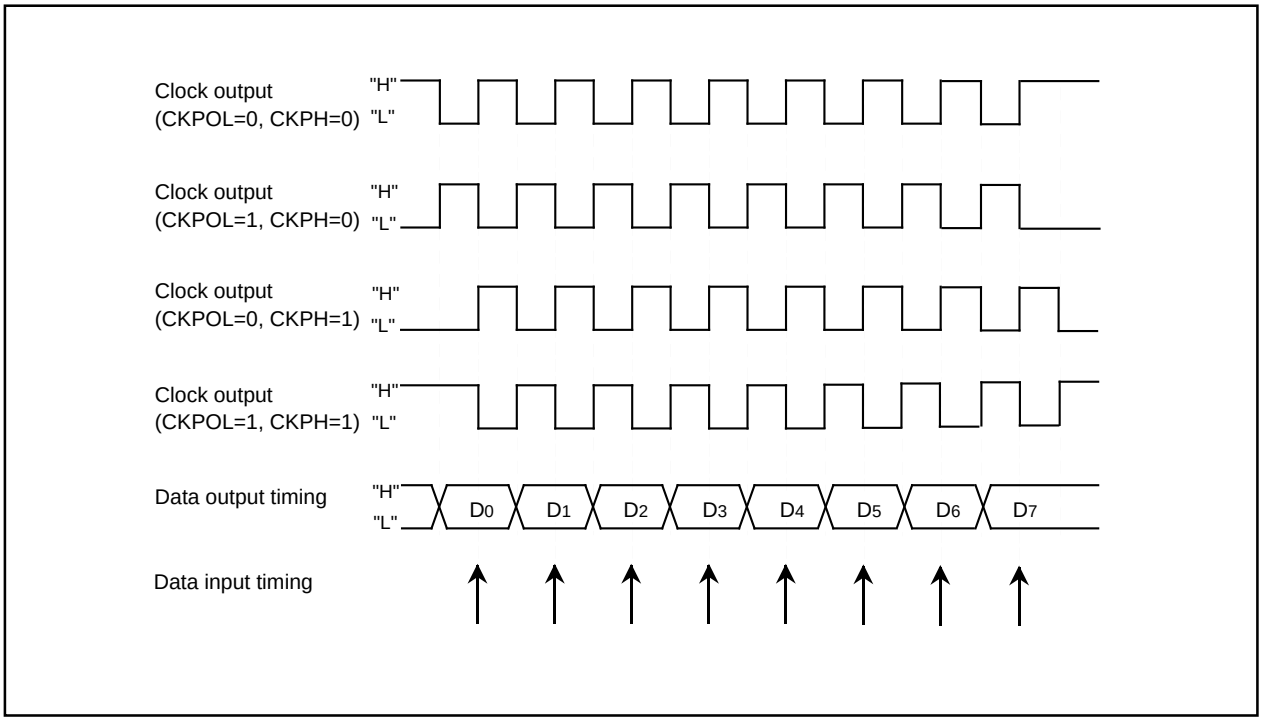


Figure 13.1.4.1.1.1. Transmission and Reception Timing in Master Mode (Internal Clock)

14.1.5 Repeat Sweep Mode 1

In repeat sweep mode 1, analog voltages applied to the all selected pins are converted to a digital code, with mainly used in the selected pins. Table 14.1.5.1 shows the repeat sweep mode 1 specifications. Figure 14.1.5.1 shows the operation example in repeat sweep mode 1. Figure 14.1.5.2 shows the ADCON0 to ADCON2 registers in repeat sweep mode 1.

Table 14.1.5.1 Repeat Sweep Mode 1 Specifications

Item	Specification
Function	The SCAN1 to SCAN0 bits in the ADCON1 register and the ADGSEL1 to ADGSEL0 bits in the ADCON2 register mainly select pins. Analog voltage applied to the all selected pins is repeatedly converted to a digital code Example : When selecting AN_0 Analog voltage is converted to a digital code in the following order $AN_0 \rightarrow AN_1 \rightarrow AN_0 \rightarrow AN_2 \rightarrow AN_0 \rightarrow AN_3$, and so on.
A/D Conversion Start Condition	• When the TRG bit in the ADCON0 register is “0” (software trigger) Set the ADST bit in the ADCON0 register to “1” (A/D conversion started) • When the TRG bit in the ADCON0 register is “1” (hardware trigger) The $\overline{ADTRG}$ pin input changes state from “H” to “L” after setting the ADST bit to “1” (A/D conversion started)
A/D Conversion Stop Condition	Set the ADST bit to “0” (A/D conversion halted)
Interrupt Request Generation Timing	None generated
Analog Input Pins Mainly Used in A/D Conversions	Select from AN_0 (1 pins), AN_0 to AN_1 (2 pins), AN_0 to AN_2 (3 pins), AN_0 to AN_3 (4 pins) (1)
Readout of A/D Conversion Result	Readout one of the AD0 to AD7 registers that corresponds to the selected pin

NOTE:

1. AN_{30} to AN_{32} can be used in the same way as AN_0 to AN_7. However, all input pins need to belong to the same group.

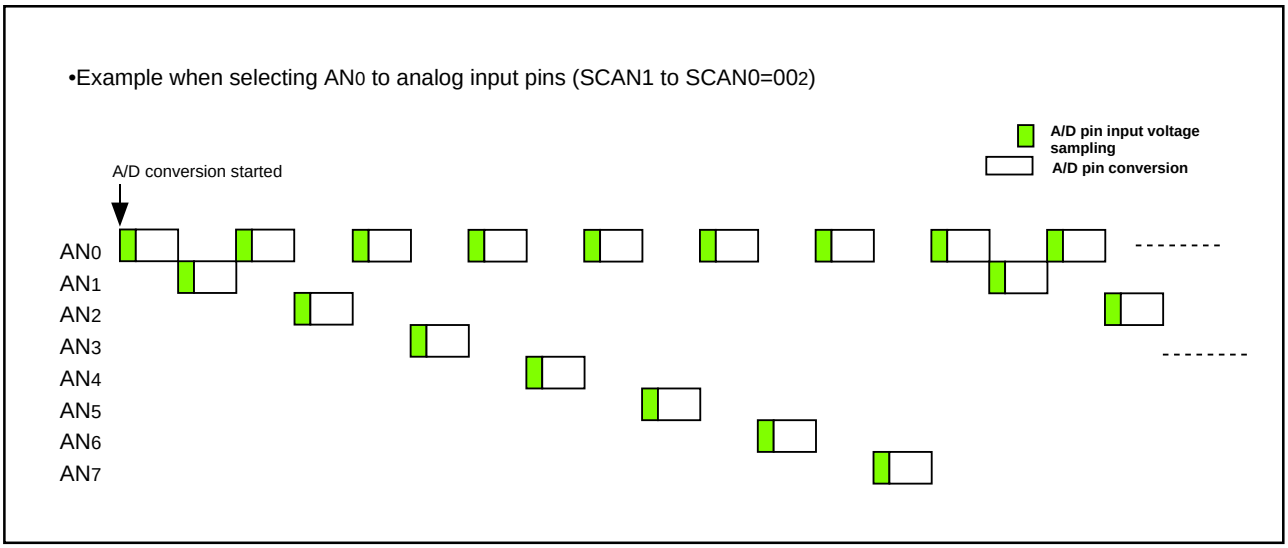


Figure 14.1.5.1 Operation Example in Repeat Sweep Mode 1

16. Programmable I/O Ports

Note

$P6_0$ to $P6_3$, $P9_2$ and $P9_3$ are not available in the 42-pin package.

The programmable input/output ports (hereafter referred to simply as “I/O ports”) consist of 39 lines $P1_5$ to $P1_7$, P6, P7, P8, $P9_0$ to $P9_3$, P10 for the 48-pin package, or 33 lines $P1_5$ to $P1_7$, $P6_4$ to $P6_7$, P7, P8, $P9_0$ to $P9_1$, P10 for the 42-pin package. Each port can be set for input or output every line by using a direction register, and can also be chosen to be or not be pulled high in sets of 4 lines.

Figures 16.1 to 16.4 show the I/O ports. Figure 16.5 shows the I/O pins.

Each pin functions as an I/O port, a peripheral function input/output.

For details on how to set peripheral functions, refer to each functional description in this manual. If any pin is used as a peripheral function input, set the direction bit for that pin to “0” (input mode). Any pin used as an output pin for peripheral functions is directed for output no matter how the corresponding direction bit is set.

16.1 Port Pi Direction Register (PDi Register, i = 1, 6 to 10)

Figure 16.1.1 shows the direction registers.

This register selects whether the I/O port is to be used for input or output. The bits in this register correspond one for one to each port.

16.2 Port Pi Register (Pi Register, i = 1, 6 to 10)

Figure 16.2.1 shows the Pi registers.

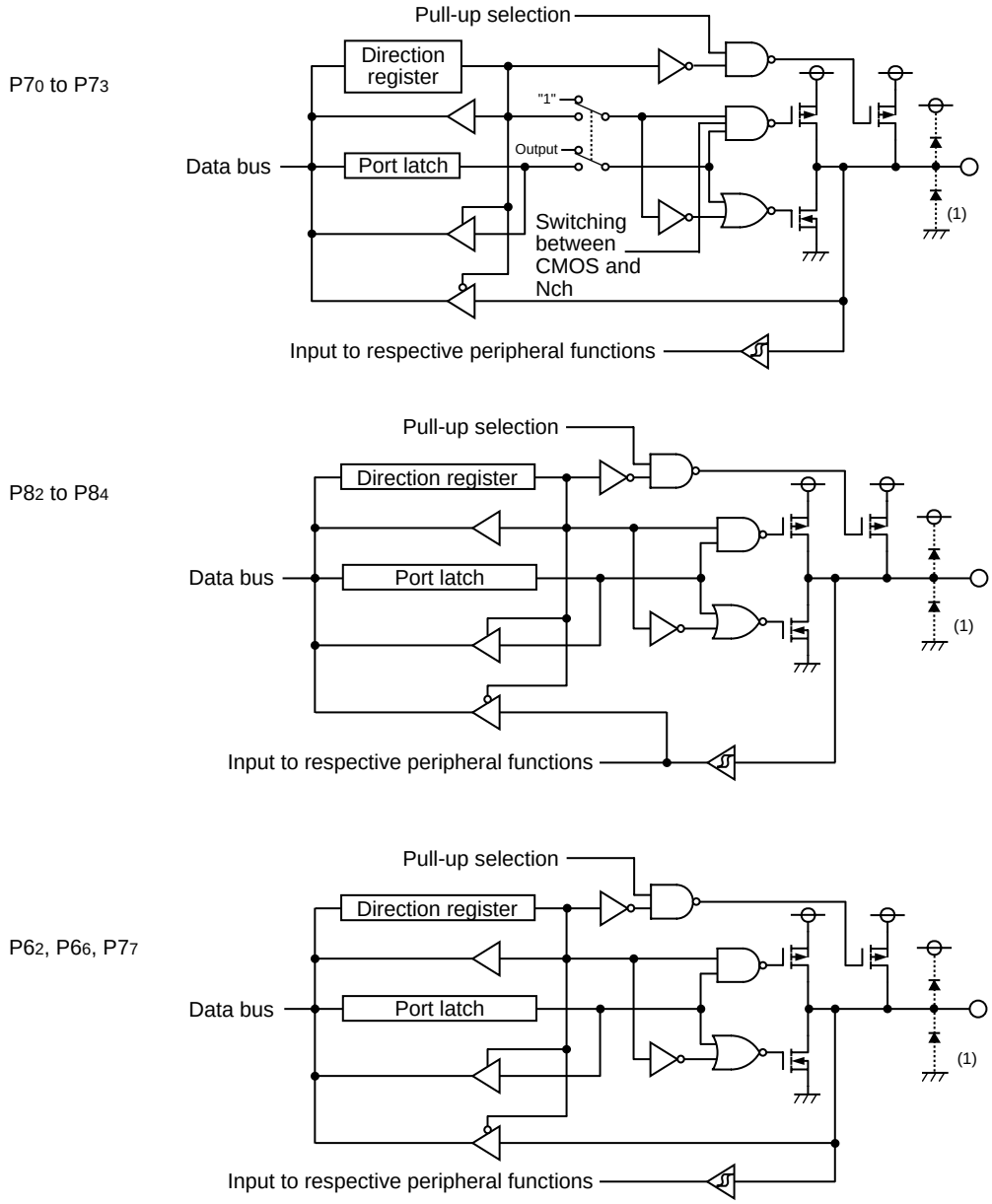
Data input/output to and from external devices are accomplished by reading and writing to the Pi register. The Pi register consists of a port latch to hold the output data and a circuit to read the pin status. For ports set for input mode, the input level of the pin can be read by reading the corresponding Pi register, and data can be written to the port latch by writing to the Pi register.

For ports set for output mode, the port latch can be read by reading the corresponding Pi register, and data can be written to the port latch by writing to the Pi register. The data written to the port latch is output from the pin. The bits in the Pi register correspond one for one to each port.

16.3 Pull-up Control Register 0 to Pull-up Control Register 2 (PUR0 to PUR2 Registers)

Figure 16.3.1 shows the PUR0 to PUR2 registers.

The PUR0 to PUR2 registers select whether the ports, divided into groups of four ports, are pulled up or not. The ports, selected by setting the bits in registers PUR2 to PUR0 to “1” (pull-up), are pulled up when the direction registers are set to “0” (input mode). The ports are pulled up regardless of their function.



NOTE:
1. ·····⧓····· symbolizes a parasitic diode.
Make sure the input voltage on each port will not exceed Vcc.

Figure 16.2. I/O Ports (2)

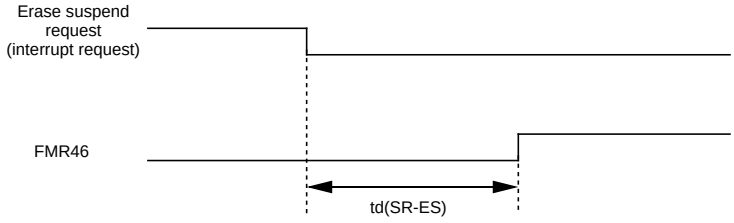
Table 18.4. Flash Memory Version Electrical Characteristic (1): Program Space and Data Space for U3 and U5, Program Space for U7 and U9

Symbol	Parameter		Standard			Unit
			Min.	Typ.(2)	Max.	
-	Program and Erase Endurance(3)		100/1000(4, 11)			cycles
-	Word Program Time (Vcc=5.0V, Topr=25° C)			75	600	µs
-	Block Erase Time (Vcc=5.0V, Topr=25° C)	2-Kbyte Block		0.2	9	s
		8-Kbyte Block		0.4	9	s
		16-Kbyte Block		0.7	9	s
		32-Kbyte Block		1.2	9	s
td(SR-ES)	Duration between Suspend Request and Erase Suspend				8	ms
tPS	Wait Time to Stabilize Flash Memory Circuit				15	µs
-	Data Hold Time (5)		20			years

Table 18.5. Flash Memory Version Electrical Characteristics (6): Data Space for U7 and U9 (7)

Symbol	Parameter	Standard			Unit
		Min.	Typ.(2)	Max.	
-	Program and Erase Endurance(3, 8, 9)	10000(4, 10)			cycles
-	Word Program Time (Vcc=5.0V, Topr=25° C)		100		µs
-	Block Erase Time (Vcc=5.0V, Topr=25° C) (2-Kbyte block)		0.3		s
td(SR-ES)	Duration between Suspend Request and Erase Suspend			8	ms
tPS	Wait Time to Stabilize Flash Memory Circuit			15	µs
-	Data Hold Time (5)	20			years

NOTES:
1. Referenced to Vcc = 2.7 to 5.5 V at Topr = 0 to 60° C (program space), -40 to 85° C (data space), unless otherwise specified.
2. Vcc = 5.0 V; Topr = 25° C
3. Program and erase endurance is defined as number of program-erase cycles per block.
   If program and erase endurance is *n* cycle (*n* = 100, 1000, 10000), each block can be erased and programmed *n* cycles.
   For example, if a 2-Kbyte block A is erased after programming one-word data to each address 1,024 times, this counts as one program and erase endurance. Data cannot be programmed to the same address more than once without erasing the block. (rewrite prohibited).
4. Number of E/W cycles for which operation is guranteed (1 to minimum value are guaranteed).
5. Topr = 55° C
6. Referenced to Vcc = 2.7 to 5.5 V at Topr = -40 to 85° C (U7) / -20 to 85° C (U9) unless otherwise specified.
7. Table 18.5 applies for data space in U7 and U9 when program and erase endurance is more than 1,000 cycles. Otherwise, use Table 18.4.
8. To reduce the number of program and erase endurance when working with systems requiring numerous rewrites, write to unused word addresses within the block instead of rewrite. Erase block only after all possible addresses are used. For example, an 8-word program can be written 128 times maximum before erase becomes necessary. Maintaining an equal number of times erasure between block A and block B will also improve efficiency. It is recommended to track the total number of erasure performed per block and to limit the number of erasure.
9. Execute the clear status register command and block erase command at least 3 times until an erase error is not generated when an erase error is generated.
10. When executing more than 100 times rewrites, set one wait state per block access by setting the FMR17 bit in the FMR1 register 1 to "1" (wait state). When accessing to all other blocks and internal RAM, wait state can be set by the PM17 bit, regardless of the FMR17 bit setting value.
11. The program and erase endurance is 100 cycles for program space and data space in U3 and U5; 1,000 cycles for program space in U7 and U9.
12. Customers desiring E/W failure rate information should contact their Renesas technical support representative.



V_{CC} = 5V

Timing Requirements

(V_{CC} = 5V, V_{SS} = 0V, at Topr = – 20 to 85°C / – 40 to 85°C unless otherwise specified)

Table 18.17. Timer B Input (Counter Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time (counted on one edge)	100		ns
$t_{w(TBH)}$	TBiIN input HIGH pulse width (counted on one edge)	40		ns
$t_{w(TBL)}$	TBiIN input LOW pulse width (counted on one edge)	40		ns
$t_{c(TB)}$	TBiIN input cycle time (counted on both edges)	200		ns
$t_{w(TBH)}$	TBiIN input HIGH pulse width (counted on both edges)	80		ns
$t_{w(TBL)}$	TBiIN input LOW pulse width (counted on both edges)	80		ns

Table 18.18. Timer B Input (Pulse Period Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time	400		ns
$t_{w(TBH)}$	TBiIN input HIGH pulse width	200		ns
$t_{w(TBL)}$	TBiIN input LOW pulse width	200		ns

Table 18.19. Timer B Input (Pulse Width Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time	400		ns
$t_{w(TBH)}$	TBiIN input HIGH pulse width	200		ns
$t_{w(TBL)}$	TBiIN input LOW pulse width	200		ns

Table 18.20. A/D Trigger Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(AD)}$	$\overline{ADTRG}$ input cycle time (trigger able minimum)	1000		ns
$t_{w(ADL)}$	$\overline{ADTRG}$ input LOW pulse width	125		ns

Table 18.21. Serial I/O

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	200		ns
$t_{w(CKH)}$	CLKi input HIGH pulse width	100		ns
$t_{w(CKL)}$	CLKi input LOW pulse width	100		ns
$t_{d(C-Q)}$	TxDi output delay time		80	ns
$t_{h(C-Q)}$	TxDi hold time	0		ns
$t_{su(D-C)}$	RxDi input setup time	70		ns
$t_{h(C-D)}$	RxDi input hold time	90		ns

Table 18.22. External Interrupt $\overline{INTi}$ Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INTi}$ input HIGH pulse width	250		ns
$t_{w(INL)}$	$\overline{INTi}$ input LOW pulse width	250		ns

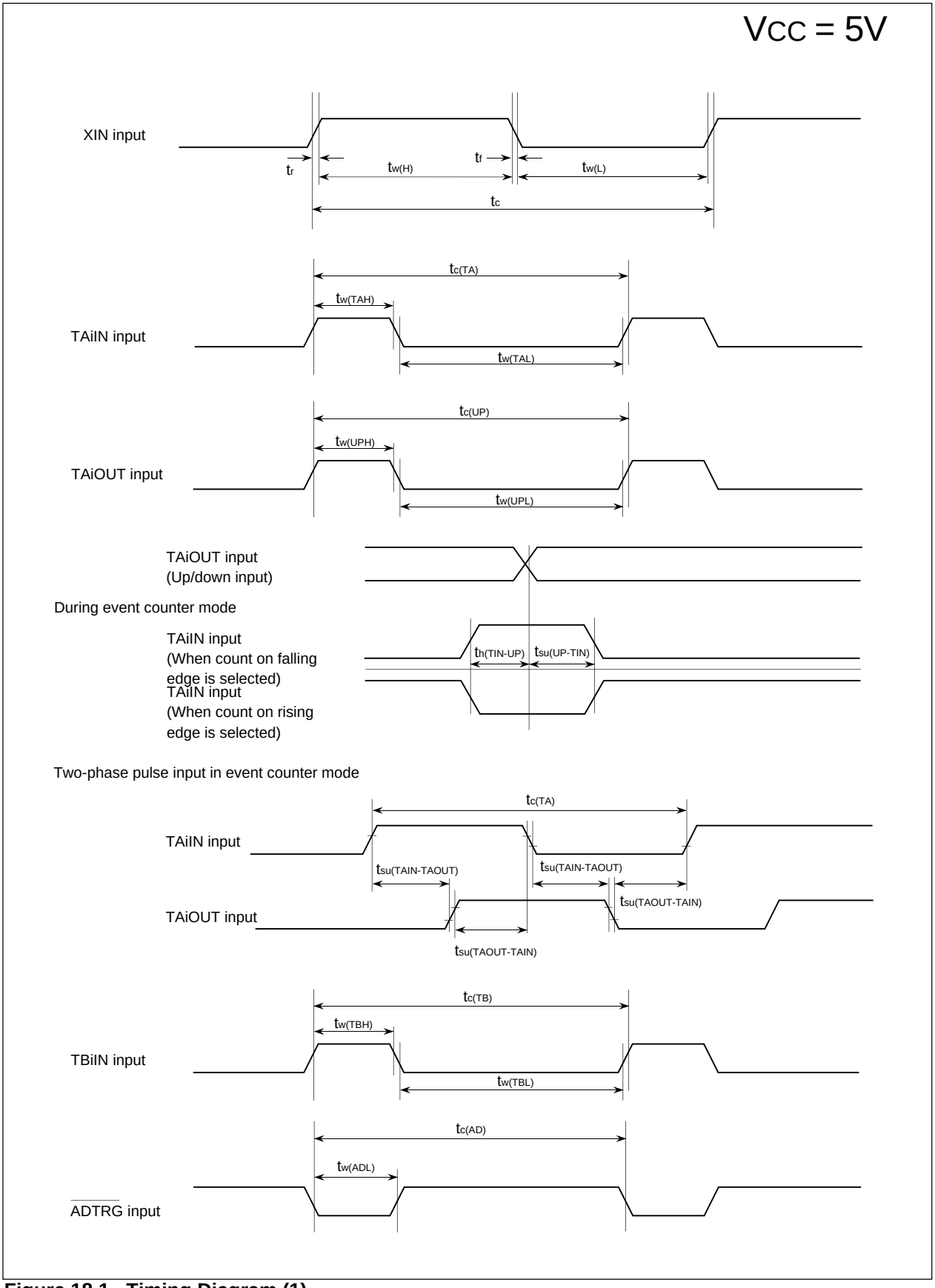


Figure 18.1. Timing Diagram (1)

18.2. M16C/26T (T version)

Table 18.38. Absolute Maximum Ratings

Symbol	Parameter			Condition	Value	Unit
V_{CC}	Supply Voltage			V_{CC} = AV_{CC}	-0.3 to 6.5	V
AV_{CC}	Analog Supply Voltage			V_{CC} = AV_{CC}	-0.3 to 6.5	V
V_I	Input Voltage	$P1_5$ to $P1_7$, $P6_0$ to $P6_7$, $P7_0$ to $P7_7$, $P8_0$ to $P8_7$, $P9_0$ to $P9_3$, $P10_0$ to $P10_7$, X_{IN}, V_{REF}, $\overline{RESET}$, CNV_{SS}			-0.3 to V_{CC}+0.3	V
V_O	Output Voltage	$P1_5$ to $P1_7$, $P6_0$ to $P6_7$, $P7_0$ to $P7_7$, $P8_0$ to $P8_7$, $P9_0$ to $P9_3$, $P10_0$ to $P10_7$, X_{OUT}			-0.3 to V_{CC}+0.3	V
Pd	Power Dissipation			-40 ≤ Topr ≤ 85° C	300	mW
Topr	Operating Ambient Temperature	during CPU operation			-40 to 85	° C
		during flash memory program and erase operation	Program Space (Block 0 to Block 3)		0 to 60	° C
			Data Space (Block A, Block B)		-40 to 85	° C
Tstg	Storage Temperature				-65 to 150	° C

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