Renesas Electronics America Inc - UPD78F9222MC-5A4-A Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	78K0S
Core Size	8-Bit
Speed	10MHz
Connectivity	LINbus, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	15
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-LSSOP (0.240", 6.10mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f9222mc-5a4-a

INTRODUCTION

Target Readers

This manual is intended for user engineers who wish to understand the functions of the 78K0S/KA1+ in order to design and develop its application systems and programs.

The target devices are the following subseries products.

<R>
- 78K0S/KA1+: μPD78F9221, 78F9222, 78F9224, 78F9221(A), 78F9222(A), 78F9221(A2), 78F9222(A2)

Purpose

This manual is intended to give users on understanding of the functions described in the **Organization** below.

Organization

Two manuals are available for the 78K0S/KA1+: this manual and the Instruction Manual (common to the 78K/0S Series).

78K0S/KA1+ User's Manual	78K/0S Series Instructions User's Manual
• Pin functions • Internal block functions • Interrupts • Other internal peripheral functions • Electrical specifications	• CPU function • Instruction set • Instruction description

How to Use This Manual

It is assumed that the readers of this manual have general knowledge of electrical engineering, logic circuits, and microcontrollers.

◊ To understand the overall functions of 78K0S/KA1+
  → Read this manual in the order of the **CONTENTS**. The mark <R> shows major revised points. The revised points can be easily searched by copying an "<R>" in the PDF file and specifying it in the "Find what:" field.

◊ How to read register formats
  → For a bit number enclosed in a square, the bit name is defined as a reserved word in the RA78K0S, and is defined as an sfr variable using the #pragma sfr directive in the CC78K0S.

◊ To learn the detailed functions of a register whose register name is known
  → See **APPENDIX C REGISTER INDEX**.

◊ To learn the details of the instruction functions of the 78K/0S Series
  → Refer to **78K/0S Series Instructions User's Manual (U11047E)** separately available.

◊ To learn the electrical specifications of the 78K0S/KA1+
  → See **CHAPTER 21** and **22 ELECTRICAL SPECIFICATIONS**.

1.2 Ordering Information

Part Number

μPD78F9 ××× - ×× (×) - ××× -×

	Semiconductor component	
-A	Lead-free	Product contains no lead in any area (Terminal finish is Sn/Bi plating)
-AX		Product contains no lead in any area (Terminal finish is Ni/Pd/Au plating)

	Quality Grades
Blank	Standard
(A)	Special
(A2)	

	Package type
MC-5A4	Plastic SSOP
MC-CAA	
CS-CAC	Plastic SDIP

	Number of pins	High-speed RAM	Flash memory
221	20 pins	128 bytes	2 K bytes
222	20 pins	256 bytes	4 K bytes
224	20 pins	256 bytes	8 K bytes

<R>

	Product type
F	Flash memory versions

Please refer to "Quality Grades on NEC Semiconductor Devices" (Document No. C11531E) published by NEC Electronics Corporation to know the specification of the quality grade on the device and its recommended applications.

[Part number list]

<R>

μPD78F9221MC-5A4-A	μPD78F9222MC-5A4-A	μPD78F9224MC-5A4-A
μPD78F9221MC(A)-5A4-A	μPD78F9222MC(A)-5A4-A	
μPD78F9221MC(A2)-5A4-A	μPD78F9222MC(A2)-5A4-A	
μPD78F9221MC(A)-CAA-AX	μPD78F9222MC(A)-CAA-AX	
μPD78F9221MC(A2)-CAA-AX	μPD78F9222MC(A2)-CAA-AX	
μPD78F9221CS-CAC-A	μPD78F9222CS-CAC-A	

2.2.7 X1 and X2

These pins connect an oscillator to oscillate the X1 input clock.

X1 and X2 also function as the P121 and P122, respectively. For the setting method for pin functions, see **CHAPTER 17 OPTION BYTE**.

Supply an external clock to X1.

Caution The P121/X1 and P122/X2 pins are pulled down during reset.

2.2.8 AV_{REF}

This is the A/D converter reference voltage input pin and the positive power supply pin of P20 to P23 and A/D converter. When the A/D converter is not used, connect this pin to V_{DD}.

2.2.9 V_{DD}

This is the positive power supply pin.

2.2.10 V_{SS}

This is the ground pin.

In the 78K0S/KA1+, V_{SS} functions alternately as the ground potential of the A/D converter. Be sure to connect V_{SS} to a stabilized GND (= 0 V).

2.3 Pin I/O Circuits and Connection of Unused Pins

Table 2-1 shows I/O circuit type of each pin and the connections of unused pins.

For the configuration of the I/O circuit of each type, refer to **Figure 2-1**.

Table 2-1. Types of Pin I/O Circuits and Connection of Unused Pins

Pin Name	I/O Circuit Type	I/O	Recommended Connection of Unused Pin
P20/ANI0 to P23/ANI3	11	I/O	Input: Independently connect to AV_{REF} or V_{SS} via a resistor. Output: Leave open.
P30/TI000/INTP0	8-A		Input: Independently connect to V_{DD} or V_{SS} via a resistor. Output: Leave open.
P31/TI010/TO00/INTP2			
P34/$\overline{\text{RESET}}$	2	Input	Connect to V_{DD} via a resistor.
P40	8-A	I/O	Input: Independently connect to V_{DD} or V_{SS} via a resistor. Output: Leave open.
P41/INTP3			
P42/TOH1			
P43/TxD6/INTP1			
P44/RxD6			
P45			
P121/X1	16-B		Input: Independently connect to V_{SS} via a resistor. Output: Leave open.
P122/X2			
P123	8-A		Input: Independently connect to V_{DD} or V_{SS} via a resistor. Output: Leave open.
P130	3-C	Output	Leave open.
AV_{REF}	–	Input	Directly connect to V_{DD}.

<R> **Table 3-3. Special Function Registers (4/4)**

Address	Symbol	Bit No.								R/W	Number of Bits Manipulated Simultaneously			After Reset	Reference page
		7	6	5	4	3	2	1	0		1	8	16		
FFE2H, FFE3H	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FFE4H	MK0	<ADMK>	<TMMK010>	<TMMK000>	<TMMKH1>	<PMK1>	<PMK0>	<LVIMK>	1	R/W	√	√	–	FFH	225
FFE5H	MK1	1	<STMK6>	<SRMK6>	<SREMK6>	<TMMK80>	<PMK3>	<PMK2>	1		√	√	–	FFH	225
FFE6H to FFEBH	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FFECH	INTM0	ES21	ES20	ES11	ES10	ES01	ES00	0	0	R/W	–	√	–	00H	226
FFEDH	INTM1	0	0	0	0	0	0	ES31	ES30		–	√	–	00H	227
FFEEH to FFF2H	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FFF3H	PPCC	0	0	0	0	0	0	PPCC1	PPCC0	R/W	√	√	–	02H	74
FFF4H	OSTS	0	0	0	0	0	0	OSTS1	OSTS0		–	√	–	Undefined Note	76, 235
FFF5H to FFFAH	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FFFBH	PCC	0	0	0	0	0	0	PCC1	0	R/W	√	√	–	02H	74
FFFCH to FFFFH	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–

Note The oscillation stabilization time that elapses after release of reset is selected by the option byte. For details, refer to **CHAPTER 17 OPTION BYTE**.

Remark For a bit name enclosed in angle brackets (<>), the bit name is defined as a reserved word in the RA78K0S, and is defined as an sfr variable using the #pragma sfr directive in the CC78K0S.

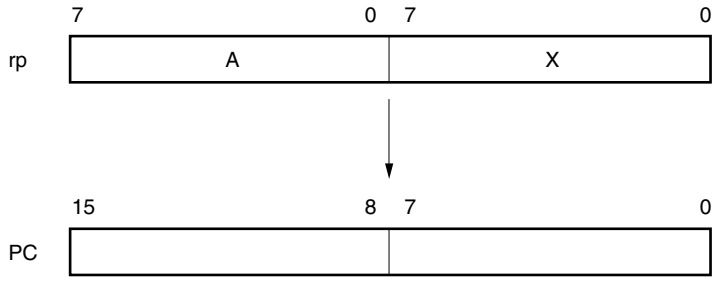
3.3.4 Register addressing

[Function]

The register pair (AX) contents to be specified with an instruction word are transferred to the program counter (PC) to branch.

This function is carried out when the BR AX instruction is executed.

[Illustration]



(1) 16-bit timer counter 00 (TM00)

TM00 is a 16-bit read-only register that counts count pulses.

The counter is incremented in synchronization with the rising edge of the count clock. If the count value is read during operation, input of the count clock is temporarily stopped, and the count value at that point is read.

Figure 6-2. Format of 16-bit Timer Counter 00 (TM00)

Address: FF12H, FF13H After reset: 0000H R

Symbol	FF13H								FF12H							
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
TM00																

The count value is reset to 0000H in the following cases.

<1> A reset signal is generated.
<2> If TMC003 and TMC002 are cleared
<3> If the valid edge of TI000 is input in the clear & start mode entered by inputting the valid edge of TI000
<4> If TM00 and CR000 match in the clear & start mode entered on a match between TM00 and CR000
<5> If OSPT00 is set to 1 in the one-shot pulse output mode

Cautions 1. Even if TM00 is read, the value is not captured by CR010.
2. When TM00 is read, count misses do not occur, since the input of the count clock is temporarily stopped and then resumed after the read.

(2) 16-bit timer capture/compare register 000 (CR000)

CR000 is a 16-bit register which has the functions of both a capture register and a compare register. Whether it is used as a capture register or as a compare register is set by bit 0 (CRC000) of capture/compare control register 00 (CRC00).

CR000 is set by 16-bit memory manipulation instruction.

A reset signal generation clears CR000 to 0000H.

Figure 6-3. Format of 16-bit Timer Capture/Compare Register 000 (CR000)

Address: FF14H, FF15H After reset: 0000H R/W

Symbol	FF15H								FF14H							
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
CR000																

- **When CR000 is used as a compare register**

  The value set in CR000 is constantly compared with the 16-bit timer/counter 00 (TM00) count value, and an interrupt request (INTTM000) is generated if they match. It can also be used as the register that holds the interval time then TM00 is set to interval timer operation.

- **When CR000 is used as a capture register**

  It is possible to select the valid edge of the TI000 pin or the TI010 pin as the capture trigger. Setting of the TI000 or TI010 valid edge is performed by means of prescaler mode register 00 (PRM00) (refer to **Table 6-2**).

(17) Changing compare register during timer operation

<1> With the 16-bit timer capture/compare register 0n0 (CR0n0) used as a compare register, when changing CR0n0 around the timing of a match between 16-bit timer counter 00 (TM00) and 16-bit timer capture/compare register 0n0 (CR0n0) during timer counting, the change timing may conflict with the timing of the match, so the operation is not guaranteed in such cases. To change CR0n0 during timer counting, INTTM000 interrupt servicing performs the following operation.

<Changing cycle (CR000)>

1. Disable the timer output inversion operation at the match between TM00 and CR000 (TOC001 = 0).
2. Disable the INTTM000 interrupt (TMMK000 = 1).
3. Rewrite CR000.
4. Wait for 1 cycle of the TM00 count clock.
5. Enable the timer output inversion operation at the match between TM00 and CR000 (TOC001 = 1).
6. Clear the interrupt request flag of INTTM000 (TMIF000 = 0).
7. Enable the INTTM000 interrupt (TMMK000 = 0).

<Changing duty (CR010)>

1. Disable the timer output inversion operation at the match between TM00 and CR010 (TOC004 = 0).
2. Disable the INTTM000 interrupt (TMMK000 = 1).
3. Rewrite CR010.
4. Wait for 1 cycle of the TM00 count clock.
5. Enable the timer output inversion operation at the match between TM00 and CR010 (TOC004 = 1).
6. Clear the interrupt request flag of INTTM000 (TMIF000 = 0).
7. Enable the INTTM000 interrupt (TMMK000 = 0).

While interrupts and timer output inversion are disabled (1 to 4 above), timer counting is continued. If the value to be set in CR0n0 is small, the value of TM00 may exceed CR0n0. Therefore, set the value, considering the time lapse of the timer clock and CPU clock after an INTTM000 interrupt has been generated.

Remark n = 0, 1

<2> If CR010 is changed during timer counting without performing processing <1> above, the value in CR010 may be rewritten twice or more, causing an inversion of the output level of the TO00 pin at each rewrite.

9.4.3 Watchdog timer operation in STOP mode (when "low-speed internal oscillator can be stopped by software" is selected by option byte)

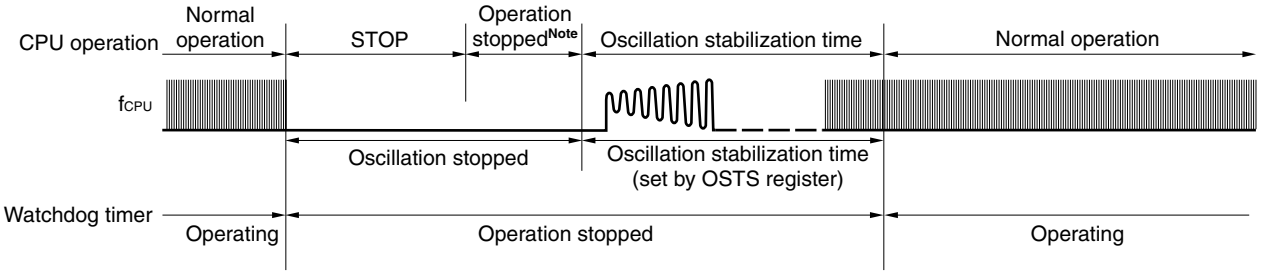
The watchdog timer stops counting during STOP instruction execution regardless of whether the system clock or low-speed internal oscillation clock is being used.

(1) When the watchdog timer operation clock is the clock to peripheral hardware (f_X) when the STOP instruction is executed

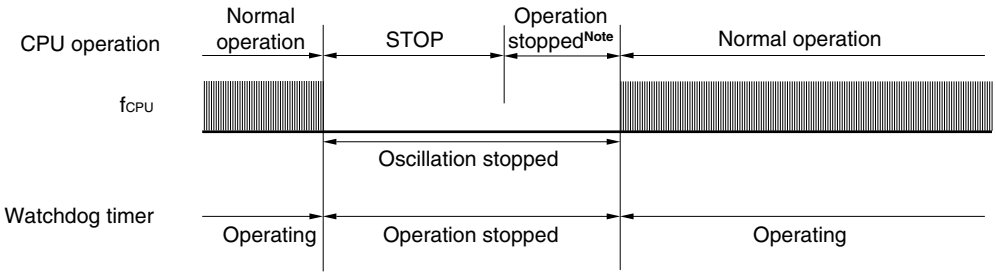
When STOP instruction is executed, operation of the watchdog timer is stopped. After STOP mode is released, operation stops for 34 μs (TYP.) (after waiting for the oscillation stabilization time set by the oscillation stabilization time select register (OSTS) after operation stops in the case of crystal/ceramic oscillation) and then counting is started again using the operation clock before the operation was stopped. At this time, the counter is not cleared to 0 but holds its value.

Figure 9-6. Operation in STOP Mode (WDT Operation Clock: Clock to Peripheral Hardware)

<1> CPU clock: Crystal/ceramic oscillation clock



<2> CPU clock: High-speed internal oscillation clock or external clock input



Note The operation stop time is 17 μs (MIN.), 34 μs (TYP.), and 67 μs (MAX.).

9.4.4 Watchdog timer operation in HALT mode (when “low-speed internal oscillator can be stopped by software” is selected by option byte)

The watchdog timer stops counting during HALT instruction execution regardless of whether the operation clock of the watchdog timer is the system clock (f_X) or low-speed internal oscillation clock (f_{RL}). After HALT mode is released, counting is started again using the operation clock before the operation was stopped. At this time, the counter is not cleared to 0 but holds its value.

Figure 9-8. Operation in HALT Mode

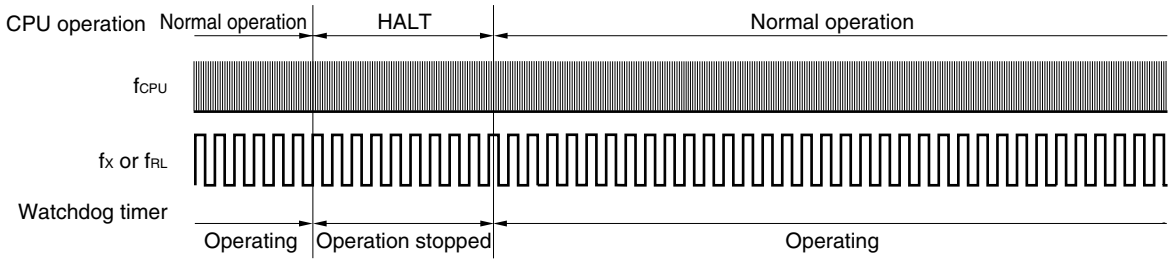
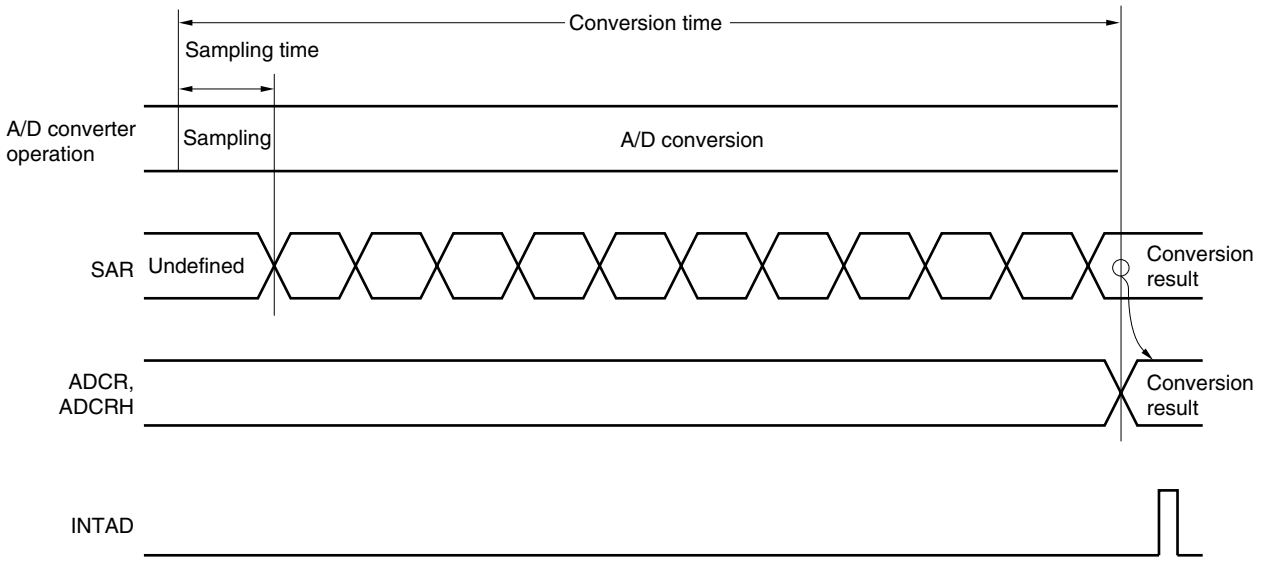


Figure 10-10. Basic Operation of A/D Converter



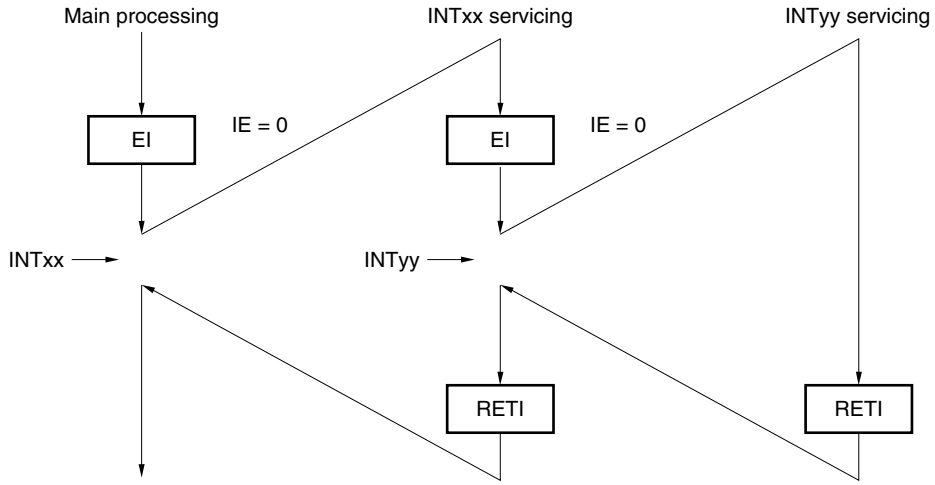
A/D conversion operations are performed continuously until bit 7 (ADCS) of the A/D converter mode register (ADM) is reset (0) by software.

If a write operation is performed to ADM or the analog input channel specification register (ADS) during an A/D conversion operation, the conversion operation is initialized, and if the ADCS bit is set (1), conversion starts again from the beginning.

Reset signal generation makes the A/D conversion result register (ADCR, ADCRH) undefined.

Figure 12-10. Example of Multiple Interrupts (1/2)

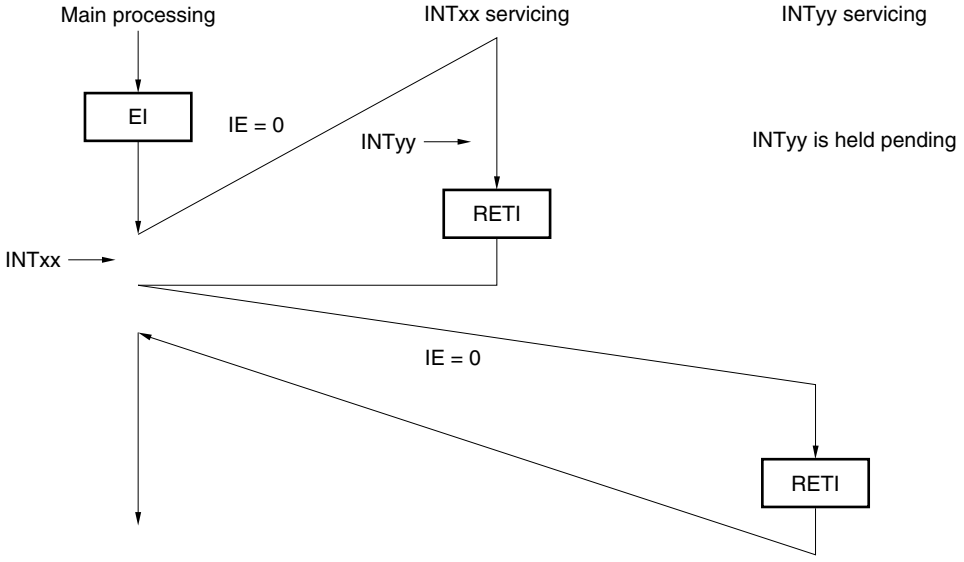
Example 1. Multiple interrupts are acknowledged



During interrupt INTxx servicing, interrupt request INTyy is acknowledged, and multiple interrupts are generated. Before each interrupt request acknowledgment, the EI instruction is issued, the interrupt mask is released, and the interrupt request acknowledgment enable state is set.

Caution Multiple interrupts can be acknowledged even for low-priority interrupts.

Example 2. Multiple interrupts are not generated because interrupts are not enabled



Because interrupts are not enabled in interrupt INTxx servicing (the EI instruction is not issued), interrupt request INTyy is not acknowledged, and multiple interrupts are not generated. The INTyy request is held pending and acknowledged after the INTxx servicing is performed.

IE = 0: Interrupt request acknowledgment disabled

CHAPTER 18 FLASH MEMORY

18.1 Features

The internal flash memory of the 78K0S/KA1+ has the following features.

- Erase/write even without preparing a separate dedicated power supply
- Capacity: 2 KB/4 KB/8 KB
  - Erase unit: 1 block (256 bytes)
  - Write unit: 1 block (at on-board/off-board programming time), 1 byte (at self programming time)
- Rewriting method
  - Rewriting by communication with dedicated flash memory programmer (on-board/off-board programming)
  - Rewriting flash memory by user program (self programming)
- Supports rewriting of the flash memory at on-board/off-board programming time through security functions
- Supports security functions in block units at self programming time through protect bytes

18.8.5 Example of shifting self programming mode to normal mode

The operating mode must be returned from self programming mode to normal mode after performing self programming.

An example of shifting to normal mode is explained below.

<1> Clear FLCMD (FLCMD = 00H).

<2> Clear the flash status register (PFS).

<3> Set normal mode using a specific sequence.

- Write the specific value (A5H) to PFCMD.
- Write 00H to FLPMC (writing in this step is invalid)
- Write 0FFH (inverted value of 00H) to FLPMC (writing in this step is invalid)
- Write 00H to FLPMC (writing in this step is valid)

<4> Check the execution result of the specific sequence using bit 0 (FPRERR) of PFS[Note].
Abnormal → <2>, normal → <5>

<5> Enable interrupt servicing (by executing the EI instruction and changing MK0 and MK1) to restore the original state.

<6> Mode shift is completed

Note Restore the CPU clock to its setting before self programming, after normal execution of the specific sequence.

Caution Be sure to perform the series of operations described above using the user program at an address where data is not erased or written.

Standard product, (A) grade product T_A = –40 to +85°C

LVI Circuit Characteristics (T_A = –40 to +85°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V_{LVI0}		4.1	4.3	4.5	V
	V_{LVI1}		3.9	4.1	4.3	V
	V_{LVI2}		3.7	3.9	4.1	V
	V_{LVI3}		3.5	3.7	3.9	V
	V_{LVI4}		3.3	3.5	3.7	V
	V_{LVI5}		3.15	3.3	3.45	V
	V_{LVI6}		2.95	3.1	3.25	V
	V_{LVI7}		2.7	2.85	3.0	V
	V_{LVI8}		2.5	2.6	2.7	V
	V_{LVI9}		2.25	2.35	2.45	V
Response time[Note 1]	t_{LD}			0.2	2.0	ms
Minimum pulse width	t_{LW}		0.2			ms
Operation stabilization wait time[Note 2]	t_{LWAIT}			0.1	0.2	ms

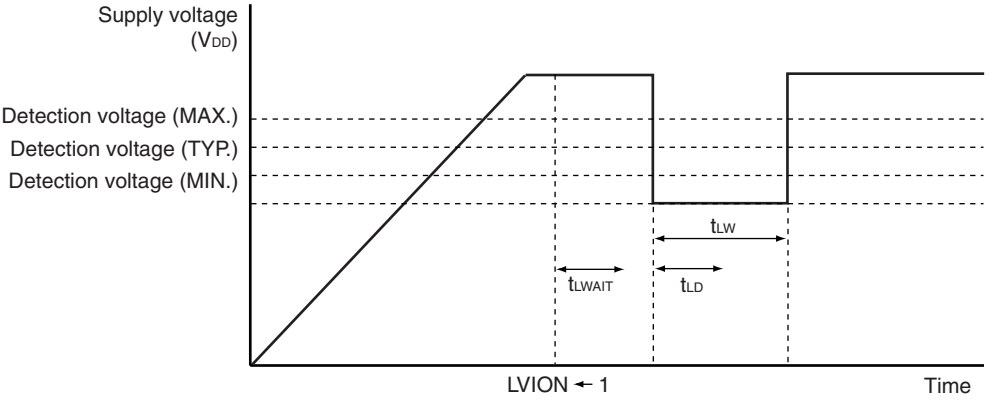
Notes 1. Time required from voltage detection to interrupt output or internal reset signal generation.

2. Time required from setting LVION to 1 to operation stabilization.

Remarks 1. $V_{LVI0} > V_{LVI1} > V_{LVI2} > V_{LVI3} > V_{LVI4} > V_{LVI5} > V_{LVI6} > V_{LVI7} > V_{LVI8} > V_{LVI9}$

2. $V_{POC} < V_{LVIm}$ (m = 0 to 9)

LVI Circuit Timing



Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (T_A = –40 to +85°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		2.0		5.5	V
Release signal set time	t_{SREL}		0			μs

(A2) grade product T_A = –40 to +125°C

AC Characteristics

(1) Basic operation (T_A = –40 to +125°C, V_{DD} = 2.0 to 5.5 V[Note 1], V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Cycle time (minimum instruction execution time)	T_{CY}	Crystal/ceramic oscillation clock, external clock input	4.0 V ≤ V_{DD} ≤ 5.5 V	0.25		16	μs
			3.0 V ≤ V_{DD} < 4.0 V	0.33		16	μs
			2.7 V ≤ V_{DD} < 3.0 V	0.4		16	μs
			2.0 V ≤ V_{DD} < 2.7 V	1		16	μs
		High-speed internal oscillation clock	4.0 V ≤ V_{DD} ≤ 5.5 V	0.23		4.22	μs
			2.7 V ≤ V_{DD} < 4.0 V	0.47		4.22	μs
			2.0 V ≤ V_{DD} < 2.7 V	0.95		4.22	μs
TI000 input high-level width, low-level width	t_{TIH}, t_{TIL}	4.0 V ≤ V_{DD} ≤ 5.5 V		$2/f_{sam}$+ 0.1[Note 2]			μs
		2.0 V ≤ V_{DD} < 4.0 V		$2/f_{sam}$+ 0.2[Note 2]			μs
Interrupt input high-level width, low-level width	t_{INTH}, t_{INTL}			1			μs
$\overline{\text{RESET}}$ input low-level width	t_{RSL}			2			μs

Notes 1. Use this product in a voltage range of 2.26 to 5.5 V because the detection voltage (V_{POC}) of the power-on-clear (POC) circuit is 2.26 V (MAX.).

2. Selection of fsam = f_{XP}, f_{XP}/4, or f_{XP}/256 is possible using bits 0 and 1 (PRM000, PRM001) of prescaler mode register 00 (PRM00). Note that when selecting the TI000 valid edge as the count clock, fsam = f_{XP}.

CPU Clock Frequency, Peripheral Clock Frequency

Parameter	Conditions	CPU Clock (f_{CPU})	Peripheral Clock (f_{XP})
Ceramic resonator, crystal resonator, external clock	4.0 V ≤ V_{DD} ≤ 5.5 V	125 kHz ≤ f_{CPU} ≤ 8 MHz	500 kHz ≤ f_{XP} ≤ 8 MHz
	3.0 V ≤ V_{DD} < 4.0 V	125 kHz ≤ f_{CPU} ≤ 6 MHz	
	2.7 V ≤ V_{DD} < 3.0 V	125 kHz ≤ f_{CPU} ≤ 5 MHz	
	2.0 V ≤ V_{DD} < 2.7 V[Note]	125 kHz ≤ f_{CPU} ≤ 2 MHz	500 kHz ≤ f_{XP} ≤ 5 MHz
High-speed internal oscillator	4.0 V ≤ V_{DD} ≤ 5.5 V	500 kHz (TYP.) ≤ f_{CPU} ≤ 8 MHz (TYP.)	2 MHz (TYP.) ≤ f_{XP} ≤ 8 MHz (TYP.)
	2.7 V ≤ V_{DD} < 4.0 V	500 kHz (TYP.) ≤ f_{CPU} ≤ 4 MHz (TYP.)	
	2.0 V ≤ V_{DD} < 2.7 V[Note]	500 kHz (TYP.) ≤ f_{CPU} ≤ 2 MHz (TYP.)	2 MHz (TYP.) ≤ f_{XP} ≤ 4 MHz (TYP.)

Note Use this product in a voltage range of 2.26 to 5.5 V because the detection voltage (V_{POC}) of the power-on-clear (POC) circuit is 2.26 V (MAX.).

(A2) grade product T_A = –40 to +125°C

A/D Converter Characteristics (T_A = –40 to +125°C, 2.7 V ≤ AV_{REF} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V[Note 1])

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution			10	10	10	bit
Overall error[Notes 2, 3]	AINL	4.0 V ≤ AV_{REF} ≤ 5.5 V		±0.2	±0.7	%FSR
		2.7 V ≤ AV_{REF} < 4.0 V		±0.3	±0.9	%FSR
Conversion time	t_{CONV}	4.5 V ≤ AV_{REF} ≤ 5.5 V	3.0		30	μs
		4.0 V ≤ AV_{REF} < 4.5 V	4.8		30	μs
		2.85 V ≤ AV_{REF} < 4.0 V	6.0		30	μs
		2.7 V ≤ AV_{REF} < 2.85 V	14.0		30	μs
Zero-scale error[Notes 2, 3]	Ezs	4.0 V ≤ AV_{REF} ≤ 5.5 V			±0.7	%FSR
		2.7 V ≤ AV_{REF} < 4.0 V			±0.9	%FSR
Full-scale error[Notes 2, 3]	Efs	4.0 V ≤ AV_{REF} ≤ 5.5 V			±0.7	%FSR
		2.7 V ≤ AV_{REF} < 4.0 V			±0.9	%FSR
Integral non-linearity error[Note 2]	ILE	4.0 V ≤ AV_{REF} ≤ 5.5 V			±5.5	LSB
		2.7 V ≤ AV_{REF} < 4.0 V			±7.5	LSB
Differential non-linearity error[Note 2]	DLE	4.0 V ≤ AV_{REF} ≤ 5.5 V			±2.5	LSB
		2.7 V ≤ AV_{REF} < 4.0 V			±3.0	LSB
Analog input voltage	V_{AIN}		V_{SS}[Note 1]		AV_{REF}	V

Notes 1. In the 78K0S/KA1+, V_{SS} functions alternately as the ground potential of the A/D converter. Be sure to connect V_{SS} to a stabilized GND (= 0 V).

2. Excludes quantization error (±1/2 LSB).

3. This value is indicated as a ratio (%FSR) to the full-scale value.

Caution The conversion accuracy may be degraded when the analog input pin is used as an alternate I/O port or if a port is changed during A/D conversion.

(A2) grade product T_A = –40 to +125°C

Flash Memory Programming Characteristics (T_A = –40 to +105°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Supply current	I_{DD}	V_{DD} = 5.5 V				7.0	mA
Erasure count[Note 1] (per 1 block)	N_{ERASE}	T_A = –40 to +105°C		1000			Times
Chip erase time	T_{CERASE}	T_A = –10 to +105°C, N_{ERASE} ≤ 100	4.5 V ≤ V_{DD} ≤ 5.5 V			0.8	s
			3.5 V ≤ V_{DD} < 4.5 V			1.0	s
			2.7 V ≤ V_{DD} < 3.5 V			1.2	s
		T_A = –10 to +105°C, N_{ERASE} ≤ 1000	4.5 V ≤ V_{DD} ≤ 5.5 V			4.8	s
			3.5 V ≤ V_{DD} < 4.5 V			5.2	s
			2.7 V ≤ V_{DD} < 3.5 V			6.1	s
		T_A = –40 to +105°C, N_{ERASE} ≤ 100	4.5 V ≤ V_{DD} ≤ 5.5 V			1.6	s
			3.5 V ≤ V_{DD} < 4.5 V			1.8	s
			2.7 V ≤ V_{DD} < 3.5 V			2.0	s
		T_A = –40 to +105°C, N_{ERASE} ≤ 1000	4.5 V ≤ V_{DD} ≤ 5.5 V			9.1	s
			3.5 V ≤ V_{DD} < 4.5 V			10.1	s
			2.7 V ≤ V_{DD} < 3.5 V			12.3	s
Block erase time	T_{BERASE}	T_A = –10 to +105°C, N_{ERASE} ≤ 100	4.5 V ≤ V_{DD} ≤ 5.5 V			0.4	s
			3.5 V ≤ V_{DD} < 4.5 V			0.5	s
			2.7 V ≤ V_{DD} < 3.5 V			0.6	s
		T_A = –10 to +105°C, N_{ERASE} ≤ 1000	4.5 V ≤ V_{DD} ≤ 5.5 V			2.6	s
			3.5 V ≤ V_{DD} < 4.5 V			2.8	s
			2.7 V ≤ V_{DD} < 3.5 V			3.3	s
		T_A = –40 to +105°C, N_{ERASE} ≤ 100	4.5 V ≤ V_{DD} ≤ 5.5 V			0.9	s
			3.5 V ≤ V_{DD} < 4.5 V			1.0	s
			2.7 V ≤ V_{DD} < 3.5 V			1.1	s
		T_A = –40 to +105°C, N_{ERASE} ≤ 1000	4.5 V ≤ V_{DD} ≤ 5.5 V			4.9	s
			3.5 V ≤ V_{DD} < 4.5 V			5.4	s
			2.7 V ≤ V_{DD} < 3.5 V			6.6	s
Byte write time	T_{WRITE}	T_A = –40 to +105°C, N_{ERASE} ≤ 1000				150	μs
Internal verify	T_{VERIFY}	Per 1 block				6.8	ms
		Per 1 byte				27	μs
Blank check	T_{BLKCHK}	Per 1 block				480	μs
Total loss	P_T[Note 3]	T_A = –40 to +105°C				120	mW
Retention years		T_A = 85°C[Note 2], N_{ERASE} ≤ 1000		10			Years

Notes 1. Depending on the erasure count (N_{ERASE}), the erase time varies. Refer to the chip erase time and block erase time parameters.

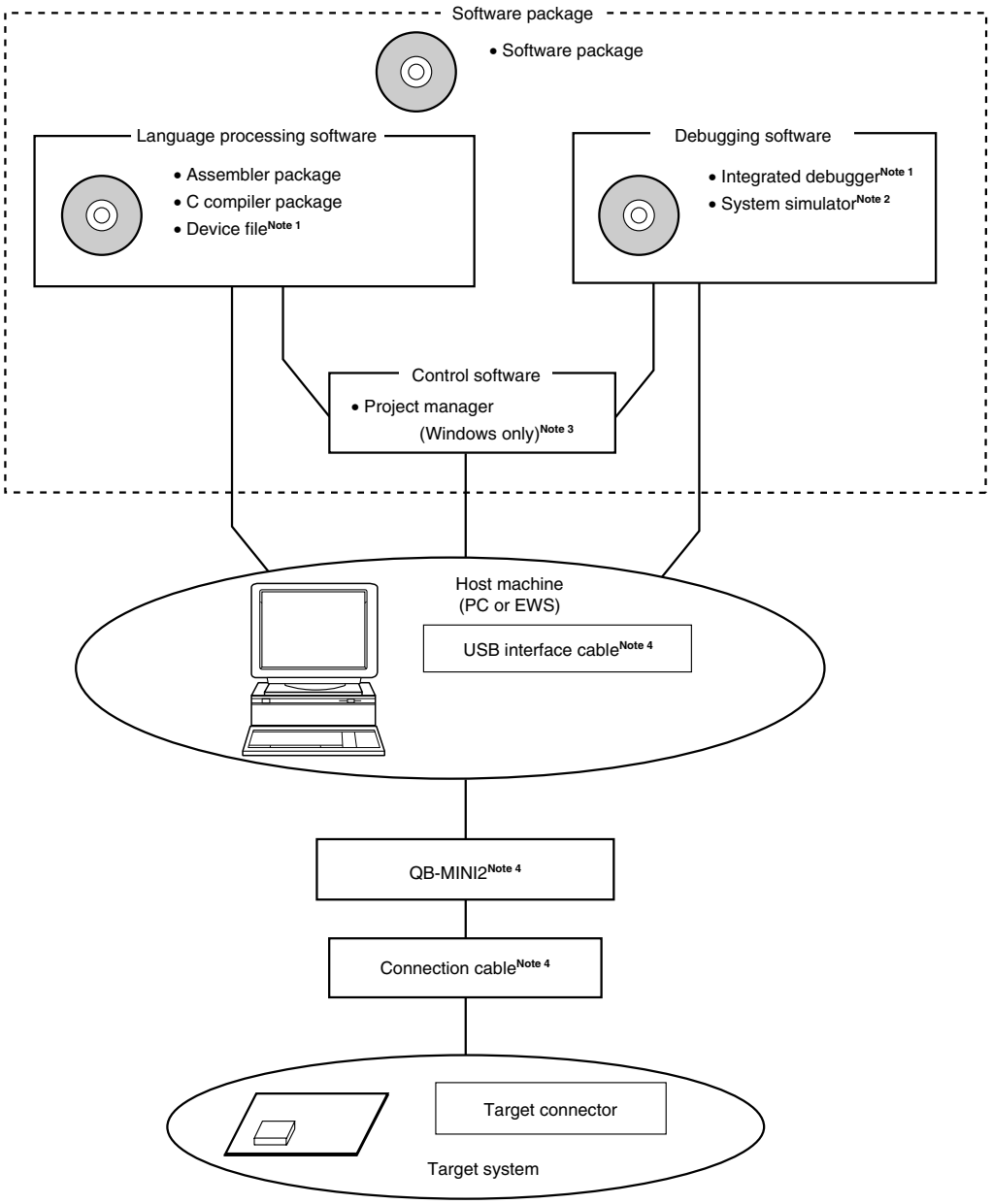
2. When the average temperature when operating and not operating is 85°C.

Remark When a product is first written after shipment, “erase → write” and “write only” are both taken as one rewrite.

(Note 3 is listed on the next page.)

Figure A-1. Development Tool Configuration (2/2)

(2) When using the on-chip debug emulator with programming function QB-MINI2



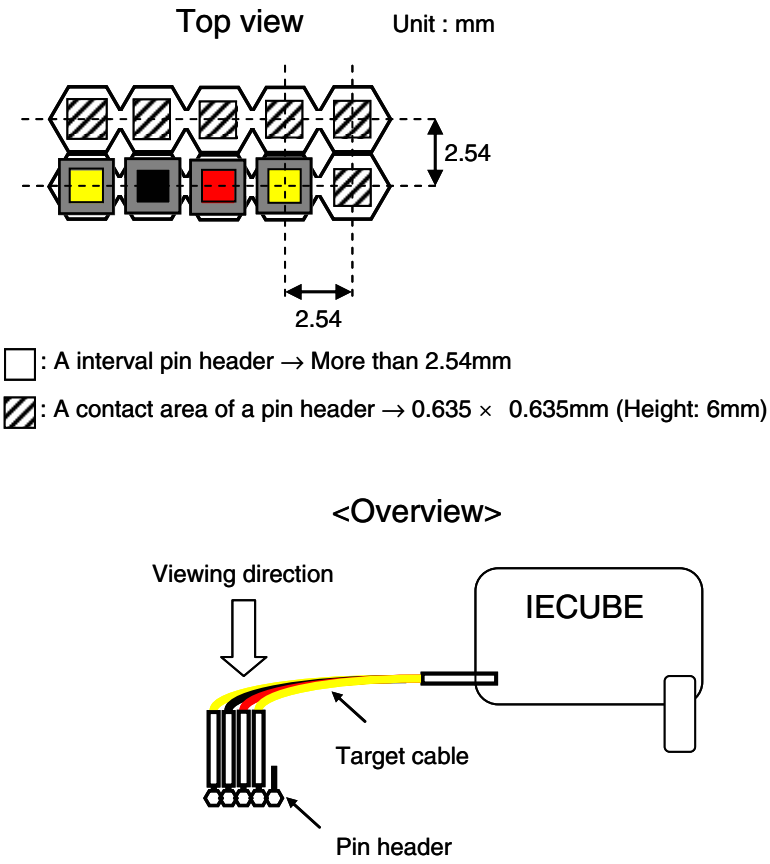
Notes 1. Download the device file for 78K0S/Kx1+ microcontrollers (DF789234) and the integrated debugger ID78K0S-QB from the download site for development tools (http://www.necel.com/micro/en/ods/).

2. SM+ for 78K0S (instruction simulation version) is included in the software package. SM+ for 78K0S/Kx1+ (instruction + peripheral simulation version) is not included.

3. The project manager PM+ is included in the assembler package.
PM+ cannot be used other than with Windows.

4. QB-MINI2 is supplied with USB interface cable and connection cable. Any other products are sold separately. In addition, download the software for operating the QB-MINI2 from the download site for development tools (http://www.necel.com/micro/en/ods/).

Figure B-2. When using the 78K0S/Kx1+ target cable (single track)



(2/10)

Edition	Description	Applied to:
2nd edition	Modification of output width of INTTM010 and INTTM000 in the following figures • **Figure 6-17 CR010 Capture Operation with Rising Edge Specified** • **Figure 6-20 Timing of Pulse Width Measurement Operation by Free-Running Counter and One Capture Register (with Both Edges Specified)** • **Figure 6-22 Timing of Pulse Width Measurement Operation with Free-Running Counter (with Both Edges Specified)** • **Figure 6-24 Timing of Pulse Width Measurement Operation by Free-Running Counter and Two Capture Registers (with Rising Edge Specified)** • **Figure 6-26 Timing of Pulse Width Measurement Operation by Means of Restart (with Rising Edge Specified)**	**CHAPTER 6 16-BIT TIMER/EVENT COUNTER 00**
	Modification of **Caution 1** in **Figure 6-29 Control Register Settings for PPG Output Operation**	
	Modification of **Figure 6-33 Timing of One-Shot Pulse Output Operation with Software Trigger**	
	Modification and addition to **6.5 Cautions Related to 16-bit Timer/Event Counter 00**	
	Addition of **Caution 2** to **Figure 7-4 Format of 8-bit Timer Mode Control Register 80 (TMC80)**	**CHAPTER 7 8-BIT TIMER 80**
	Modification of **Table 9-1 Loop Detection Time of Watchdog Timer**	**CHAPTER 9 WATCHDOG TIMER**
	Addition of **Caution 4** and modification to **Figure 9-2 Format of Watchdog Timer Mode Register (WDTM)**	
	Modification of **Figure 9-4 Status Transition Diagram When "Low-Speed Internal Oscillator Cannot Be Stopped" Is Selected by Option Byte**	
	Modification of **Figure 9-5 Status Transition Diagram When "Low-Speed Internal Oscillator Can Be Stopped by Software" Is Selected by Option Byte**	
	Addition of **Note** to and modification of **Figure 10-1 Timing of A/D Converter Sampling and A/D Conversion**	**CHAPTER 10 A/D CONVERTER**
	Addition of **Note 1**, **Caution**, and **Remark 2** to and modification of **Table 10-1 Sampling Time and A/D Conversion Time**	
	Modification of **Figure 10-2 Block Diagram of A/D Converter**	
	Modification of **Note 5**, addition of **Notes 1, 2**, **Cautions 1, 2, 4** and **Remark 2** to, and modification of **Figure 10-3 Format of A/D Converter Mode Register (ADM)**	
	Modification of **Note** in **Figure 10-4 Timing Chart When Comparator Is Used**	
	Addition of explanation <3> to **10.4.1 Basic operations of A/D converter**	
	Modification of **Figure 10-11 Relationship Between Analog Input Voltage and A/D Conversion Result**	
	Addition of explanation <3> to **10.4.3 A/D converter operation mode**	
	Partial modification of **10.6 (1) Operating current in STOP mode** and **(6) Input impedance of ANI0 to ANI3 pins**	
	Modification of capacitor value in **Figure 10-19 Analog Input Pin Connection**	
	Modification of **Figure 10-21 Internal Equivalent Circuit of ANIn Pin** and **Table 10-4 Resistance and Capacitance Values (Reference Values) of Equivalent Circuit**	
	Addition of description to **11.2 (3) Transmit buffer register 6 (TXB6)**	**CHAPTER 11 SERIAL INTERFACE UART6**
	Modification of **Note 1** in **Figure 11-5 Format of Asynchronous Serial Interface Operation Mode Register 6 (ASIM6) (1/2)**	
	Modification of **Caution** in **11.3 (6) Asynchronous serial interface control register 6 (ASICL6)**	
	Modification of **Caution 1** in **11.4.2 (2) (d) Continuous transmission**	