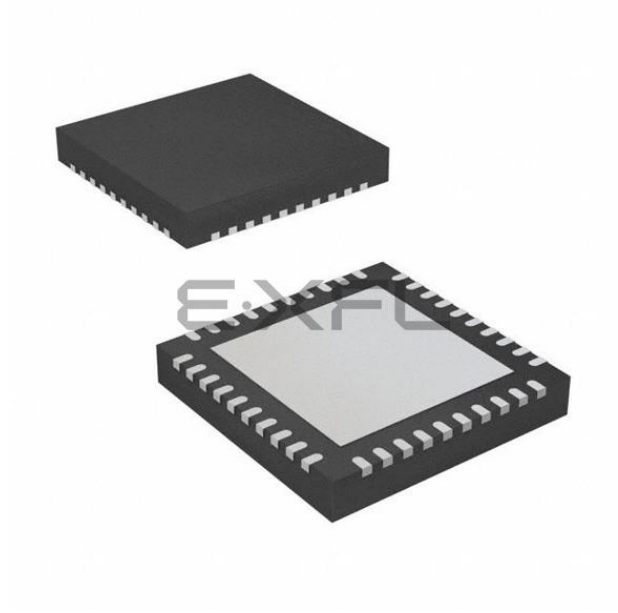

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	44MHz
Connectivity	EBI/EMI, I²C, SPI, UART/USART
Peripherals	PLA, PWM, PSM, Temp Sensor, WDT
Number of I/O	14
Program Memory Size	62KB (31K x16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 32
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 5x12b; D/A 3x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	40-VFQFN Exposed Pad, CSP
Supplier Device Package	40-LFCSP-VQ (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/aduc7019bcpz62i

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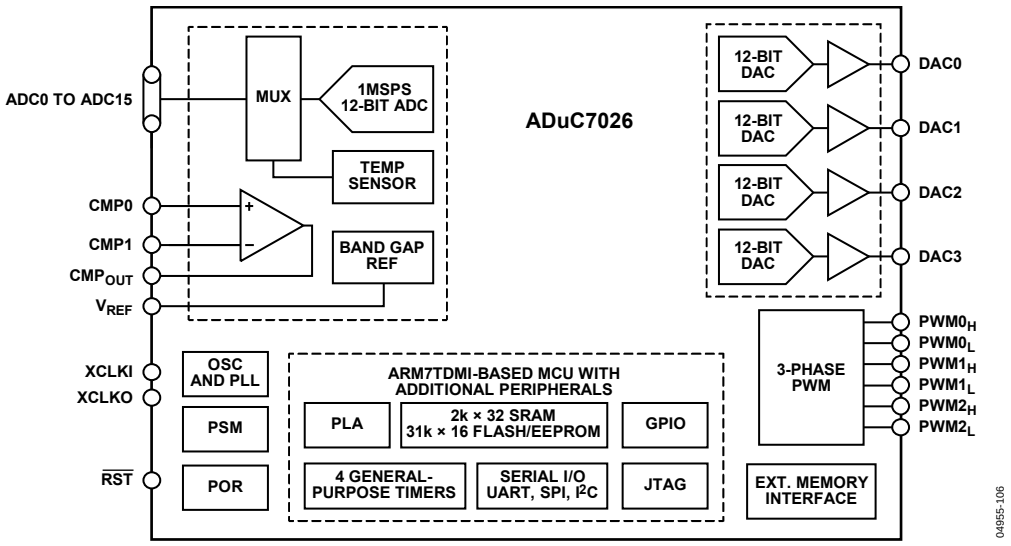

Figure 7.

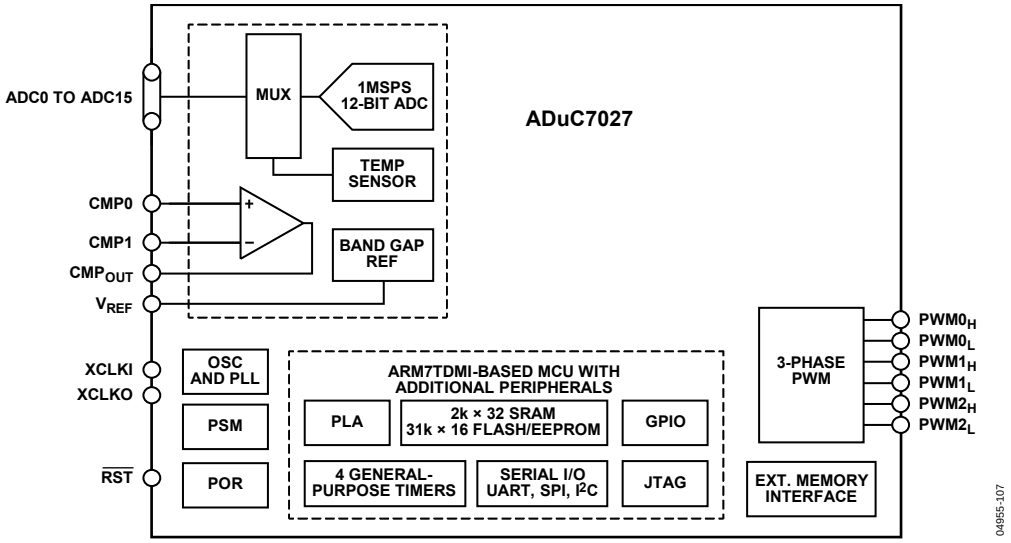

Figure 8.

SPECIFICATIONS

AV_{DD} = IOV_{DD} = 2.7 V to 3.6 V, V_{REF} = 2.5 V internal reference, f_{CORE} = 41.78 MHz, T_A = −40°C to +125°C, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
ADC CHANNEL SPECIFICATIONS					Eight acquisition clocks and fADC/2
ADC Power-Up Time		5		µs	
DC Accuracy[1, 2]					
Resolution	12			Bits	
Integral Nonlinearity		±0.6	±1.5	LSB	2.5 V internal reference
		±1.0		LSB	1.0 V external reference
Differential Nonlinearity[3, 4]		±0.5	+1/−0.9	LSB	2.5 V internal reference
		+0.7/−0.6		LSB	1.0 V external reference
DC Code Distribution		1		LSB	ADC input is a dc voltage
ENDPOINT ERRORS[5]					
Offset Error		±1	±2	LSB	
Offset Error Match		±1		LSB	
Gain Error		±2	±5	LSB	
Gain Error Match		±1		LSB	
DYNAMIC PERFORMANCE					f_{IN} = 10 kHz sine wave, f_{SAMPLE} = 1 MSPS
Signal-to-Noise Ratio (SNR)		69		dB	Includes distortion and noise components
Total Harmonic Distortion (THD)		−78		dB	
Peak Harmonic or Spurious Noise (PHSN)		−75		dB	
Channel-to-Channel Crosstalk		−80		dB	Measured on adjacent channels
ANALOG INPUT					
Input Voltage Ranges					
Differential Mode			V_{CM}[6] ± V_{REF}/2	V	
Single-Ended Mode			0 to V_{REF}	V	
Leakage Current		±1	±6	µA	
Input Capacitance		20		pF	During ADC acquisition
ON-CHIP VOLTAGE REFERENCE					0.47 µF from V_{REF} to AGND
Output Voltage		2.5		V	
Accuracy			±5	mV	T_A = 25°C
Reference Temperature Coefficient		±40		ppm/°C	
Power Supply Rejection Ratio		75		dB	
Output Impedance		70		Ω	T_A = 25°C
Internal V_{REF} Power-On Time		1		ms	
EXTERNAL REFERENCE INPUT					
Input Voltage Range	0.625		AV_{DD}	V	
DAC CHANNEL SPECIFICATIONS					R_L = 5 kΩ, C_L = 100 pF
DC Accuracy[7]					
Resolution		12		Bits	
Relative Accuracy		±2		LSB	
Differential Nonlinearity			±1	LSB	Guaranteed monotonic
Offset Error			±15	mV	2.5 V internal reference
Gain Error[8]			±1	%	
Gain Error Mismatch		0.1		%	% of full scale on DAC0
ANALOG OUTPUTS					
Output Voltage Range_0		0 to DAC_{REF}		V	DAC_{REF} range: DACGND to $DACV_{DD}$
Output Voltage Range_1		0 to 2.5		V	
Output Voltage Range_2		0 to $DACV_{DD}$		V	
Output Impedance		2		Ω	

Table 7. SPI Master Mode Timing (Phase Mode = 0)

Parameter	Description	Min	Typ	Max	Unit
t_{SL}	SCLK low pulse width[1]		(SPIDIV + 1) × t_{HCLK}		ns
t_{SH}	SCLK high pulse width[1]		(SPIDIV + 1) × t_{HCLK}		ns
t_{DAV}	Data output valid after SCLK edge			25	ns
t_{DOSU}	Data output setup before SCLK edge			75	ns
t_{DSU}	Data input setup time before SCLK edge[2]	1 × t_{UCLK}			ns
t_{DHD}	Data input hold time after SCLK edge[2]	2 × t_{UCLK}			ns
t_{DF}	Data output fall time		5	12.5	ns
t_{DR}	Data output rise time		5	12.5	ns
t_{SR}	SCLK rise time		5	12.5	ns
t_{SF}	SCLK fall time		5	12.5	ns

[1] t_{HCLK} depends on the clock divider or CD bits in the POWCONMMR. $t_{HCLK} = t_{UCLK}/2^{CD}$; see Figure 67.
[2] t_{UCLK} = 23.9 ns. It corresponds to the 41.78 MHz internal clock from the PLL before the clock divider; see Figure 67.

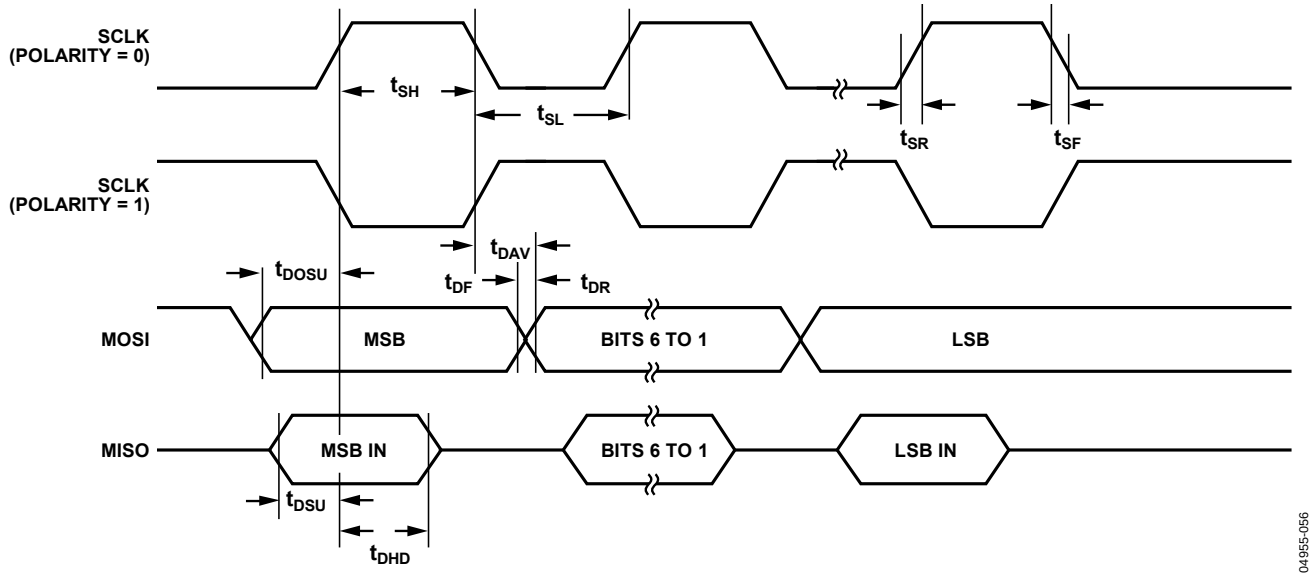

Figure 16. SPI Master Mode Timing (Phase Mode = 0)

Table 8. SPI Slave Mode Timing (Phsae Mode = 1)

Parameter	Description	Min	Typ	Max	Unit
$t_{\overline{CS}}$	$\overline{CS}$ to SCLK edge[1]	$(2 \times t_{HCLK}) + (2 \times t_{UCLK})$			ns
t_{SL}	SCLK low pulse width[2]		$(SPIDIV + 1) \times t_{HCLK}$		ns
t_{SH}	SCLK high pulse width[2]		$(SPIDIV + 1) \times t_{HCLK}$		ns
t_{DAV}	Data output valid after SCLK edge			25	ns
t_{DSU}	Data input setup time before SCLK edge[1]	$1 \times t_{UCLK}$			ns
t_{DHD}	Data input hold time after SCLK edge[1]	$2 \times t_{UCLK}$			ns
t_{DF}	Data output fall time		5	12.5	ns
t_{DR}	Data output rise time		5	12.5	ns
t_{SR}	SCLK rise time		5	12.5	ns
t_{SF}	SCLK fall time		5	12.5	ns
t_{SFS}	$\overline{CS}$ high after SCLK edge	0			ns

[1] t_{UCLK} = 23.9 ns. It corresponds to the 41.78 MHz internal clock from the PLL before the clock divider; see Figure 67.
[2] t_{HCLK} depends on the clock divider or CD bits in the POWCONMMR. $t_{HCLK} = t_{UCLK}/2^{CD}$; see Figure 67.

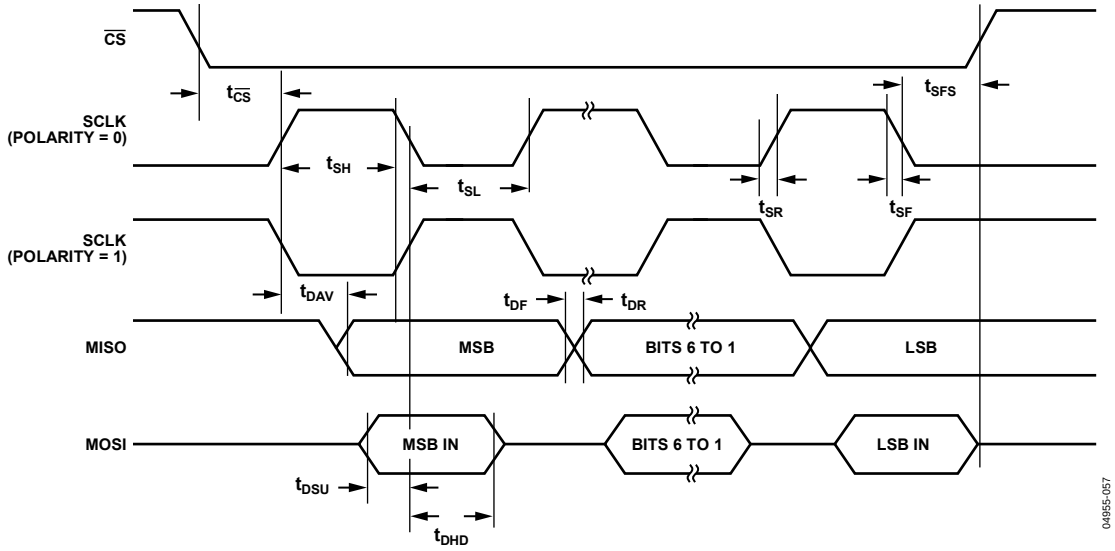

Figure 17. SPI Slave Mode Timing (Phase Mode = 1)

Pin No.				
7019/7020	7021	7022	Mnemonic	Description
22	22	21	P2.0/SPM9/PLAO[5]/$\overline{CONV_{START}}$	Serial Port Multiplexed. General-Purpose Input and Output Port 2.0/UART/ Programmable Logic Array Output Element 5/Start Conversion Input Signal for ADC.
23	23	22	P0.7/ECLK/XCLK/SPM8/PLAO[4]	Serial Port Multiplexed. General-Purpose Input and Output Port 0.7/ Output for External Clock Signal/Input to the Internal Clock Generator Circuits/UART/ Programmable Logic Array Output Element 4.
24	24	23	XCLKO	Output from the Crystal Oscillator Inverter.
25	25	24	XCLKI	Input to the Crystal Oscillator Inverter and Input to the Internal Clock Generator Circuits.
26	26	25	P1.7/SPM7/PLAO[0]	Serial Port Multiplexed. General-Purpose Input and Output Port 1.7/UART, SPI/Programmable Logic Array Output Element 0.
27	27	26	P1.6/SPM6/PLAI[6]	Serial Port Multiplexed. General-Purpose Input and Output Port 1.6/UART, SPI/Programmable Logic Array Input Element 6.
28	28	27	P1.5/SPM5/PLAI[5]/IRQ3	Serial Port Multiplexed. General-Purpose Input and Output Port 1.5/UART, SPI/Programmable Logic Array Input Element 5/External Interrupt Request 3, Active High.
29	29	28	P1.4/SPM4/PLAI[4]/IRQ2	Serial Port Multiplexed. General-Purpose Input and Output Port 1.4/UART, SPI/Programmable Logic Array Input Element 4/External Interrupt Request 2, Active High.
30	30	29	P1.3/SPM3/PLAI[3]	Serial Port Multiplexed. General-Purpose Input and Output Port 1.3/UART, I2C1/Programmable Logic Array Input Element 3.
31	31	30	P1.2/SPM2/PLAI[2]	Serial Port Multiplexed. General-Purpose Input and Output Port 1.2/UART, I2C1/Programmable Logic Array Input Element 2.
32	32	31	P1.1/SPM1/PLAI[1]	Serial Port Multiplexed. General-Purpose Input and Output Port 1.1/UART, I2C0/Programmable Logic Array Input Element 1.
33	33	32	P1.0/T1/SPM0/PLAI[0]	Serial Port Multiplexed. General-Purpose Input and Output Port 1.0/ Timer1 Input/UART, I2C0/Programmable Logic Array Input Element 0.
34	–	–	P4.2/PLAO[10]	General-Purpose Input and Output Port 4.2/Programmable Logic Array Output Element 10.
35	34	33	V_{REF}	2.5 V Internal Voltage Reference. Must be connected to a 0.47 µF capacitor when using the internal reference.
36	35	34	AGND	Analog Ground. Ground reference point for the analog circuitry.
37	36	35	AV_{DD}	3.3 V Analog Power.
0	0	0	EP	Exposed Pad. The pin configuration for the ADuC7019/ADuC7020/ ADuC7021/ADuC7022 has an exposed pad that must be soldered for mechanical purposes and left unconnected.

Pin No.	Mnemonic	Description
18	P4.6/AD14/PLAO[14]	General-Purpose Input and Output Port 4.6/External Memory Interface/Programmable Logic Array Output Element 14.
19	P4.7/AD15/PLAO[15]	General-Purpose Input and Output Port 4.7/External Memory Interface/Programmable Logic Array Output Element 15.
20	BM/P0.0/CMP_{OUT}/PLAI[7]/MS0	Multifunction I/O Pin. Boot Mode. The ADuC7026/ADuC7027 enter UART download mode if BM is low at reset and execute code if BM is pulled high at reset through a 1 kΩ resistor/General-Purpose Input and Output Port 0.0/Voltage Comparator Output/Programmable Logic Array Input Element 7/External Memory Select 0.
21	P0.6/T1/MRST/PLAO[3]	Multifunction Pin, Driven Low After Reset. General-Purpose Output Port 0.6/Timer1 Input/Power-On Reset Output/Programmable Logic Array Output Element 3.
22	TCK	JTAG Test Port Input, Test Clock. Debug and download access.
23	TDO	JTAG Test Port Output, Test Data Out. Debug and download access.
24	P0.2/$PWM2_L$/$\overline{BHE}$	General-Purpose Input and Output Port 0.2/PWM Phase 2 Low-Side Output/External Memory Byte High Enable.
25	IOGND	Ground for GPIO (see Table 78). Typically connected to DGND.
26	IOV_{DD}	3.3 V Supply for GPIO (see Table 78) and Input of the On-Chip Voltage Regulator.
27	LV_{DD}	2.6 V Output of the On-Chip Voltage Regulator. This output must be connected to a 0.47 µF capacitor to DGND only.
28	DGND	Ground for Core Logic.
29	P3.0/AD0/$PWM0_H$/PLAI[8]	General-Purpose Input and Output Port 3.0/External Memory Interface/PWM Phase 0 High-Side Output/Programmable Logic Array Input Element 8.
30	P3.1/AD1/$PWM0_L$/PLAI[9]	General-Purpose Input and Output Port 3.1/External Memory Interface/PWM Phase 0 Low-Side Output/Programmable Logic Array Input Element 9.
31	P3.2/AD2/$PWM1_H$/PLAI[10]	General-Purpose Input and Output Port 3.2/External Memory Interface/PWM Phase 1 High-Side Output/Programmable Logic Array Input Element 10.
32	P3.3/AD3/$PWM1_L$/PLAI[11]	General-Purpose Input and Output Port 3.3/External Memory Interface/PWM Phase 1 Low-Side Output/Programmable Logic Array Input Element 11.
33	P2.4/$PWM0_H$/MS0	General-Purpose Input and Output Port 2.4/PWM Phase 0 High-Side Output/External Memory Select 0.
34	P0.3/TRST/A16/ADC_{BUSY}	General-Purpose Input and Output Port 0.3/JTAG Test Port Input, Test Reset/ADC_{BUSY} Signal Output.
35	P2.5/$PWM0_L$/MS1	General-Purpose Input and Output Port 2.5/PWM Phase 0 Low-Side Output/External Memory Select 1.
36	P2.6/$PWM1_H$/MS2	General-Purpose Input and Output Port 2.6/PWM Phase 1 High-Side Output/External Memory Select 2.
37	$\overline{RST}$	Reset Input, Active Low.
38	P3.4/AD4/$PWM2_H$/PLAI[12]	General-Purpose Input and Output Port 3.4/External Memory Interface/PWM Phase 2 High-Side Output/Programmable Logic Array Input 12.
39	P3.5/AD5/$PWM2_L$/PLAI[13]	General-Purpose Input and Output Port 3.5/External Memory Interface/PWM Phase 2 Low-Side Output/Programmable Logic Array Input Element 13.
40	IRQ0/P0.4/PWM_{TRIP}/PLAO[1]/MS1	Multifunction I/O Pin. External Interrupt Request 0, Active High/General-Purpose Input and Output Port 0.4/PWM Trip External Input/Programmable Logic Array Output Element 1/External Memory Select 1.
41	IRQ1/P0.5/ADC_{BUSY}/PLAO[2]/MS2	Multifunction I/O Pin. External Interrupt Request 1, Active High/General-Purpose Input and Output Port 0.5/ADC_{BUSY} Signal Output/Programmable Logic Array Output Element 2/External Memory Select 2.
42	P2.0/SPM9/PLAO[5]/$\overline{CONV_{START}}$	Serial Port Multiplexed. General-Purpose Input and Output Port 2.0/UART/Programmable Logic Array Output Element 5/Start Conversion Input Signal for ADC.
43	P0.7/ECLK/XCLK/SPM8/PLAO[4]	Serial Port Multiplexed. General-Purpose Input and Output Port 0.7/Output for External Clock Signal/Input to the Internal Clock Generator Circuits/UART/Programmable Logic Array Output Element 4.
44	XCLKO	Output from the Crystal Oscillator Inverter.
45	XCLKI	Input to the Crystal Oscillator Inverter and Input to the Internal Clock Generator Circuits.

Pin No.	Mnemonic	Description
46	P3.6/AD6/PWM_{TRIP}/PLAI[14]	General-Purpose Input and Output Port 3.6/External Memory Interface/PWM Safety Cutoff/ Programmable Logic Array Input Element 14.
47	P3.7/AD7/PWM_{SYNC}/PLAI[15]	General-Purpose Input and Output Port 3.7/External Memory Interface/PWM Synchronization/ Programmable Logic Array Input Element 15.
48	P2.7/$PWM1_L$/MS3	General-Purpose Input and Output Port 2.7/PWM Phase 1 Low-Side Output/External Memory Select 3.
49	P2.1/$\overline{WS}$/$PWM0_H$/PLAO[6]	General-Purpose Input and Output Port 2.1/External Memory Write Strobe/PWM Phase 0 High-Side Output/Programmable Logic Array Output Element 6.
50	P2.2/$\overline{RS}$/$PWM0_L$/PLAO[7]	General-Purpose Input and Output Port 2.2/External Memory Read Strobe/PWM Phase 0 Low-Side Output/Programmable Logic Array Output Element 7.
51	P1.7/SPM7/PLAO[0]	Serial Port Multiplexed. General-Purpose Input and Output Port 1.7/UART, SPI/Programmable Logic Array Output Element 0.
52	P1.6/SPM6/PLAI[6]	Serial Port Multiplexed. General-Purpose Input and Output Port 1.6/UART, SPI/Programmable Logic Array Input Element 6.
53	IOGND	Ground for GPIO (see Table 78). Typically connected to DGND.
54	IOV_{DD}	3.3 V Supply for GPIO (see Table 78) and Input of the On-Chip Voltage Regulator.
55	P4.0/AD8/PLAO[8]	General-Purpose Input and Output Port 4.0/External Memory Interface/Programmable Logic Array Output Element 8.
56	P4.1/AD9/PLAO[9]	General-Purpose Input and Output Port 4.1/External Memory Interface/Programmable Logic Array Output Element 9.
57	P1.5/SPM5/PLAI[5]/IRQ3	Serial Port Multiplexed. General-Purpose Input and Output Port 1.5/UART, SPI/Programmable Logic Array Input Element 5/External Interrupt Request 3, Active High.
58	P1.4/SPM4/PLAI[4]/IRQ2	Serial Port Multiplexed. General-Purpose Input and Output Port 1.4/UART, SPI/Programmable Logic Array Input Element 4/External Interrupt Request 2, Active High.
59	P1.3/SPM3/PLAI[3]	Serial Port Multiplexed. General-Purpose Input and Output Port 1.3/UART, I2C1/Programmable Logic Array Input Element 3.
60	P1.2/SPM2/PLAI[2]	Serial Port Multiplexed. General-Purpose Input and Output Port 1.2/UART, I2C1/Programmable Logic Array Input Element 2.
61	P1.1/SPM1/PLAI[1]	Serial Port Multiplexed. General-Purpose Input and Output Port 1.1/UART, I2C0/Programmable Logic Array Input Element 1.
62	P1.0/T1/SPM0/PLAI[0]	Serial Port Multiplexed. General-Purpose Input and Output Port 1.0/Timer1 Input/UART, I2C0/ Programmable Logic Array Input Element 0.
63	P4.2/AD10/PLAO[10]	General-Purpose Input and Output Port 4.2/External Memory Interface/Programmable Logic Array Output Element 10.
64	P4.3/AD11/PLAO[11]	General-Purpose Input and Output Port 4.3/External Memory Interface/Programmable Logic Array Output Element 11.
65	P4.4/AD12/PLAO[12]	General-Purpose Input and Output Port 4.4/External Memory Interface/Programmable Logic Array Output Element 12.
66	P4.5/AD13/PLAO[13]	General-Purpose Input and Output Port 4.5/External Memory Interface/Programmable Logic Array Output Element 13.
67	REFGND	Ground for the Reference. Typically connected to AGND.
68	V_{REF}	2.5 V Internal Voltage Reference. Must be connected to a 0.47 µF capacitor when using the internal reference.
69	DAC_{REF}	External Voltage Reference for the DACs. Range: DACGND to $DACV_{DD}$.
70	DACGND	Ground for the DAC. Typically connected to AGND.
71, 72	AGND	Analog Ground. Ground reference point for the analog circuitry.
73, 74	AV_{DD}	3.3 V Analog Power.
75	$DACV_{DD}$	3.3 V Power Supply for the DACs. Must be connected to AV_{DD}.
76	ADC11	Single-Ended or Differential Analog Input 11.
77	ADC0	Single-Ended or Differential Analog Input 0.
78	ADC1	Single-Ended or Differential Analog Input 1.
79	ADC2/CMP0	Single-Ended or Differential Analog Input 2/Comparator Positive Input.
80	ADC3/CMP1	Single-Ended or Differential Analog Input 3/Comparator Negative Input.

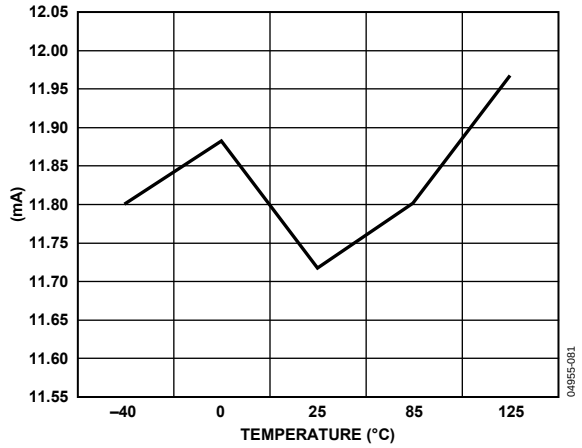

Figure 40. Current Consumption vs. Temperature @ CD = 3

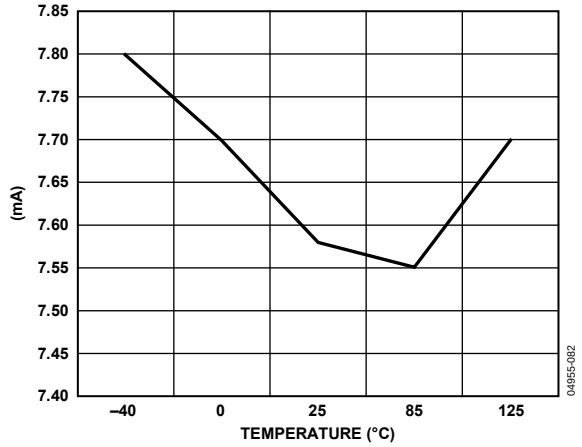

Figure 41. Current Consumption vs. Temperature @ CD = 7

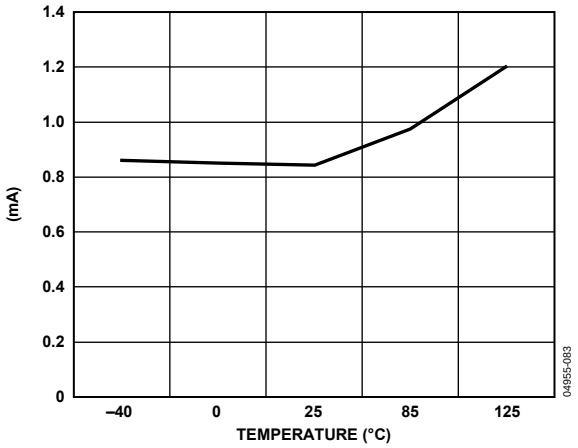

Figure 42. Current Consumption vs. Temperature in Sleep Mode

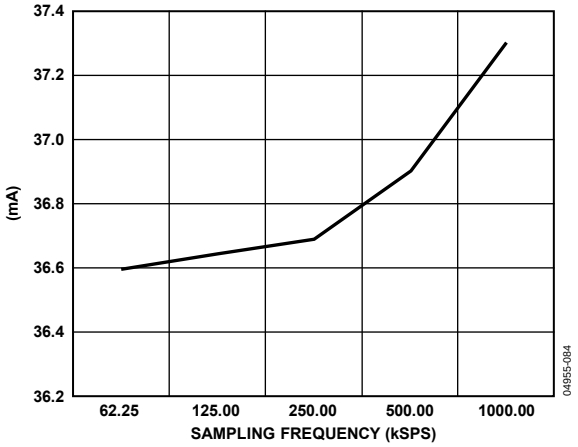

Figure 43. Current Consumption vs. Sampling Frequency

MEMORY ORGANIZATION

The ADuC7019/20/21/22/24/25/26/27/28/29 incorporate two separate blocks of memory: 8 kB of SRAM and 64 kB of on-chip Flash/EE memory. The 62 kB of on-chip Flash/EE memory is available to the user, and the remaining 2 kB are reserved for the factory-configured boot page. These two blocks are mapped as shown in Figure 45.

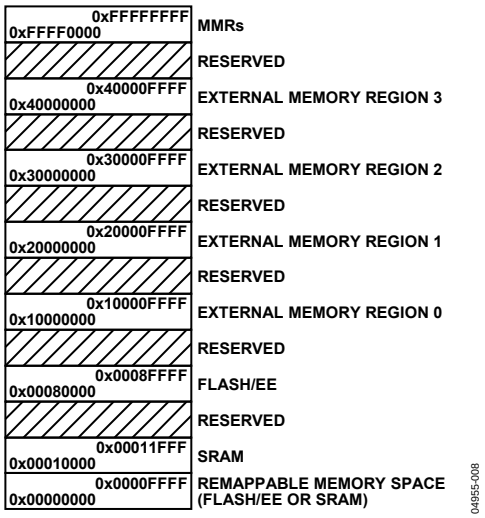

Figure 45. Physical Memory Map

Note that by default, after a reset, the Flash/EE memory is mirrored at Address 0x00000000. It is possible to remap the SRAM at Address 0x00000000 by clearing Bit 0 of the REMAP MMR. This remap function is described in more detail in the Flash/EE Memory section.

MEMORY ACCESS

The ARM7 core sees memory as a linear array of a 2^{32} byte location where the different blocks of memory are mapped as outlined in Figure 45.

The ADuC7019/20/21/22/24/25/26/27/28/29 memory organizations are configured in little endian format, which means that the least significant byte is located in the lowest byte address, and the most significant byte is in the highest byte address.

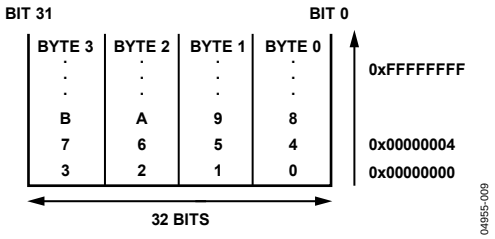

Figure 46. Little Endian Format

FLASH/EE MEMORY

The total 64 kB of Flash/EE memory is organized as 32 k × 16 bits; 31 k × 16 bits is user space and 1 k × 16 bits is reserved for the on-chip kernel. The page size of this Flash/EE memory is 512 bytes.

Sixty-two kilobytes of Flash/EE memory are available to the user as code and nonvolatile data memory. There is no distinction between data and program because ARM code shares the same space. The real width of the Flash/EE memory is 16 bits, which means that in ARM mode (32-bit instruction), two accesses to the Flash/EE are necessary for each instruction fetch. It is therefore recommended to use thumb mode when executing from Flash/EE memory for optimum access speed. The maximum access speed for the Flash/EE memory is 41.78 MHz in thumb mode and 20.89 MHz in full ARM mode. More details about Flash/EE access time are outlined in the Execution Time from SRAM and Flash/EE section.

SRAM

Eight kilobytes of SRAM are available to the user, organized as 2 k × 32 bits, that is, two words. ARM code can run directly from SRAM at 41.78 MHz, given that the SRAM array is configured as a 32-bit wide memory array. More details about SRAM access time are outlined in the Execution Time from SRAM and Flash/EE section.

MEMORY MAPPED REGISTERS

The memory mapped register (MMR) space is mapped into the upper two pages of the memory array and accessed by indirect addressing through the ARM7 banked registers.

The MMR space provides an interface between the CPU and all on-chip peripherals. All registers, except the core registers, reside in the MMR area. All shaded locations shown in Figure 47 are unoccupied or reserved locations and should not be accessed by user software. Table 16 shows the full MMR memory map.

The access time for reading from or writing to an MMR depends on the advanced microcontroller bus architecture (AMBA) bus used to access the peripheral. The processor has two AMBA buses: the advanced high performance bus (AHB) used for system modules and the advanced peripheral bus (APB) used for lower performance peripheral. Access to the AHB is one cycle, and access to the APB is two cycles. All peripherals on the ADuC7019/20/21/22/24/25/26/27/28/29 are on the APB except the Flash/EE memory, the GPIOs (see Table 78), and the PWM.

ADC CIRCUIT OVERVIEW

The analog-to-digital converter (ADC) incorporates a fast, multichannel, 12-bit ADC. It can operate from 2.7 V to 3.6 V supplies and is capable of providing a throughput of up to 1 MSPS when the clock source is 41.78 MHz. This block provides the user with a multichannel multiplexer, a differential track-and-hold, an on-chip reference, and an ADC.

The ADC consists of a 12-bit successive approximation converter based around two capacitor DACs. Depending on the input signal configuration, the ADC can operate in one of three modes.

- Fully differential mode, for small and balanced signals
- Single-ended mode, for any single-ended signals
- Pseudo differential mode, for any single-ended signals, taking advantage of the common-mode rejection offered by the pseudo differential input

The converter accepts an analog input range of 0 V to V_{REF} when operating in single-ended or pseudo differential mode. In fully differential mode, the input signal must be balanced around a common-mode voltage (V_{CM}) in the 0 V to AV_{DD} range with a maximum amplitude of 2 V_{REF} (see Figure 48).

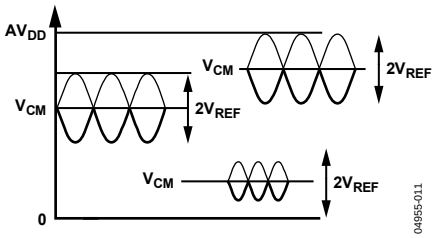

Figure 48. Examples of Balanced Signals in Fully Differential Mode

A high precision, low drift, factory calibrated, 2.5 V reference is provided on-chip. An external reference can also be connected as described in the Band Gap Reference section.

Single or continuous conversion modes can be initiated in the software. An external $\overline{CONV_{START}}$ pin, an output generated from the on-chip PLA, or a Timer0 or Timer1 overflow can also be used to generate a repetitive trigger for ADC conversions.

A voltage output from an on-chip band gap reference proportional to absolute temperature can also be routed through the front-end ADC multiplexer, effectively an additional ADC channel input. This facilitates an internal temperature sensor channel that measures die temperature to an accuracy of ±3°C.

TRANSFER FUNCTION

Pseudo Differential and Single-Ended Modes

In pseudo differential or single-ended mode, the input range is 0 V to V_{REF}. The output coding is straight binary in pseudo differential and single-ended modes with

1 LSB = *FS*/4096, or
2.5 V/4096 = 0.61 mV, or
610 µV when V_{REF} = 2.5 V

The ideal code transitions occur midway between successive integer LSB values (that is, 1/2 LSB, 3/2 LSB, 5/2 LSB, … , FS – 3/2 LSB). The ideal input/output transfer characteristic is shown in Figure 49.

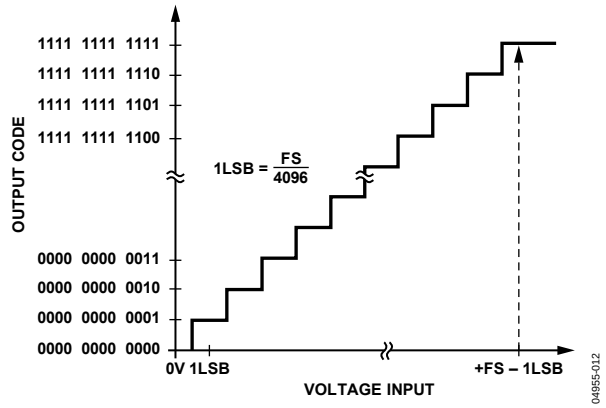

Figure 49. ADC Transfer Function in Pseudo Differential or Single-Ended Mode

Fully Differential Mode

The amplitude of the differential signal is the difference between the signals applied to the V_{IN+} and V_{IN-} input voltage pins (that is, $V_{IN+} - V_{IN-}$). The maximum amplitude of the differential signal is, therefore, $-V_{REF}$ to $+V_{REF}$ p-p (that is, $2 \times V_{REF}$). This is regardless of the common mode (CM). The common mode is the average of the two signals, for example, $(V_{IN+} + V_{IN-})/2$, and is, therefore, the voltage that the two inputs are centered on. This results in the span of each input being CM ± $V_{REF}/2$. This voltage has to be set up externally, and its range varies with V_{REF} (see the Driving the Analog Inputs section).

The output coding is twos complement in fully differential mode with 1 LSB = 2 $V_{REF}/4096$ or 2 × 2.5 V/4096 = 1.22 mV when V_{REF} = 2.5 V. The output result is ±11 bits, but this is shifted by 1 to the right. This allows the result in ADCDAT to be declared as a signed integer when writing C code. The designed code transitions occur midway between successive integer LSB values (that is, 1/2 LSB, 3/2 LSB, 5/2 LSB, … , FS – 3/2 LSB). The ideal input/output transfer characteristic is shown in Figure 50.

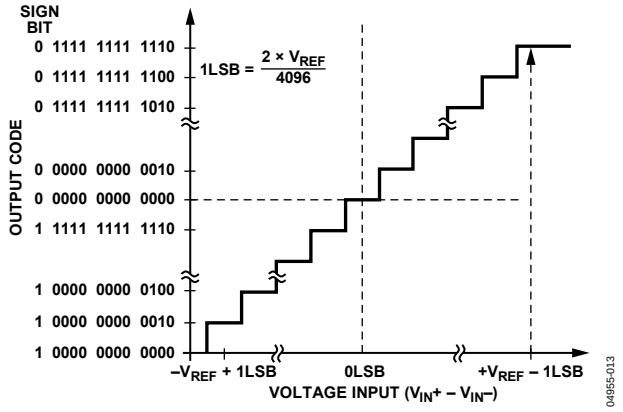

Figure 50. ADC Transfer Function in Differential Mode

Table 22. ADCCN MMR Bit Designation

Bit	Value	Description
7:5		Reserved.
4:0		Negative channel selection bits.
	00000	ADC0.
	00001	ADC1.
	00010	ADC2.
	00011	ADC3.
	00100	ADC4.
	00101	ADC5.
	00110	ADC6.
	00111	ADC7.
	01000	ADC8.
	01001	ADC9.
	01010	ADC10.
	01011	ADC11.
	01100	DAC0/ADC12.
	01101	DAC1/ADC13.
	01110	DAC2/ADC14.
	01111	DAC3/ADC15.
	10000	Internal reference (self-diagnostic feature).
	Others	Reserved.

Table 23. ADCSTA Register

Name	Address	Default Value	Access
ADCSTA	0xFFFF050C	0x00	R

ADCSTA is an ADC status register that indicates when an ADC conversion result is ready. The ADCSTA register contains only one bit, ADCReady (Bit 0), representing the status of the ADC. This bit is set at the end of an ADC conversion, generating an ADC interrupt. It is cleared automatically by reading the ADCDAT MMR. When the ADC is performing a conversion, the status of the ADC can be read externally via the ADC_{BUSY} pin. This pin is high during a conversion. When the conversion is finished, ADC_{BUSY} goes back low. This information can be available on P0.5 (see the General-Purpose Input/Output section) if enabled in the ADCCON register.

Table 24. ADCDAT Register

Name	Address	Default Value	Access
ADCDAT	0xFFFF0510	0x00000000	R

ADCDAT is an ADC data result register. It holds the 12-bit ADC result as shown in Figure 51.

Table 25. ADCRST Register

Name	Address	Default Value	Access
ADCRST	0xFFFF0514	0x00	R/W

ADCRST resets the digital interface of the ADC. Writing any value to this register resets all the ADC registers to their default values.

Table 26. ADCGN Register

Name	Address	Default Value	Access
ADCGN	0xFFFF0530	0x0200	R/W

ADCGN is a 10-bit gain calibration register.

Table 27. ADCOF Register

Name	Address	Default Value	Access
ADCOF	0xFFFF0534	0x0200	R/W

ADCOF is a 10-bit offset calibration register.

CONVERTER OPERATION

The ADC incorporates a successive approximation (SAR) architecture involving a charge-sampled input stage. This architecture can operate in three modes: differential, pseudo differential, and single-ended.

Differential Mode

The ADuC7019/20/21/22/24/25/26/27/28/29 each contain a successive approximation ADC based on two capacitive DACs. Figure 54 and Figure 55 show simplified schematics of the ADC in acquisition and conversion phase, respectively. The ADC comprises control logic, a SAR, and two capacitive DACs. In Figure 54 (the acquisition phase), SW3 is closed and SW1 and SW2 are in Position A. The comparator is held in a balanced condition, and the sampling capacitor arrays acquire the differential signal on the input.

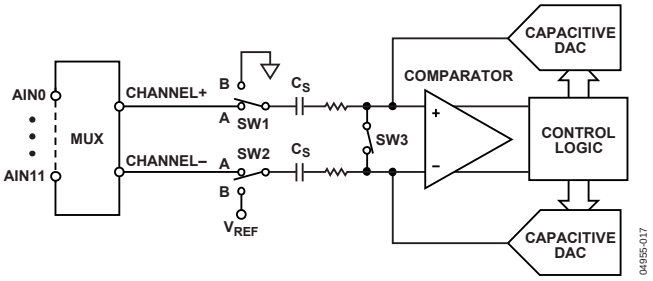

Figure 54. ADC Acquisition Phase

When the ADC starts a conversion, as shown in Figure 55, SW3 opens, and then SW1 and SW2 move to Position B. This causes the comparator to become unbalanced. Both inputs are disconnected once the conversion begins. The control logic and the charge redistribution DACs are used to add and subtract fixed amounts of charge from the sampling capacitor arrays to bring the comparator back into a balanced condition. When the comparator is rebalanced, the conversion is complete. The control logic generates the ADC output code. The output impedances of the sources driving the V_{IN+} and V_{IN-} input voltage pins must be matched; otherwise, the two inputs have different settling times, resulting in errors.

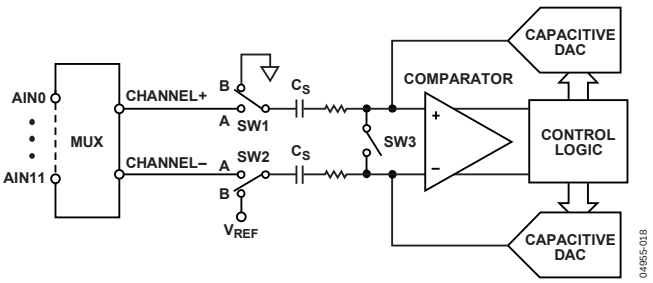

Figure 55. ADC Conversion Phase

Table 28. V_{CM} Ranges

AV_{DD}	V_{REF}	V_{CM} Min	V_{CM} Max	Signal Peak-to-Peak
3.3 V	2.5 V	1.25 V	2.05 V	2.5 V
	2.048 V	1.024 V	2.276 V	2.048 V
	1.25 V	0.75 V	2.55 V	1.25 V
3.0 V	2.5 V	1.25 V	1.75 V	2.5 V
	2.048 V	1.024 V	1.976 V	2.048 V
	1.25 V	0.75 V	2.25 V	1.25 V

CALIBRATION

By default, the factory-set values written to the ADC offset (ADCOF) and gain coefficient registers (ADCGN) yield optimum performance in terms of end-point errors and linearity for standalone operation of the part (see the Specifications section). If system calibration is required, it is possible to modify the default offset and gain coefficients to improve end-point errors, but note that any modification to the factory-set ADCOF and ADCGN values can degrade ADC linearity performance.

For system offset error correction, the ADC channel input stage must be tied to AGND. A continuous software ADC conversion loop must be implemented by modifying the value in ADCOF until the ADC result (ADCDAT) reads Code 0 to Code 1. If the ADCDAT value is greater than 1, ADCOF should be decremented until ADCDAT reads 0 to 1. Offset error correction is done digitally and has a resolution of 0.25 LSB and a range of ±3.125% of V_{REF}.

For system gain error correction, the ADC channel input stage must be tied to V_{REF}. A continuous software ADC conversion loop must be implemented to modify the value in ADCGN until the ADC result (ADCDAT) reads Code 4094 to Code 4095. If the ADCDAT value is less than 4094, ADCGN should be incremented until ADCDAT reads 4094 to 4095. Similar to the offset calibration, the gain calibration resolution is 0.25 LSB with a range of ±3% of V_{REF}.

TEMPERATURE SENSOR

The ADuC7019/20/21/22/24/25/26/27/28/29 provide voltage output from on-chip band gap references proportional to absolute temperature. This voltage output can also be routed through the front-end ADC multiplexer (effectively an additional ADC channel input) facilitating an internal temperature sensor channel, measuring die temperature to an accuracy of ±3°C.

The following is an example routine showing how to use the internal temperature sensor:

```
int main(void)
{
float a = 0;
      short b;
      ADCCON = 0x20;    // power-on the ADC
      delay(2000);
      ADCCP = 0x10;  // Select Temperature
Sensor as an // input to the ADC
      REFCON = 0x01; // connect internal 2.5V
reference // to Vref pin
      ADCCON = 0xE4; // continuous conversion
      while(1)
      {
              while (!ADCSTA){};
      // wait for end of conversion
              b = (ADCDAT >> 16);
      // To calculate temperature in °C, use
the formula:
              a = 0x525 - b;
      // ((Temperature = 0x525 - Sensor
Voltage) / 1.3)
              a /= 1.3;
              b = floor(a);
              printf("Temperature: %d
oC\n",b);
      }
      return 0;
}
```

BAND GAP REFERENCE

Each ADuC7019/20/21/22/24/25/26/27/28/29 provides an on-chip band gap reference of 2.5 V, which can be used for the ADC and DAC. This internal reference also appears on the V_{REF} pin. When using the internal reference, a 0.47 µF capacitor must be connected from the external V_{REF} pin to AGND to ensure stability and fast response during ADC conversions. This reference can also be connected to an external pin (V_{REF}) and used as a reference for other circuits in the system. An external buffer is required because of the low drive capability of the V_{REF} output. A programmable option also allows an external reference input on the V_{REF} pin. Note that it is not possible to disable the internal reference. Therefore, the external reference source must be capable of overdriving the internal reference source.

Table 29. REFCON Register

Name	Address	Default Value	Access
REFCON	0xFFFF048C	0x00	R/W

The band gap reference interface consists of an 8-bit MMR REFCON, described in Table 30.

Table 30. REFCON MMR Bit Designations

Bit	Description
7:1	Reserved.
0	Internal reference output enable. Set by user to connect the internal 2.5 V reference to the V_{REF} pin. The reference can be used for an external component but must be buffered. Cleared by user to disconnect the reference from the V_{REF} pin.

Example source code

```
    t2val_old= T2VAL;
     T2LD = 5;
     TCON = 0x480;


  while ((T2VAL == t2val_old) || (T2VAL >
3)) //ensures timer value loaded
  IRQEN = 0x10;
//enable T2 interrupt
  PLLKEY1 = 0xAA;
  PLLCON = 0x01;
  PLLKEY2 = 0x55;

  POWKEY1 = 0x01;
  POWCON = 0x27;
// Set Core into Nap mode
  POWKEY2 = 0xF4;
```

In noisy environments, noise can couple to the external crystal pins, and PLL may lose lock momentarily. A PLL interrupt is provided in the interrupt controller. The core clock is immediately halted, and this interrupt is only serviced when the lock is restored.

In case of crystal loss, the watchdog timer should be used. During initialization, a test on the RSTSTA register can determine if the reset came from the watchdog timer.

External Clock Selection

To switch to an external clock on P0.7, configure P0.7 in Mode 1. The external clock can be up to 44 MHz, providing the tolerance is 1%.

Example source code

```
    t2val_old= T2VAL;
     T2LD = 5;
     TCON = 0x480;


  while ((T2VAL == t2val_old) || (T2VAL
> 3)) //ensures timer value loaded
  IRQEN = 0x10;
//enable T2 interrupt
  PLLKEY1 = 0xAA;
  PLLCON = 0x03; //Select external clock
  PLLKEY2 = 0x55;

  POWKEY1 = 0x01;
  POWCON = 0x27;
// Set Core into Nap mode
  POWKEY2 = 0xF4;
```

Power Control System

A choice of operating modes is available on the ADuC7019/20/21/22/24/25/26/27/28/29. Table 57 describes what part is powered on in the different modes and indicates the power-up time.

Table 58 gives some typical values of the total current consumption (analog + digital supply currents) in the different modes, depending on the clock divider bits. The ADC is turned off. Note that these values also include current consumption of the regulator and other parts on the test board where these values are measured.

Table 57. Operating Modes[1]

Mode	Core	Peripherals	PLL	XTAL/T2/T3	IRQ0 to IRQ3	Start-Up/Power-On Time
Active	X	X	X	X	X	130 ms at CD = 0
Pause		X	X	X	X	24 ns at CD = 0; 3 µs at CD = 7
Nap			X	X	X	24 ns at CD = 0; 3 µs at CD = 7
Sleep				X	X	1.58 ms
Stop					X	1.7 ms

[1] X indicates that the part is powered on.

Table 58. Typical Current Consumption at 25°C in Milliamperes

PC[2:0]	Mode	CD = 0	CD = 1	CD = 2	CD = 3	CD = 4	CD = 5	CD = 6	CD = 7
000	Active	33.1	21.2	13.8	10	8.1	7.2	6.7	6.45
001	Pause	22.7	13.3	8.5	6.1	4.9	4.3	4	3.85
010	Nap	3.8	3.8	3.8	3.8	3.8	3.8	3.8	3.8
011	Sleep	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4
100	Stop	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4

DIGITAL PERIPHERALS

3-PHASE PWM

Each ADuC7019/20/21/22/24/25/26/27/28/29 provides a flexible and programmable, 3-phase pulse-width modulation (PWM) waveform generator. It can be programmed to generate the required switching patterns to drive a 3-phase voltage source inverter for ac induction motor control (ACIM). Note that only active high patterns can be produced.

The PWM generator produces three pairs of PWM signals on the six PWM output pins ($PWM0_H$, $PWM0_L$, $PWM1_H$, $PWM1_L$, $PWM2_H$, and $PWM2_L$). The six PWM output signals consist of three high-side drive signals and three low-side drive signals.

The switching frequency and dead time of the generated PWM patterns are programmable using the PWMDAT0 and PWMDAT1 MMRs. In addition, three duty-cycle control registers (PWMCH0, PWMCH1, and PWMCH2) directly control the duty cycles of the three pairs of PWM signals.

Each of the six PWM output signals can be enabled or disabled by separate output enable bits of the PWMEN register. In addition, three control bits of the PWMEN register permit crossover of the two signals of a PWM pair. In crossover mode, the PWM signal destined for the high-side switch is diverted to the complementary low-side output. The signal destined for the low-side switch is diverted to the corresponding high-side output signal.

In many applications, there is a need to provide an isolation barrier in the gate-drive circuits that turn on the inverter power devices. In general, there are two common isolation techniques: optical isolation using optocouplers and transformer isolation using pulse transformers. The PWM controller permits mixing of the output PWM signals with a high frequency chopping signal to permit easy interface to such pulse transformers. The features of this gate-drive chopping mode can be controlled by the PWMCFG register. An 8-bit value within the PWMCFG register directly controls the chopping frequency. High frequency chopping can be independently enabled for the high-side and low-side outputs using separate control bits in the PWMCFG register.

The PWM generator can operate in one of two distinct modes: single update mode or double update mode. In single update mode, the duty cycle values are programmable only once per PWM period so that the resulting PWM patterns are symmetrical about the midpoint of the PWM period. In the double update mode, a second updating of the PWM duty cycle values is implemented at the midpoint of the PWM period.

In double update mode, it is also possible to produce asymmetrical PWM patterns that produce lower harmonic distortion in 3-phase PWM inverters. This technique permits closed-loop controllers to change the average voltage applied to the machine windings at a faster rate. As a result, faster closed-loop bandwidths are achieved. The operating mode of the PWM block is selected by a control bit in the PWMCON register. In single update mode, an internal synchronization pulse, PWMSYNC, is produced at the start of each PWM period. In double update mode, an additional PWMSYNC pulse is produced at the midpoint of each PWM period.

The PWM block can also provide an internal synchronization pulse on the PWM_{SYNC} pin that is synchronized to the PWM switching frequency. In single update mode, a pulse is produced at the start of each PWM period. In double update mode, an additional pulse is produced at the mid-point of each PWM period. The width of the pulse is programmable through the PWMDAT2 register. The PWM block can also accept an external synchronization pulse on the PWM_{SYNC} pin. The selection of external synchronization or internal synchronization is in the PWMCON register. The SYNC input timing can be synchronized to the internal peripheral clock, which is selected in the PWMCON register. If the external synchronization pulse from the chip pin is asynchronous to the internal peripheral clock (typical case), the external PWMSYNC is considered asynchronous and should be synchronized. The synchronization logic adds latency and jitter from the external pulse to the actual PWM outputs. The size of the pulse on the PWM_{SYNC} pin must be greater than two core clock periods.

The PWM signals produced by the ADuC7019/20/21/22/24/25/26/27/28/29 can be shut off via a dedicated asynchronous PWM shutdown pin, PWM_{TRIP}. When brought low, PWM_{TRIP} instantaneously places all six PWM outputs in the off state (high). This hardware shutdown mechanism is asynchronous so that the associated PWM disable circuitry does not go through any clocked logic. This ensures correct PWM shutdown even in the event of a core clock loss.

Status information about the PWM system is available to the user in the PWMSTA register. In particular, the state of the PWM_{TRIP} pin is available, as well as a status bit that indicates whether operation is in the first half or the second half of the PWM period.

40-Pin Package Devices

On the 40-pin package devices, the PWM outputs are not directly accessible, as described in the General-Purpose Input/Output section. One channel can be brought out on a GPIO (see Table 78) via the PLA as shown in the following example:

```
PWMCON = 0x1;           // enables PWM o/p
PWMDAT0 = 0x055F;       // PWM switching freq
// Configure Port Pins
GP4CON = 0x300;         // P4.2 as PLA output
GP3CON = 0x1;           // P3.0 configured as
                        // output of PWM0
                        //(internally)
// PWM0 onto P4.2
PLAELM8 = 0x0035;       // P3.0 (PWM output)
                        // input of element 8
PLAELM10 = 0x0059;      // PWM from element 8
```

Table 116. COMIID1 MMR Bit Descriptions

Bit 3:1 Status Bits	Bit 0 NINT	Priority	Definition	Clearing Operation
000	1		No interrupt	
110	0	2	Matching network address	Read COMRX
101	0	3	Address transmitted, buffer empty	Write data to COMTX or read COMIID0
011	0	1	Receive line status interrupt	Read COMSTA0
010	0	2	Receive buffer full interrupt	Read COMRX
001	0	3	Transmit buffer empty interrupt	Write data to COMTX or read COMIID0
000	0	4	Modem status interrupt	Read COMSTA1

Note that to receive a network address interrupt, the slave must ensure that Bit 0 of COMIEN0 (enable receive buffer full interrupt) is set to 1.

Table 117. COMADR Register

Name	Address	Default Value	Access
COMADR	0xFFFF0728	0xAA	R/W

COMADR is an 8-bit, read/write network address register that holds the address checked for by the network addressable UART. Upon receiving this address, the device interrupts the processor and/or sets the appropriate status bit in COMIID1.

SERIAL PERIPHERAL INTERFACE

The ADuC7019/20/21/22/24/25/26/27/28/29 integrate a complete hardware serial peripheral interface (SPI) on-chip. SPI is an industry standard, synchronous serial interface that allows eight bits of data to be synchronously transmitted and simultaneously received, that is, full duplex up to a maximum bit rate of 3.48 Mb, as shown in Table 118. The SPI interface is not operational with core clock divider (CD) bits. POWCON[2:0] = 6 or 7 in master mode.

The SPI port can be configured for master or slave operation. and typically consists of four pins: MISO (P1.5), MOSI (P1.6), SCLK (P1.4), and $\overline{CS}$ (P1.7).

On the transmit side, the SPITX register (and a TX shift register outside it) loads data onto the transmit pin (in slave mode, MISO; in master mode, MOSI). The transmit status bit, Bit 0, in SPISTA indicates whether there is valid data in the SPITX register.

Similarly, the receive data path consists of the SPIRX register (and an RX shift register). SPISTA, Bit 3 indicates whether there is valid data in the SPIRX register. If valid data in the SPIRX register is overwritten or if valid data in the RX shift register is discarded, SPISTA, Bit 5 (the overflow bit) is set.

MISO (Master In, Slave Out) Pin

The MISO pin is configured as an input line in master mode and an output line in slave mode. The MISO line on the master (data in) should be connected to the MISO line in the slave device (data out). The data is transferred as byte wide (8-bit) serial data, MSB first.

MOSI (Master Out, Slave In) Pin

The MOSI pin is configured as an output line in master mode and an input line in slave mode. The MOSI line on the master (data out) should be connected to the MOSI line in the slave device (data in). The data is transferred as byte wide (8-bit) serial data, MSB first.

SCLK (Serial Clock I/O) Pin

The master serial clock (SCLK) is used to synchronize the data being transmitted and received through the MOSI SCLK period. Therefore, a byte is transmitted/received after eight SCLK periods. The SCLK pin is configured as an output in master mode and as an input in slave mode.

In master mode, the polarity and phase of the clock are controlled by the SPICON register, and the bit rate is defined in the SPIDIV register as follows:

$$f_{SERIAL\,CLOCK} = \frac{f_{UCLK}}{2\times(1+SPIDIV)}$$

The maximum speed of the SPI clock is dependent on the clock divider bits and is summarized in Table 118.

Table 118. SPI Speed vs. Clock Divider Bits in Master Mode

CD Bits	0	1	2	3	4	5
SPIDIV in Hex	0x05	0x0B	0x17	0x2F	0x5F	0xBF
SPI dpeed in MHz	3.482	1.741	0.870	0.435	0.218	0.109

In slave mode, the SPICON register must be configured with the phase and polarity of the expected input clock. The slave accepts data from an external master up to 10.4 Mb at CD = 0. The formula to determine the maximum speed is as follows:

$$f_{SERIAL\,CLOCK} = \frac{f_{HCLK}}{4}$$

In both master and slave modes, data is transmitted on one edge of the SCL signal and sampled on the other. Therefore, it is important that the polarity and phase be configured the same for the master and slave devices.

Chip Select ($\overline{CS}$ Input) Pin

In SPI slave mode, a transfer is initiated by the assertion of $\overline{CS}$, which is an active low input signal. The SPI port then transmits and receives 8-bit data until the transfer is concluded by deassertion of $\overline{CS}$. In slave mode, $\overline{CS}$ is always an input.

Table 148. PLACLK Register

Name	Address	Default Value	Access
PLACLK	0xFFFF0B40	0x00	R/W

PLACLK is the clock selection for the flip-flops of Block 0 and Block 1. Note that the maximum frequency when using the GPIO pins as the clock input for the PLA blocks is 44 MHz.

Table 149. PLACLK MMR Bit Descriptions

Bit	Value	Description
7		Reserved.
6:4		Block 1 clock source selection.
	000	GPIO clock on P0.5.
	001	GPIO clock on P0.0.
	010	GPIO clock on P0.7.
	011	HCLK.
	100	OCLK (32.768 kHz) external crystal only.
	101	Timer1 overflow.
	Other	Reserved.
3		Reserved.
2:0		Block 0 clock source selection.
	000	GPIO clock on P0.5.
	001	GPIO clock on P0.0.
	010	GPIO clock on P0.7.
	011	HCLK.
	100	OCLK (32.768 kHz) external crystal only.
	101	Timer1 overflow.
	Other	Reserved.

Table 150. PLAIRQ Register

Name	Address	Default Value	Access
PLAIRQ	0xFFFF0B44	0x00000000	R/W

PLAIRQ enables IRQ0 and/or IRQ1 and selects the source of the IRQ.

Table 151. PLAIRQ MMR Bit Descriptions

Bit	Value	Description
15:13		Reserved.
12		PLA IRQ1 enable bit. Set by user to enable IRQ1 output from PLA. Cleared by user to disable IRQ1 output from PLA.
11:8		PLA IRQ1 source.
	0000	PLA Element 0.
	0001	PLA Element 1.
	1111	PLA Element 15.
7:5		Reserved.
4		PLA IRQ0 enable bit. Set by user to enable IRQ0 output from PLA. Cleared by user to disable IRQ0 output from PLA.
3:0		PLA IRQ0 source.
	0000	PLA Element 0.
	0001	PLA Element 1.
	1111	PLA Element 15.

Table 152. Feedback Configuration

Bit	Value	PLAELM0	PLAELM1 to PLAELM7	PLAELM8	PLAELM9 to PLAELM15
10:9	00	Element 15	Element 0	Element 7	Element 8
	01	Element 2	Element 2	Element 10	Element 10
	10	Element 4	Element 4	Element 12	Element 12
	11	Element 6	Element 6	Element 14	Element 14
8:7	00	Element 1	Element 1	Element 9	Element 9
	01	Element 3	Element 3	Element 11	Element 11
	10	Element 5	Element 5	Element 13	Element 13
	11	Element 7	Element 7	Element 15	Element 15

Table 191. T3CON MMR Bit Descriptions

Bit	Value	Description
15:9		Reserved.
8		Count up. Set by user for Timer3 to count up. Cleared by user for Timer3 to count down by default.
7		Timer3 enable bit. Set by user to enable Timer3. Cleared by user to disable Timer3 by default.
6		Timer3 mode. Set by user to operate in periodic mode. Cleared by user to operate in free-running mode. Default mode.
5		Watchdog mode enable bit. Set by user to enable watchdog mode. Cleared by user to disable watchdog mode by default.
4		Secure clear bit. Set by user to use the secure clear option. Cleared by user to disable the secure clear option by default.
3:2		Prescale.
	00	Source Clock/1 by default.
	01	Source Clock/16.
	10	Source Clock/256.
	11	Undefined. Equivalent to 00.
1		Watchdog IRQ option bit. Set by user to produce an IRQ instead of a reset when the watchdog reaches 0. Cleared by user to disable the IRQ option.
0		Reserved.

Table 192. T3CLRI Register

Name	Address	Default Value	Access
T3CLRI	0xFFFF036C	0x00	W

T3CLRI is an 8-bit register. Writing any value to this register on successive occassions clears the Timer3 interrupt in normal mode or resets a new timeout period in watchdog mode.

Note that the user must perform successive writes to this register to ensure resetting the timeout period.

Secure Clear Bit (Watchdog Mode Only)

The secure clear bit is provided for a higher level of protection. When set, a specific sequential value must be written to T3CLRI to avoid a watchdog reset. The value is a sequence generated by the 8-bit linear feedback shift register (LFSR) polynomial = X8 + X6 + X5 + X + 1, as shown in Figure 81.

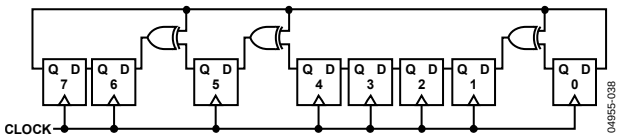

Figure 81. 8-Bit LFSR

The initial value or seed is written to T3CLRI before entering watchdog mode. After entering watchdog mode, a write to T3CLRI must match this expected value. If it matches, the LFSR is advanced to the next state when the counter reload occurs. If it fails to match the expected state, a reset is immediately generated, even if the count has not yet expired.

The value 0x00 should not be used as an initial seed due to the properties of the polynomial. The value 0x00 is always guaranteed to force an immediate reset. The value of the LFSR cannot be read; it must be tracked/generated in software.

The following is an example of a sequence:

1. Enter initial seed, 0xAA, in T3CLRI before starting Timer3 in watchdog mode.
2. Enter 0xAA in T3CLRI; Timer3 is reloaded.
3. Enter 0x37 in T3CLRI; Timer3 is reloaded.
4. Enter 0x6E in T3CLRI; Timer3 is reloaded.
5. Enter 0x66. 0xDC was expected; the watchdog resets the chip.

EXTERNAL MEMORY INTERFACING

The ADuC7026 and ADuC7027 are the only models in their series that feature an external memory interface. The external memory interface requires a larger number of pins. This is why it is only available on larger pin count packages. The XMCFG MMR must be set to 1 to use the external port.

Although 32-bit addresses are supported internally, only the lower 16 bits of the address are on external pins.

The memory interface can address up to four 128 kB blocks of asynchronous memory (SRAM or/and EEPROM).

The pins required for interfacing to an external memory are shown in Table 193.

Table 193. External Memory Interfacing Pins

Pin	Function
AD[16:1]	Address/data bus
A16	Extended addressing for 8-bit memory only
MS[3:0]	Memory select
$\overline{WS}$	Write strobe
$\overline{RS}$	Read strobe
AE	Address latch enable
$\overline{BHE}$, $\overline{BLE}$	Byte write capability

There are four external memory regions available, as described in Table 194. Associated with each region are the MS[3:0] pins. These signals allow access to the particular region of external memory. The size of each memory region can be 128 kB maximum, 64 k × 16 or 128 k × 8. To access 128 k with an 8-bit memory, an extra address line (A16) is provided (see the example in Figure 82). The four regions are configured independently.

Table 194. Memory Regions

Address Start	Address End	Contents
0x10000000	0x1000FFFF	External Memory 0
0x20000000	0x2000FFFF	External Memory 1
0x30000000	0x3000FFFF	External Memory 2
0x40000000	0x4000FFFF	External Memory 3

Each external memory region can be controlled through three MMRs: XMCFG, XMxCON, and XMxPAR.

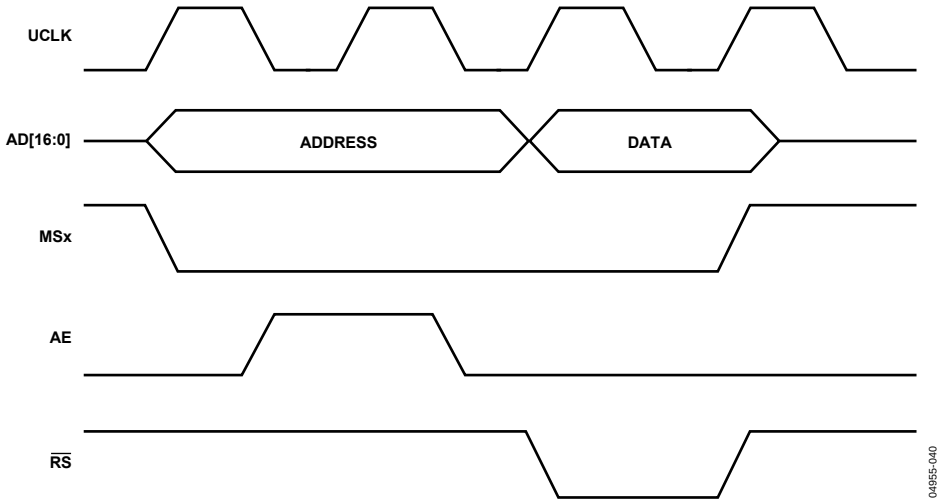

Figure 83. External Memory Read Cycle

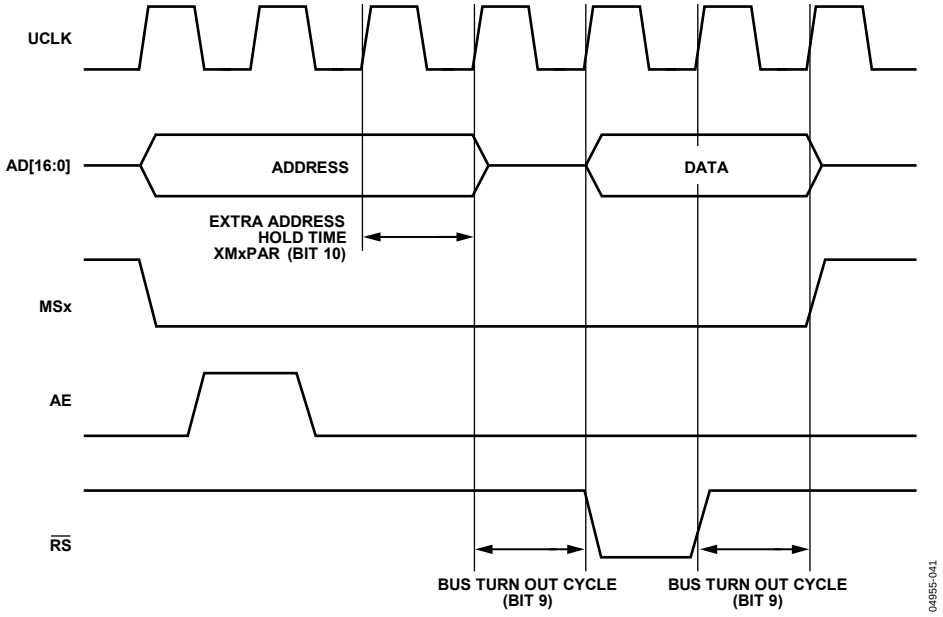

Figure 84. External Memory Read Cycle with Address Hold and Bus Turn Cycles

DEVELOPMENT TOOLS

PC-BASED TOOLS

Four types of development systems are available for the ADuC7019/20/21/22/24/25/26/27/28/29 family.

- The ADuC7026 QuickStart Plus is intended for new users who want to have a comprehensive hardware development environment. Because the ADuC7026 contains the superset of functions available on the ADuC7019/20/21/22/24/25/26/27/28/29, it is suitable for users who wish to develop on any of the parts in this family. All parts are fully code compatible.
- The ADuC7019, ADuC7024, and ADuC7026 QuickStart systems are intended for users who already have an emulator.

These systems consist of the following PC-based (Windows® compatible) hardware and software development tools.

Hardware

- ADuC7019/20/21/22/24/25/26/27/28/29 evaluation board
- Serial port programming cable
- RDI-compliant JTAG emulator (included in the ADuC7026 QuickStart Plus only)

Software

- Integrated development environment, incorporating assembler, compiler, and nonintrusive JTAG-based debugger
- Serial downloader software
- Example code

Miscellaneous

CD-ROM documentation

IN-CIRCUIT SERIAL DOWNLOADER

The serial downloader is a Windows application that allows the user to serially download an assembled program to the on-chip program Flash/EE memory via the serial port on a standard PC.

The UART-based serial downloader is included in all the development systems and is usable with the ADuC7019/20/21/22/24/25/26/27/28/29 parts that do not contain the I suffix in the Ordering Guide.

An I^2C based serial downloader and a USB-to-I^2C adaptor board, USB-EA-CONVZ, are also available at www.analog.com. The I^2C-based serial downloader is only usable with the part models containing the I suffix (see Ordering Guide).