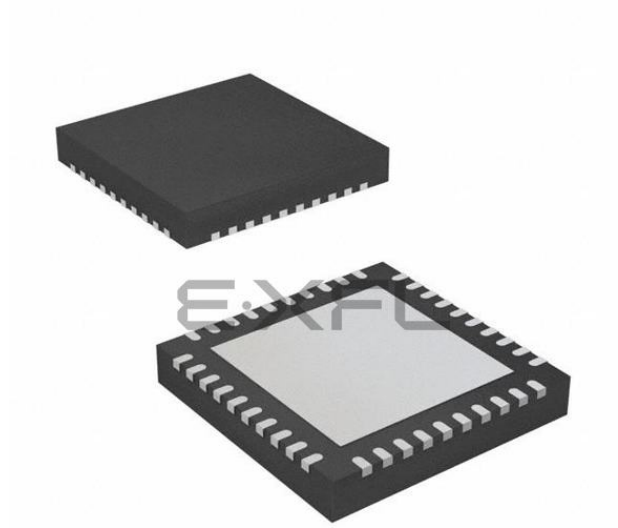


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	44MHz
Connectivity	EBI/EMI, I²C, SPI, UART/USART
Peripherals	PLA, PWM, PSM, Temp Sensor, WDT
Number of I/O	14
Program Memory Size	62KB (31K x16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 32
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 5x12b; D/A 3x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	40-VFQFN Exposed Pad, CSP
Supplier Device Package	40-LFCSP-VQ (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/aduc7019bcpz62irl7

GENERAL DESCRIPTION

The ADuC7019/20/21/22/24/25/26/27/28/29 are fully integrated, 1 MSPS, 12-bit data acquisition systems incorporating high performance multichannel ADCs, 16-bit/32-bit MCUs, and Flash®/EE memory on a single chip.

The ADC consists of up to 12 single-ended inputs. An additional four inputs are available but are multiplexed with the four DAC output pins. The four DAC outputs are available only on certain models (ADuC7020, ADuC7026, ADuC7028, and ADuC7029). However, in many cases where the DAC outputs are not present, these pins can still be used as additional ADC inputs, giving a maximum of 16 ADC input channels. The ADC can operate in single-ended or differential input mode. The ADC input voltage is 0 V to V_{REF}. A low drift band gap reference, temperature sensor, and voltage comparator complete the ADC peripheral set.

Depending on the part model, up to four buffered voltage output DACs are available on-chip. The DAC output range is programmable to one of three voltage ranges.

The devices operate from an on-chip oscillator and a PLL generating an internal high frequency clock of 41.78 MHz (UCLK). This clock is routed through a programmable clock divider from which the MCU core clock operating frequency is generated. The microcontroller core is an ARM7TDMI®, 16-bit/32-bit RISC machine, which offers up to 41 MIPS peak performance. Eight kilobytes of SRAM and 62 kilobytes of nonvolatile Flash/EE memory are provided on-chip. The ARM7TDMI core views all memory and registers as a single linear array.

On-chip factory firmware supports in-circuit serial download via the UART or I²C serial interface port; nonintrusive emulation is also supported via the JTAG interface. These features are incorporated into a low cost QuickStart™ development system supporting this MicroConverter® family.

The parts operate from 2.7 V to 3.6 V and are specified over an industrial temperature range of −40°C to +125°C. When operating at 41.78 MHz, the power dissipation is typically 120 mW. The ADuC7019/20/21/22/24/25/26/27/28/29 are available in a variety of memory models and packages (see Ordering Guide).

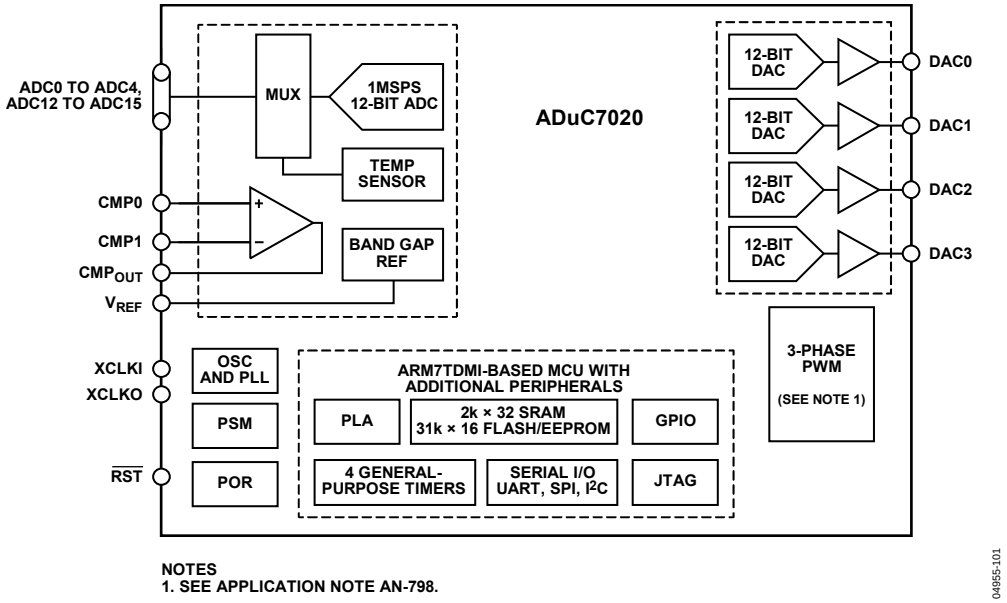


Figure 2.

Table 7. SPI Master Mode Timing (Phase Mode = 0)

Parameter	Description	Min	Typ	Max	Unit
t_{SL}	SCLK low pulse width[1]		(SPIDIV + 1) × t_{HCLK}		ns
t_{SH}	SCLK high pulse width[1]		(SPIDIV + 1) × t_{HCLK}		ns
t_{DAV}	Data output valid after SCLK edge			25	ns
t_{DOSU}	Data output setup before SCLK edge			75	ns
t_{DSU}	Data input setup time before SCLK edge[2]	1 × t_{UCLK}			ns
t_{DHD}	Data input hold time after SCLK edge[2]	2 × t_{UCLK}			ns
t_{DF}	Data output fall time		5	12.5	ns
t_{DR}	Data output rise time		5	12.5	ns
t_{SR}	SCLK rise time		5	12.5	ns
t_{SF}	SCLK fall time		5	12.5	ns

[1] t_{HCLK} depends on the clock divider or CD bits in the POWCONMMR. $t_{HCLK} = t_{UCLK}/2^{CD}$; see Figure 67.
[2] t_{UCLK} = 23.9 ns. It corresponds to the 41.78 MHz internal clock from the PLL before the clock divider; see Figure 67.

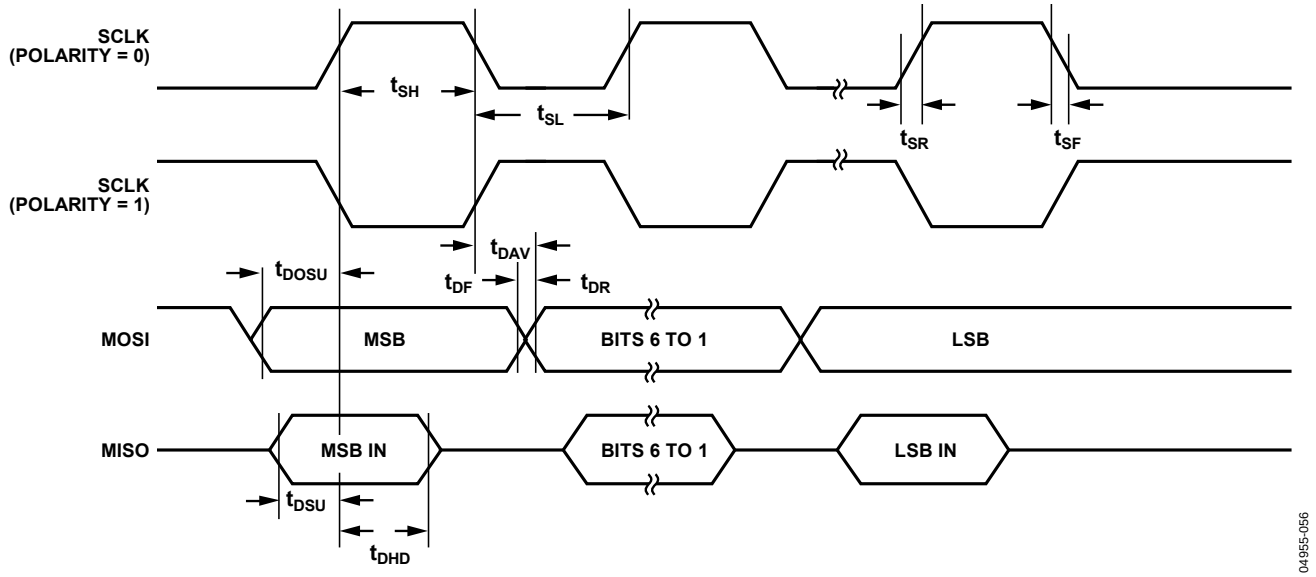
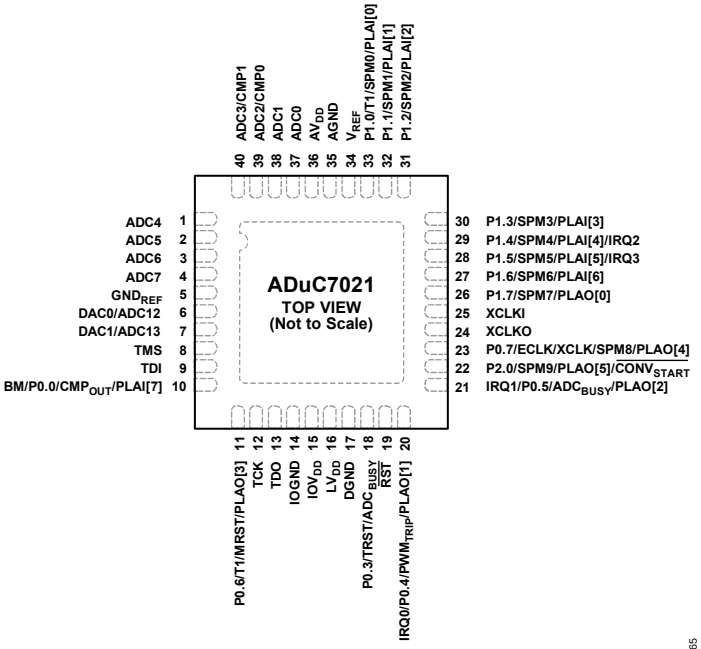


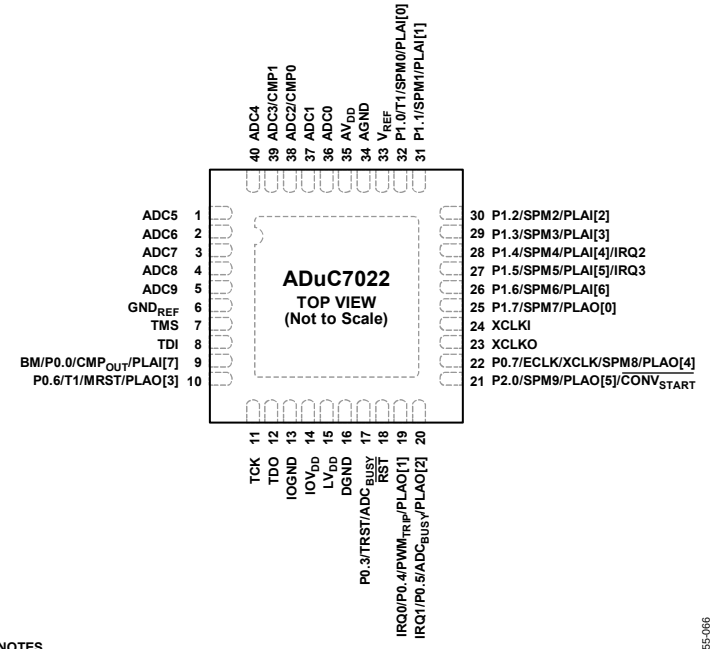
Figure 16. SPI Master Mode Timing (Phase Mode = 0)



NOTES
1. THE EXPOSED PAD MUST BE SOLDERED FOR MECHANICAL PURPOSES AND LEFT UNCONNECTED.

04955-065

Figure 21. 40-Lead LFCSP_WQ Pin Configuration (ADuC7021)



NOTES
1. THE EXPOSED PAD MUST BE SOLDERED FOR MECHANICAL PURPOSES AND LEFT UNCONNECTED.

04955-066

Figure 22. 40-Lead LFCSP_WQ Pin Configuration (ADuC7022)

Pin No.	Mnemonic	Description
D7	P1.6/SPM6/PLAI[6]	Serial Port Multiplexed. General-Purpose Input and Output Port 1.6/UART, SPI/Programmable Logic Array Input Element 6.
D8	IOV_{DD}	3.3 V Supply for GPIO (see Table 78) and Input of the On-Chip Voltage Regulator.
E1	DAC3/ADC15	DAC3 Voltage Output/ADC Input 15.
E2	DAC2/ADC14	DAC2 Voltage Output/ADC Input 14.
E3	DAC1/ADC13	DAC1 Voltage Output/ADC Input 13.
E4	P3.0/$PWM0_H$/PLAI[8]	General-Purpose Input and Output Port 3.0/PWM Phase 0 High-Side Output/Programmable Logic Array Input Element 8.
E5	P3.2/$PWM1_H$/PLAI[10]	General-Purpose Input and Output Port 3.2/PWM Phase 1 High-Side Output/Programmable Logic Array Input Element 10.
E6	P1.5/SPM5/PLAI[5]/IRQ3	Serial Port Multiplexed. General-Purpose Input and Output Port 1.5/UART, SPI/Programmable Logic Array Input Element 5/External Interrupt Request 3, Active High.
E7	P3.7/PWM_{SYNC}/PLAI[15]	General-Purpose Input and Output Port 3.7/PWM Synchronization/Programmable Logic Array Input Element 15.
E8	XCLKI	Input to the Crystal Oscillator Inverter and Input to the Internal Clock Generator Circuits.
F1	P4.6/PLAO[14]	General-Purpose Input and Output Port 4.6/Programmable Logic Array Output Element 14.
F2	TDI	JTAG Test Port Input, Test Data In. Debug and download access.
F3	DAC0/ADC12	DAC0 Voltage Output/ADC Input 12.
F4	P3.1/$PWM0_L$/PLAI[9]	General-Purpose Input and Output Port 3.1/PWM Phase 0 Low-Side Output/Programmable Logic Array Input Element 9.
F5	P3.3/$PWM1_L$/PLAI[11]	General-Purpose Input and Output Port 3.3/PWM Phase 1 Low-Side Output/Programmable Logic Array Input Element 11.
F6	$\overline{RST}$	Reset Input, Active Low.
F7	P0.7/ECLK/XCLK/SPM8/PLAO[4]	Serial Port Multiplexed. General-Purpose Input and Output Port 0.7/Output for External Clock Signal/Input to the Internal Clock Generator Circuits/UART/Programmable Logic Array Output Element 4.
F8	XCLKO	Output from the Crystal Oscillator Inverter.
G1	BM/P0.0/CMP_{OUT}/PLAI[7]	Multifunction I/O Pin. Boot mode. The ADuC7028 enters UART download mode if BM is low at reset and executes code if BM is pulled high at reset through a 1 kΩ resistor/General-Purpose Input and Output Port 0.0/Voltage Comparator Output/Programmable Logic Array Input Element 7.
G2	P4.7/PLAO[15]	General-Purpose Input and Output Port 4.7/Programmable Logic Array Output Element 15.
G3	TMS	JTAG Test Port Input, Test Mode Select. Debug and download access.
G4	TDO	JTAG Test Port Output, Test Data Out. Debug and download access.
G5	P0.3/TRST/ADC_{BUSY}	General-Purpose Input and Output Port 0.3/JTAG Test Port Input, Test Reset/ADC_{BUSY} Signal Output.
G6	P3.4/$PWM2_H$/PLAI[12]	General-Purpose Input and Output Port 3.4/PWM Phase 2 High-Side Output/Programmable Logic Array Input 12.
G7	P3.5/$PWM2_L$/PLAI[13]	General-Purpose Input and Output Port 3.5/PWM Phase 2 Low-Side Output/Programmable Logic Array Input Element 13.
G8	P2.0/SPM9/PLAO[5]/$\overline{CONV_{START}}$	Serial Port Multiplexed. General-Purpose Input and Output Port 2.0/UART/Programmable Logic Array Output Element 5/Start Conversion Input Signal for ADC.
H1	P0.6/T1/MRST/PLAO[3]	Multifunction Pin, Driven Low After Reset. General-Purpose Output Port 0.6/Timer1 Input/Power-On Reset Output/Programmable Logic Array Output Element 3.
H2	TCK	JTAG Test Port Input, Test Clock. Debug and download access.
H3	IOGND	Ground for GPIO (see Table 78). Typically connected to DGND.
H4	IOV_{DD}	3.3 V Supply for GPIO (see Table 78) and Input of the On-Chip Voltage Regulator.
H5	LV_{DD}	2.6 V Output of the On-Chip Voltage Regulator. This output must be connected to a 0.47 µF capacitor to DGND only.
H6	DGND	Ground for Core Logic.
H7	IRQ0/P0.4/PWM_{TRIP}/PLAO[1]	Multifunction I/O Pin. External Interrupt Request 0, Active High/General-Purpose Input and Output Port 0.4/PWM Trip External Input/Programmable Logic Array Output Element 1.
H8	IRQ1/P0.5/ADC_{BUSY}/PLAO[2]	Multifunction I/O Pin. External Interrupt Request 1, Active High/General-Purpose Input and Output Port 0.5/ADC_{BUSY} Signal Output/Programmable Logic Array Output Element 2.

OVERVIEW OF THE ARM7TDMI CORE

The ARM7® core is a 32-bit reduced instruction set computer (RISC). It uses a single 32-bit bus for instruction and data. The length of the data can be eight bits, 16 bits, or 32 bits. The length of the instruction word is 32 bits.

The ARM7TDMI is an ARM7 core with four additional features.

- T support for the thumb (16-bit) instruction set.
- D support for debug.
- M support for long multiplications.
- I includes the EmbeddedICE module to support embedded system debugging.

THUMB MODE (T)

An ARM instruction is 32 bits long. The ARM7TDMI processor supports a second instruction set that is compressed into 16 bits, called the thumb instruction set. Faster execution from 16-bit memory and greater code density can usually be achieved by using the thumb instruction set instead of the ARM instruction set, which makes the ARM7TDMI core particularly suitable for embedded applications.

However, the thumb mode has two limitations.

- Thumb code typically requires more instructions for the same job. As a result, ARM code is usually best for maximizing the performance of time-critical code.
- The thumb instruction set does not include some of the instructions needed for exception handling, which automatically switches the core to ARM code for exception handling.

See the ARM7TDMI user guide for details on the core architecture, the programming model, and both the ARM and ARM thumb instruction sets.

LONG MULTIPLY (M)

The ARM7TDMI instruction set includes four extra instructions that perform 32-bit by 32-bit multiplication with a 64-bit result, and 32-bit by 32-bit multiplication-accumulation (MAC) with a 64-bit result. These results are achieved in fewer cycles than required on a standard ARM7 core.

EmbeddedICE (I)

EmbeddedICE provides integrated on-chip support for the core. The EmbeddedICE module contains the breakpoint and watchpoint registers that allow code to be halted for debugging purposes. These registers are controlled through the JTAG test port.

When a breakpoint or watchpoint is encountered, the processor halts and enters debug state. Once in a debug state, the processor registers can be inspected as well as the Flash/EE, SRAM, and memory mapped registers.

EXCEPTIONS

ARM supports five types of exceptions and a privileged processing mode for each type. The five types of exceptions are

- Normal interrupt or IRQ, which is provided to service general-purpose interrupt handling of internal and external events.
- Fast interrupt or FIQ, which is provided to service data transfers or communication channels with low latency. FIQ has priority over IRQ.
- Memory abort.
- Attempted execution of an undefined instruction.
- Software interrupt instruction (SWI), which can be used to make a call to an operating system.

Typically, the programmer defines interrupt as IRQ, but for higher priority interrupt, that is, faster response time, the programmer can define interrupt as FIQ.

ARM REGISTERS

ARM7TDMI has a total of 37 registers: 31 general-purpose registers and six status registers. Each operating mode has dedicated banked registers.

When writing user-level programs, 15 general-purpose 32-bit registers (R0 to R14), the program counter (R15), and the current program status register (CPSR) are usable. The remaining registers are used for system-level programming and exception handling only.

When an exception occurs, some of the standard registers are replaced with registers specific to the exception mode. All exception modes have replacement banked registers for the stack pointer (R13) and the link register (R14), as represented in Figure 44. The fast interrupt mode has more registers (R8 to R12) for fast interrupt processing. This means that interrupt processing can begin without the need to save or restore these registers and, thus, save critical time in the interrupt handling process.

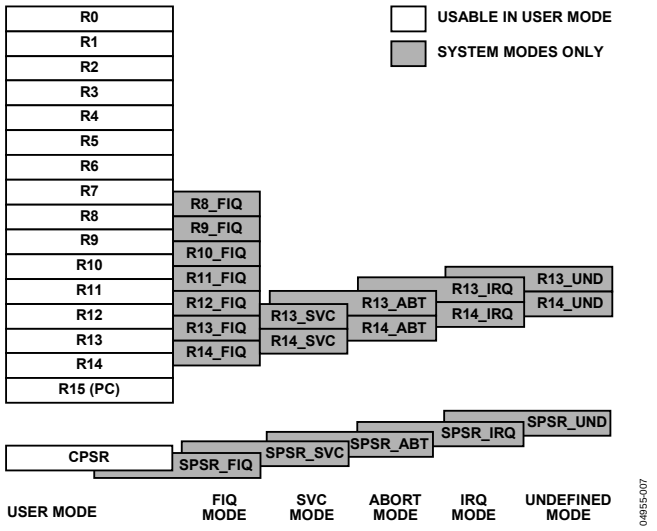


Figure 44. Register Organization

Table 28. V_{CM} Ranges

AV_{DD}	V_{REF}	V_{CM} Min	V_{CM} Max	Signal Peak-to-Peak
3.3 V	2.5 V	1.25 V	2.05 V	2.5 V
	2.048 V	1.024 V	2.276 V	2.048 V
	1.25 V	0.75 V	2.55 V	1.25 V
3.0 V	2.5 V	1.25 V	1.75 V	2.5 V
	2.048 V	1.024 V	1.976 V	2.048 V
	1.25 V	0.75 V	2.25 V	1.25 V

CALIBRATION

By default, the factory-set values written to the ADC offset (ADCOF) and gain coefficient registers (ADCGN) yield optimum performance in terms of end-point errors and linearity for standalone operation of the part (see the Specifications section). If system calibration is required, it is possible to modify the default offset and gain coefficients to improve end-point errors, but note that any modification to the factory-set ADCOF and ADCGN values can degrade ADC linearity performance.

For system offset error correction, the ADC channel input stage must be tied to AGND. A continuous software ADC conversion loop must be implemented by modifying the value in ADCOF until the ADC result (ADCDAT) reads Code 0 to Code 1. If the ADCDAT value is greater than 1, ADCOF should be decremented until ADCDAT reads 0 to 1. Offset error correction is done digitally and has a resolution of 0.25 LSB and a range of ±3.125% of V_{REF}.

For system gain error correction, the ADC channel input stage must be tied to V_{REF}. A continuous software ADC conversion loop must be implemented to modify the value in ADCGN until the ADC result (ADCDAT) reads Code 4094 to Code 4095. If the ADCDAT value is less than 4094, ADCGN should be incremented until ADCDAT reads 4094 to 4095. Similar to the offset calibration, the gain calibration resolution is 0.25 LSB with a range of ±3% of V_{REF}.

TEMPERATURE SENSOR

The ADuC7019/20/21/22/24/25/26/27/28/29 provide voltage output from on-chip band gap references proportional to absolute temperature. This voltage output can also be routed through the front-end ADC multiplexer (effectively an additional ADC channel input) facilitating an internal temperature sensor channel, measuring die temperature to an accuracy of ±3°C.

The following is an example routine showing how to use the internal temperature sensor:

```
int main(void)
{
float a = 0;
      short b;
      ADCCON = 0x20;    // power-on the ADC
      delay(2000);
      ADCCP = 0x10;  // Select Temperature
Sensor as an // input to the ADC
      REFCON = 0x01; // connect internal 2.5V
reference // to Vref pin
      ADCCON = 0xE4; // continuous conversion
      while(1)
      {
              while (!ADCSTA){};
      // wait for end of conversion
              b = (ADCDAT >> 16);
      // To calculate temperature in °C, use
the formula:
              a = 0x525 - b;
      // ((Temperature = 0x525 - Sensor
Voltage) / 1.3)
              a /= 1.3;
              b = floor(a);
              printf("Temperature: %d
oC\n",b);
      }
      return 0;
}
```

BAND GAP REFERENCE

Each ADuC7019/20/21/22/24/25/26/27/28/29 provides an on-chip band gap reference of 2.5 V, which can be used for the ADC and DAC. This internal reference also appears on the V_{REF} pin. When using the internal reference, a 0.47 µF capacitor must be connected from the external V_{REF} pin to AGND to ensure stability and fast response during ADC conversions. This reference can also be connected to an external pin (V_{REF}) and used as a reference for other circuits in the system. An external buffer is required because of the low drive capability of the V_{REF} output. A programmable option also allows an external reference input on the V_{REF} pin. Note that it is not possible to disable the internal reference. Therefore, the external reference source must be capable of overdriving the internal reference source.

Table 29. REFCON Register

Name	Address	Default Value	Access
REFCON	0xFFFF048C	0x00	R/W

The band gap reference interface consists of an 8-bit MMR REFCON, described in Table 30.

Table 30. REFCON MMR Bit Designations

Bit	Description
7:1	Reserved.
0	Internal reference output enable. Set by user to connect the internal 2.5 V reference to the V_{REF} pin. The reference can be used for an external component but must be buffered. Cleared by user to disconnect the reference from the V_{REF} pin.

OTHER ANALOG PERIPHERALS

DAC

The ADuC7019/20/21/22/24/25/26/27/28/29 incorporate two, three, or four 12-bit voltage output DACs on-chip, depending on the model. Each DAC has a rail-to-rail voltage output buffer capable of driving 5 kΩ/100 pF.

Each DAC has three selectable ranges: 0 V to V_{REF} (internal band gap 2.5 V reference), 0 V to DAC_{REF}, and 0 V to AV_{DD}. DAC_{REF} is equivalent to an external reference for the DAC. The signal range is 0 V to AV_{DD}.

MMRs Interface

Each DAC is independently configurable through a control register and a data register. These two registers are identical for the four DACs. Only DAC0CON (see Table 50) and DAC0DAT (see Table 52) are described in detail in this section.

Table 49. DACxCON Registers

Name	Address	Default Value	Access
DAC0CON	0xFFFF0600	0x00	R/W
DAC1CON	0xFFFF0608	0x00	R/W
DAC2CON	0xFFFF0610	0x00	R/W
DAC3CON	0xFFFF0618	0x00	R/W

Table 50. DAC0CON MMR Bit Designations

Bit	Name	Value	Description
7:6			Reserved.
5	DACCLK		DAC update rate. Set by user to update the DAC using Timer1. Cleared by user to update the DAC using HCLK (core clock).
4	DACCLR		DAC clear bit. Set by user to enable normal DAC operation. Cleared by user to reset data register of the DAC to 0.
3			Reserved. This bit should be left at 0.
2			Reserved. This bit should be left at 0.
1:0			DAC range bits.
		00	Power-down mode. The DAC output is in three-state.
		01	0 V to DAC_{REF} range.
		10	0 V to V_{REF} (2.5 V) range.
		11	0 V to AV_{DD} range.

Table 51. DACxDAT Registers

Name	Address	Default Value	Access
DAC0DAT	0xFFFF0604	0x00000000	R/W
DAC1DAT	0xFFFF060C	0x00000000	R/W
DAC2DAT	0xFFFF0614	0x00000000	R/W
DAC3DAT	0xFFFF061C	0x00000000	R/W

Table 52. DAC0DAT MMR Bit Designations

Bit	Description
31:28	Reserved.
27:16	12-bit data for DAC0.
15:0	Reserved.

Using the DACs

The on-chip DAC architecture consists of a resistor string DAC followed by an output buffer amplifier. The functional equivalent is shown in Figure 63.

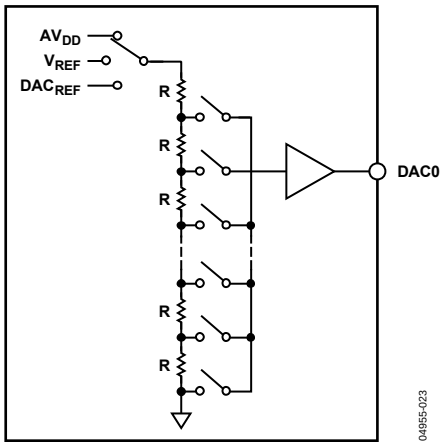


Figure 63. DAC Structure

As illustrated in Figure 63, the reference source for each DAC is user-selectable in software. It can be AV_{DD}, V_{REF}, or DAC_{REF}. In 0-to-AV_{DD} mode, the DAC output transfer function spans from 0 V to the voltage at the AV_{DD} pin. In 0-to-DAC_{REF} mode, the DAC output transfer function spans from 0 V to the voltage at the DAC_{REF} pin. In 0-to-V_{REF} mode, the DAC output transfer function spans from 0 V to the internal 2.5 V reference, V_{REF}.

The DAC output buffer amplifier features a true, rail-to-rail output stage implementation. This means that when unloaded, each output is capable of swinging to within less than 5 mV of both AV_{DD} and ground. Moreover, the DAC's linearity specification (when driving a 5 kΩ resistive load to ground) is guaranteed through the full transfer function, except Code 0 to Code 100, and, in 0-to-AV_{DD} mode only, Code 3995 to Code 4095.

Input offset voltage (V_{OS}) is the difference between the center of the hysteresis range and the ground level. This can either be positive or negative. The hysteresis voltage (V_H) is one-half the width of the hysteresis range.

Comparator Interface

The comparator interface consists of a 16-bit MMR, CMPCON, which is described in Table 56.

Table 55. CMPCON Register

Name	Address	Default Value	Access
CMPCON	0xFFFF0444	0x0000	R/W

Table 56. CMPCON MMR Bit Descriptions

Bit	Name	Value	Description
15:11			Reserved.
10	CMPEN		Comparator enable bit. Set by user to enable the comparator. Cleared by user to disable the comparator.
9:8	CMPIN		Comparator negative input select bits.
		00	$AV_{DD}/2$.
		01	ADC3 input.
		10	DAC0 output.
		11	Reserved.
7:6	CMPOC		Comparator output configuration bits.
		00	Reserved.
		01	Reserved.
		10	Output on CMP_{OUT}.
		11	IRQ.
5	CMPOL		Comparator output logic state bit. When low, the comparator output is high if the positive input (CMP0) is above the negative input (CMP1). When high, the comparator output is high if the positive input is below the negative input.
4:3	CMPRES		Response time.
		00	5 µs response time is typical for large signals (2.5 V differential). 17 µs response time is typical for small signals (0.65 mV differential).
		11	3 µs typical.
		01/10	Reserved.
2	CMPHYST		Comparator hysteresis bit. Set by user to have a hysteresis of about 7.5 mV. Cleared by user to have no hysteresis.
1	CMPORI		Comparator output rising edge interrupt. Set automatically when a rising edge occurs on the monitored voltage (CMP0). Cleared by user by writing a 1 to this bit.
0	CMPOFI		Comparator output falling edge interrupt. Set automatically when a falling edge occurs on the monitored voltage (CMP0). Cleared by user.

OSCILLATOR AND PLL—POWER CONTROL

Clocking System

Each ADuC7019/20/21/22/24/25/26/27/28/29 integrates a 32.768 kHz ±3% oscillator, a clock divider, and a PLL. The PLL locks onto a multiple (1275) of the internal oscillator or an external 32.768 kHz crystal to provide a stable 41.78 MHz clock (UCLK) for the system. To allow power saving, the core can operate at this frequency, or at binary submultiples of it. The actual core operating frequency, $UCLK/2^{CD}$, is refered to as HCLK. The default core clock is the PLL clock divided by 8 (CD = 3) or 5.22 MHz. The core clock frequency can also come from an external clock on the ECLK pin as described in Figure 67. The core clock can be outputted on ECLK when using an internal oscillator or external crystal.

Note that when the ECLK pin is used to output the core clock, the output signal is not buffered and is not suitable for use as a clock source to an external device without an external buffer.

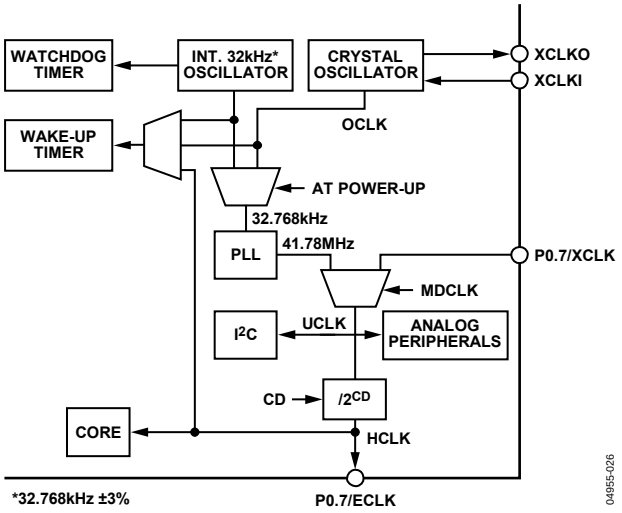


Figure 67. Clocking System

The selection of the clock source is in the PLLCON register. By default, the part uses the internal oscillator feeding the PLL.

External Crystal Selection

To switch to an external crystal, the user must do the following:

1. Enable the Timer2 interrupt and configure it for a timeout period of >120 µs.
2. Follow the write sequence to the PLLCON register, setting the MDCLK bits to 01 and clearing the OSEL bit.
3. Force the part into NAP mode by following the correct write sequence to the POWCON register.

   When the part is interrupted from NAP mode by the Timer2 interrupt source, the clock source has switched to the external clock.

Example source code

```
    t2val_old= T2VAL;
     T2LD = 5;
     TCON = 0x480;


  while ((T2VAL == t2val_old) || (T2VAL >
3)) //ensures timer value loaded
  IRQEN = 0x10;
//enable T2 interrupt
  PLLKEY1 = 0xAA;
  PLLCON = 0x01;
  PLLKEY2 = 0x55;

  POWKEY1 = 0x01;
  POWCON = 0x27;
// Set Core into Nap mode
  POWKEY2 = 0xF4;
```

In noisy environments, noise can couple to the external crystal pins, and PLL may lose lock momentarily. A PLL interrupt is provided in the interrupt controller. The core clock is immediately halted, and this interrupt is only serviced when the lock is restored.

In case of crystal loss, the watchdog timer should be used. During initialization, a test on the RSTSTA register can determine if the reset came from the watchdog timer.

External Clock Selection

To switch to an external clock on P0.7, configure P0.7 in Mode 1. The external clock can be up to 44 MHz, providing the tolerance is 1%.

Example source code

```
    t2val_old= T2VAL;
     T2LD = 5;
     TCON = 0x480;


  while ((T2VAL == t2val_old) || (T2VAL
> 3)) //ensures timer value loaded
  IRQEN = 0x10;
//enable T2 interrupt
  PLLKEY1 = 0xAA;
  PLLCON = 0x03; //Select external clock
  PLLKEY2 = 0x55;

  POWKEY1 = 0x01;
  POWCON = 0x27;
// Set Core into Nap mode
  POWKEY2 = 0xF4;
```

Power Control System

A choice of operating modes is available on the ADuC7019/20/21/22/24/25/26/27/28/29. Table 57 describes what part is powered on in the different modes and indicates the power-up time.

Table 58 gives some typical values of the total current consumption (analog + digital supply currents) in the different modes, depending on the clock divider bits. The ADC is turned off. Note that these values also include current consumption of the regulator and other parts on the test board where these values are measured.

Table 57. Operating Modes[1]

Mode	Core	Peripherals	PLL	XTAL/T2/T3	IRQ0 to IRQ3	Start-Up/Power-On Time
Active	X	X	X	X	X	130 ms at CD = 0
Pause		X	X	X	X	24 ns at CD = 0; 3 µs at CD = 7
Nap			X	X	X	24 ns at CD = 0; 3 µs at CD = 7
Sleep				X	X	1.58 ms
Stop					X	1.7 ms

[1] X indicates that the part is powered on.

Table 58. Typical Current Consumption at 25°C in Milliamperes

PC[2:0]	Mode	CD = 0	CD = 1	CD = 2	CD = 3	CD = 4	CD = 5	CD = 6	CD = 7
000	Active	33.1	21.2	13.8	10	8.1	7.2	6.7	6.45
001	Pause	22.7	13.3	8.5	6.1	4.9	4.3	4	3.85
010	Nap	3.8	3.8	3.8	3.8	3.8	3.8	3.8	3.8
011	Sleep	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4
100	Stop	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4

Output Control Unit

The operation of the output control unit is controlled by the 9-bit read/write PWMEN register. This register controls two distinct features of the output control unit that are directly useful in the control of electronic counter measures (ECM) or binary decimal counter measures (BDCM). The PWMEN register contains three crossover bits, one for each pair of PWM outputs. Setting Bit 8 of the PWMEN register enables the crossover mode for the 0H/0L pair of PWM signals, setting Bit 7 enables crossover on the 1H/1L pair of PWM signals, and setting Bit 6 enables crossover on the 2H/2L pair of PWM signals. If crossover mode is enabled for any pair of PWM signals, the high-side PWM signal from the timing unit (0H, for example) is diverted to the associated low-side output of the output control unit so that the signal ultimately appears at the $PWM0_L$ pin. Of course, the corresponding low-side output of the timing unit is also diverted to the complementary high-side output of the output control unit so that the signal appears at the $PWM0_H$ pin. Following a reset, the three crossover bits are cleared, and the crossover mode is disabled on all three pairs of PWM signals. The PWMEN register also contains six bits (Bit 0 to Bit 5) that can be used to individually enable or disable each of the six PWM outputs. If the associated bit of the PWMEN register is set, the corresponding PWM output is disabled regardless of the corresponding value of the duty cycle register. This PWM output signal remains in the off state as long as the corresponding enable/disable bit of the PWMEN register is set. The implementation of this output enable function is implemented after the crossover function.

Following a reset, all six enable bits of the PWMEN register are cleared, and all PWM outputs are enabled by default. In a manner identical to the duty cycle registers, the PWMEN is latched on the rising edge of the PWMSYNC signal. As a result, changes to this register become effective only at the start of each PWM cycle in single update mode. In double update mode, the PWMEN register can also be updated at the midpoint of the PWM cycle.

In the control of an ECM, only two inverter legs are switched at any time, and often the high-side device in one leg must be switched on at the same time as the low-side driver in a second leg. Therefore, by programming identical duty cycle values for two PWM channels (for example, PWMCH0 = PWMCH1) and setting Bit 7 of the PWMEN register to cross over the 1H/1L pair of PWM signals, it is possible to turn on the high-side switch of Phase A and the low-side switch of Phase B at the same time. In the control of ECM, it is usual for the third inverter leg (Phase C in this example) to be disabled for a number of PWM cycles. This function is implemented by disabling both the 2H and 2L PWM outputs by setting Bit 0 and Bit 1 of the PWMEN register.

This situation is illustrated in Figure 71, where it can be seen that both the 0H and 1L signals are identical because PWMCH0 = PWMCH1 and the crossover bit for Phase B is set.

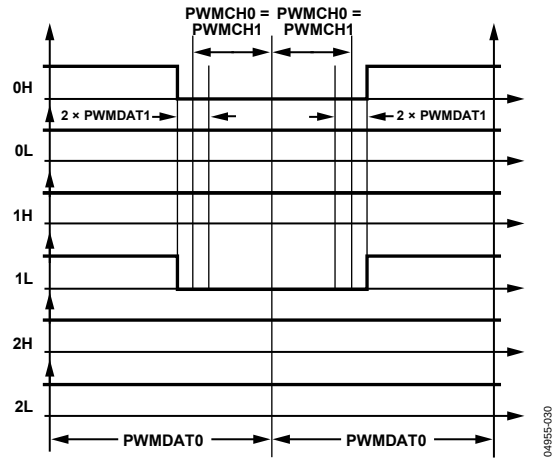


Figure 71. Active Low PWM Signals Suitable for ECM Control, PWMCH0 = PWMCH1, Crossover 1H/1L Pair and Disable 0L, 1H, 2H, and 2L Outputs in Single Update Mode.

In addition, the other four signals (0L, 1H, 2H, and 2L) have been disabled by setting the appropriate enable/disable bits of the PWMEN register. In Figure 71, the appropriate value for the PWMEN register is 0x00A7. In normal ECM operation, each inverter leg is disabled for certain periods of time to change the PWMEN register based on the position of the rotor shaft (motor commutation).

Gate Drive Unit

The gate drive unit of the PWM controller adds features that simplify the design of isolated gate-drive circuits for PWM inverters. If a transformer-coupled, power device, gate-drive amplifier is used, the active PWM signal must be chopped at a high frequency. The 16-bit read/write PWMCFG register programs this high frequency chopping mode. The chopped active PWM signals can be required for the high-side drivers only, the low-side drivers only, or both the high-side and low-side switches. Therefore, independent control of this mode for both high-side and low-side switches is included with two separate control bits in the PWMCFG register.

Typical PWM output signals with high frequency chopping enabled on both high-side and low-side signals are shown in Figure 72. Chopping of the high-side PWM outputs (0H, 1H, and 2H) is enabled by setting Bit 8 of the PWMCFG register. Chopping of the low-side PWM outputs (0L, 1L, and 2L) is enabled by setting Bit 9 of the PWMCFG register. The high chopping frequency is controlled by the 8-bit word (GDCLK) placed in Bit 0 to Bit 7 of the PWMCFG register. The period of this high frequency carrier is

$$t_{CHOP} = (4 \times (GDCLK + 1)) \times t_{CORE}$$

The chopping frequency is, therefore, an integral subdivision of the MicroConverter core frequency

$$f_{CHOP} = f_{CORE}/(4 \times (GDCLK + 1))$$

Table 83. GPIO Drive Strength Control Bits Descriptions

Control Bits Value	Description
00	Medium drive strength.
01	Low drive strength.
1x	High drive strength.

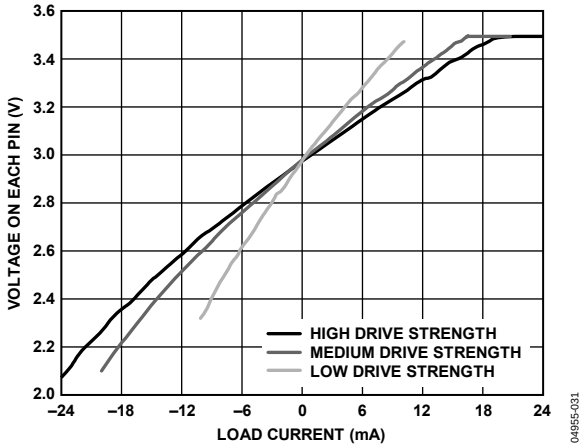


Figure 73. Programmable Strength for High Level (Typical Values)

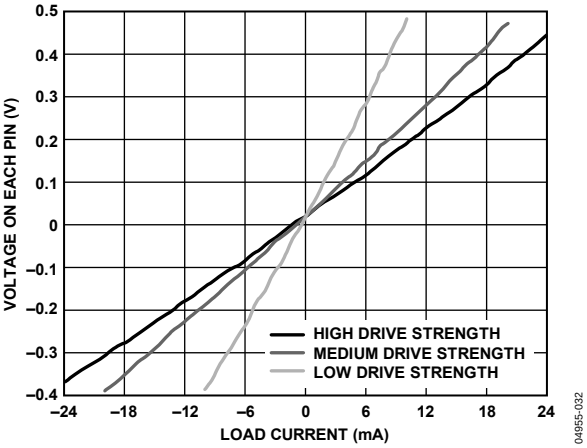


Figure 74. Programmable Strength for Low Level (Typical Values)

The drive strength bits can be written to one time only after reset. More writing to related bits has no effect on changing drive strength. The GPIO drive strength and pull-up disable is not always adjustable for the GPIO port. Some control bits cannot be changed (see Table 84).

Table 84. GPxPAR Control Bits Access Descriptions

Bit	GP0PAR	GP1PAR
31	Reserved	Reserved
30 to 29	R/W	R/W
28	R/W	R/W
27	Reserved	Reserved
26 to 25	R/W	R/W
24	R/W	R/W
23	Reserved	Reserved
22 to 21	R/W	R (b00)
20	R/W	R/W
19	Reserved	Reserved
18 to 17	R (b00)	R (b00)
16	R/W	R/W
15	Reserved	Reserved
14 to 13	R (b00)	R (b00)
12	R/W	R/W
11	Reserved	Reserved
10 to 9	R (b00)	R (b00)
8	R/W	R/W
7	Reserved	Reserved
6 to 5	R (b00)	R (b00)
4	R/W	R/W
3	Reserved	Reserved
2 to 1	R (b00)	R (b00)
0	R/W	R/W

Table 99. COMDIV1 Register

Name	Address	Default Value	Access
COMDIV1	0xFFFF0704	0x00	R/W

COMDIV1 is a divisor latch (high byte) register.

Table 100. COMIID0 Register

Name	Address	Default Value	Access
COMIID0	0xFFFF0708	0x01	R

COMIID0 is the interrupt identification register.

Table 101. COMIID0 MMR Bit Descriptions

Bit 2:1 Status Bits	Bit 0 NINT	Priority	Definition	Clearing Operation
00	1	N/A	No interrupt	N/A
11	0	1 (Highest)	Receive line status interrupt	Read COMSTA0
10	0	2	Receive buffer full interrupt	Read COMRX
01	0	3	Transmit buffer empty interrupt	Write data to COMTX or read COMIID0
00	0	4 (Lowest)	Modem status interrupt	Read COMSTA1

Table 102. COMCON0 Register

Name	Address	Default Value	Access
COMCON0	0xFFFF070C	0x00	R/W

COMCON0 is the line control register.

Table 103. COMCON0 MMR Bit Descriptions

Bit	Name	Description
7	DLAB	Divisor latch access. Set by user to enable access to the COMDIV0 and COMDIV1 registers. Cleared by user to disable access to COMDIV0 and COMDIV1 and enable access to COMRX and COMTX.
6	BRK	Set break. Set by user to force SOUT to 0. Cleared to operate in normal mode.
5	SP	Stick parity. Set by user to force parity to defined values: 1 if EPS = 1 and PEN = 1, 0 if EPS = 0 and PEN = 1.
4	EPS	Even parity select bit. Set for even parity. Cleared for odd parity.
3	PEN	Parity enable bit. Set by user to transmit and check the parity bit. Cleared by user for no parity transmission or checking.
2	STOP	Stop bit. Set by user to transmit 1.5 stop bits if the word length is five bits or 2 stop bits if the word length is six bits, seven bits, or eight bits. The receiver checks the first stop bit only, regardless of the number of stop bits selected. Cleared by user to generate 1 stop bit in the transmitted data.
1:0	WLS	Word length select: 00 = five bits, 01 = six bits, 10 = seven bits, 11 = eight bits.

Table 104. COMCON1 Register

Name	Address	Default Value	Access
COMCON1	0xFFFF0710	0x00	R/W

COMCON1 is the modem control register.

Table 105. COMCON1 MMR Bit Descriptions

Bit	Name	Description
7:5		Reserved.
4	LOOPBACK	Loopback. Set by user to enable loopback mode. In loopback mode, SOUT (see Table 78) is forced high. The modem signals are also directly connected to the status inputs (RTS to CTS and DTR to DSR). Cleared by user to be in normal mode.
3	PEN	Parity enable bit. Set by user to transmit and check the parity bit. Cleared by user for no parity transmission or checking.
2	STOP	Stop bit. Set by user to transmit 1.5 stop bits if the word length is five bits, or 2 stop bits if the word length is six bits, seven bits, or eight bits. The receiver checks the first stop bit only, regardless of the number of stop bits selected. Cleared by user to generate 1 stop bit in the transmitted data.
1	RTS	Request to send. Set by user to force the RTS output to 0. Cleared by user to force the RTS output to 1.
0	DTR	Data terminal ready. Set by user to force the DTR output to 0. Cleared by user to force the DTR output to 1.

Table 106. COMSTA0 Register

Name	Address	Default Value	Access
COMSTA0	0xFFFF0714	0x60	R

COMSTA0 is the line status register.

Table 107. COMSTA0 MMR Bit Descriptions

Bit	Name	Description
7		Reserved.
6	TEMT	COMTX and shift register empty status bit. Set automatically if COMTX and shift register are empty. Cleared automatically when writing to COMTX.
5	THRE	COMTX empty. Set automatically if COMTX is empty. Cleared automatically when writing to COMTX.
4	BI	Break error. Set when SIN is held low for more than the maximum word length. Cleared automatically.
3	FE	Framing error. Set when an invalid stop bit occurs. Cleared automatically.
2	PE	Parity error. Set when a parity error occurs. Cleared automatically.
1	OE	Overrun error. Set automatically if data is over-written before being read. Cleared automatically.
0	DR	Data ready. Set automatically when COMRX is full. Cleared by reading COMRX.

PROGRAMMABLE LOGIC ARRAY (PLA)

Every ADuC7019/20/21/22/24/25/26/27/28/29 integrates a fully programmable logic array (PLA) that consists of two independent but interconnected PLA blocks. Each block consists of eight PLA elements, giving each part a total of 16 PLA elements.

Each PLA element contains a two-input lookup table that can be configured to generate any logic output function based on two inputs and a flip-flop. This is represented in Figure 76.

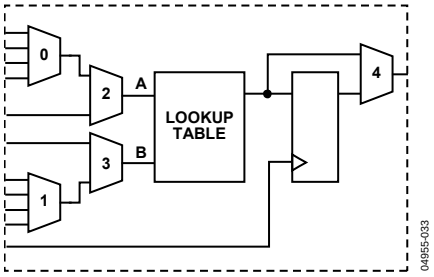


Figure 76. PLA Element

In total, 30 GPIO pins are available on each ADuC7019/20/21/22/24/25/26/27/28/29 for the PLA. These include 16 input pins and 14 output pins, which msut be configured in the GPxCON register as PLA pins before using the PLA. Note that the comparator output is also included as one of the 16 input pins.

The PLA is configured via a set of user MMRs. The output(s) of the PLA can be routed to the internal interrupt system, to the $\overline{\text{CONV}}_{\text{START}}$ signal of the ADC, to an MMR, or to any of the 16 PLA output pins.

The two blocks can be interconnected as follows:

- Output of Element 15 (Block 1) can be fed back to Input 0 of Mux 0 of Element 0 (Block 0).
- Output of Element 7 (Block 0) can be fed back to the Input 0 of Mux 0 of Element 8 (Block 1).

Table 145. Element Input/Output

PLA Block 0			PLA Block 1		
Element	**Input**	**Output**	**Element**	**Input**	**Output**
0	P1.0	P1.7	8	P3.0	P4.0
1	P1.1	P0.4	9	P3.1	P4.1
2	P1.2	P0.5	10	P3.2	P4.2
3	P1.3	P0.6	11	P3.3	P4.3
4	P1.4	P0.7	12	P3.4	P4.4
5	P1.5	P2.0	13	P3.5	P4.5
6	P1.6	P2.1	14	P3.6	P4.6
7	P0.0	P2.2	15	P3.7	P4.7

PLA MMRs Interface

The PLA peripheral interface consists of the 22 MMRs described in this section.

Table 146. PLAELMx Registers

Name	Address	Default Value	Access
PLAELM0	0xFFFF0B00	0x0000	R/W
PLAELM1	0xFFFF0B04	0x0000	R/W
PLAELM2	0xFFFF0B08	0x0000	R/W
PLAELM3	0xFFFF0B0C	0x0000	R/W
PLAELM4	0xFFFF0B10	0x0000	R/W
PLAELM5	0xFFFF0B14	0x0000	R/W
PLAELM6	0xFFFF0B18	0x0000	R/W
PLAELM7	0xFFFF0B1C	0x0000	R/W
PLAELM8	0xFFFF0B20	0x0000	R/W
PLAELM9	0xFFFF0B24	0x0000	R/W
PLAELM10	0xFFFF0B28	0x0000	R/W
PLAELM11	0xFFFF0B2C	0x0000	R/W
PLAELM12	0xFFFF0B30	0x0000	R/W
PLAELM13	0xFFFF0B34	0x0000	R/W
PLAELM14	0xFFFF0B38	0x0000	R/W
PLAELM15	0xFFFF0B3C	0x0000	R/W

PLAELMx are Element 0 to Element 15 control registers. They configure the input and output mux of each element, select the function in the lookup table, and bypass/use the flip-flop. See Table 147 and Table 152.

Table 147. PLAELMx MMR Bit Descriptions

Bit	Value	Description
31:11		Reserved.
10:9		Mux 0 control (see Table 152).
8:7		Mux 1 control (see Table 152).
6		Mux 2 control. Set by user to select the output of Mux 0. Cleared by user to select the bit value from PLADIN.
5		Mux 3 control. Set by user to select the input pin of the particular element. Cleared by user to select the output of Mux 1.
4:1		Lookup table control.
	0000	0.
	0001	NOR.
	0010	B AND NOT A.
	0011	NOT A.
	0100	A AND NOT B.
	0101	NOT B.
	0110	EXOR.
	0111	NAND.
	1000	AND.
	1001	EXNOR.
	1010	B.
	1011	NOT A OR B.
	1100	A.
	1101	A OR NOT B.
	1110	OR.
	1111	1.
0		Mux 4 control. Set by user to bypass the flip-flop. Cleared by user to select the flip-flop (cleared by default).

In normal mode, an IRQ is generated each time the value of the counter reaches zero when counting down. It is also generated each time the counter value reaches full scale when counting up. An IRQ can be cleared by writing any value to clear the register of that particular timer (TxCLRI).

When using an asynchronous clock-to-clock timer, the interrupt in the timer block may take more time to clear than the time it takes for the code in the interrupt routine to execute. Ensure that the interrupt signal is cleared before leaving the interrupt service routine. This can be done by checking the IRQSTA MMR.

Hour:Minute:Second:1/128 Format

To use the timer in hour:minute:second:hundredths format, select the 32,768 kHz clock and prescaler of 256. The hundredths field does not represent milliseconds but 1/128 of a second (256/32,768). The bits representing the hour, minute, and second are not consecutive in the register. This arrangement applies to TxLD and TxVAL when using the hour:minute:second:hundredths format as set in TxCON[5:4]. See Table 171 for additional details.

Table 171. Hour:Minnute:Second:Hundredths Format

Bit	Value	Description
31:24	0 to 23 or 0 to 255	Hours
23:22	0	Reserved
21:16	0 to 59	Minutes
15:14	0	Reserved
13.8	0 to 59	Seconds
7	0	Reserved
6:0	0 to 127	1/128 second

Timer0 (RTOS Timer)

Timer0 is a general-purpose, 16-bit timer (count down) with a programmable prescaler (see Figure 77). The prescaler source is the core clock frequency (HCLK) and can be scaled by factors of 1, 16, or 256.

Timer0 can be used to start ADC conversions as shown in the block diagram in Figure 77.

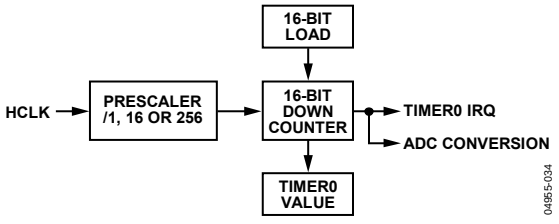


Figure 77. Timer0 Block Diagram

The Timer0 interface consists of four MMRs: T0LD, T0VAL, T0CON, and T0CLRI.

Table 172. T0LD Register

Name	Address	Default Value	Access
T0LD	0xFFFF0300	0x0000	R/W

T0LD is a 16-bit load register.

Table 173. T0VAL Register

Name	Address	Default Value	Access
T0VAL	0xFFFF0304	0xFFFF	R

T0VAL is a 16-bit read-only register representing the current state of the counter.

Table 174. T0CON Register

Name	Address	Default Value	Access
T0CON	0xFFFF0308	0x0000	R/W

T0CON is the configuration MMR described in Table 175.

Table 175. T0CON MMR Bit Descriptions

Bit	Value	Description
15:8		Reserved.
7		Timer0 enable bit. Set by user to enable Timer0. Cleared by user to disable Timer0 by default.
6		Timer0 mode. Set by user to operate in periodic mode. Cleared by user to operate in free-running mode. Default mode.
5:4		Reserved.
3:2		Prescale.
	00	Core Clock/1. Default value.
	01	Core Clock/16.
	10	Core Clock/256.
	11	Undefined. Equivalent to 00.
1:0		Reserved.

Table 176. T0CLRI Register

Name	Address	Default Value	Access
T0CLRI	0xFFFF030C	0xFF	W

T0CLRI is an 8-bit register. Writing any value to this register clears the interrupt.

Table 186. T2CON MMR Bit Descriptions

Bit	Value	Description
31:11		Reserved.
10:9		Clock source.
	00	External crystal.
	01	External crystal.
	10	Internal oscillator.
	11	Core clock (41 MHz/2^{CD}).
8		Count up. Set by user for Timer2 to count up. Cleared by user for Timer2 to count down by default.
7		Timer2 enable bit. Set by user to enable Timer2. Cleared by user to disable Timer2 by default.
6		Timer2 mode. Set by user to operate in periodic mode. Cleared by user to operate in free-running mode. Default mode.
5:4		Format.
	00	Binary.
	01	Reserved.
	10	Hr: min: sec: Hundredths (23 hours to 0 hour).
	11	Hr: min: sec: Hundredths (255 hours to 0 hour).
3:0		Prescale.
	0000	Source Clock/1 by default.
	0100	Source Clock/16.
	1000	Source Clock/256 expected for Format 2 and Format 3.
	1111	Source Clock/32,768.

Table 187. T2CLRI Register

Name	Address	Default Value	Access
T2CLRI	0xFFFF034C	0xFF	W

T2CLRI is an 8-bit register. Writing any value to this register clears the Timer2 interrupt.

Timer3 (Watchdog Timer)

Timer3 has two modes of operation: normal mode and watchdog mode. The watchdog timer is used to recover from an illegal software state. Once enabled, it requires periodic servicing to prevent it from forcing a processor reset.

Normal Mode

Timer3 in normal mode is identical to Timer0, except for the clock source and the count-up functionality. The clock source is 32 kHz from the PLL and can be scaled by a factor of 1, 16, or 256 (see Figure 80).

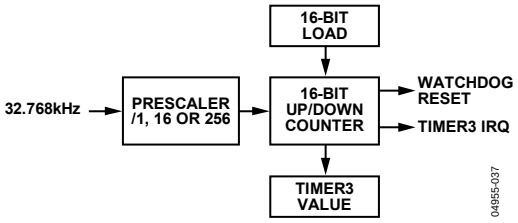


Figure 80. Timer3 Block Diagram

Watchdog Mode

Watchdog mode is entered by setting Bit 5 in the T3CON MMR. Timer3 decreases from the value present in the T3LD register to 0. T3LD is used as the timeout. The maximum timeout can be 512 sec, using the prescaler/256, and full scale in T3LD. Timer3 is clocked by the internal 32 kHz crystal when operating in watchdog mode. Note that to enter watchdog mode successfully, Bit 5 in the T3CON MMR must be set after writing to the T3LD MMR.

If the timer reaches 0, a reset or an interrupt occurs, depending on Bit 1 in the T3CON register. To avoid reset or interrupt, any value must be written to T3CLRI before the expiration period. This reloads the counter with T3LD and begins a new timeout period.

When watchdog mode is entered, T3LD and T3CON are write-protected. These two registers cannot be modified until a reset clears the watchdog enable bit, which causes Timer3 to exit watchdog mode.

The Timer3 interface consists of four MMRs: T3LD, T3VAL, T3CON, and T3CLRI.

Table 188. T3LD Register

Name	Address	Default Value	Access
T3LD	0xFFFF0360	0x0000	R/W

T3LD is a 16-bit register load register.

Table 189. T3VAL Register

Name	Address	Default Value	Access
T3VAL	0xFFFF0364	0xFFFF	R

T3VAL is a 16-bit read-only register that represents the current state of the counter.

Table 190. T3CON Register

Name	Address	Default Value	Access
T3CON	0xFFFF0368	0x0000	R/W

T3CON is the configuration MMR described in Table 191.

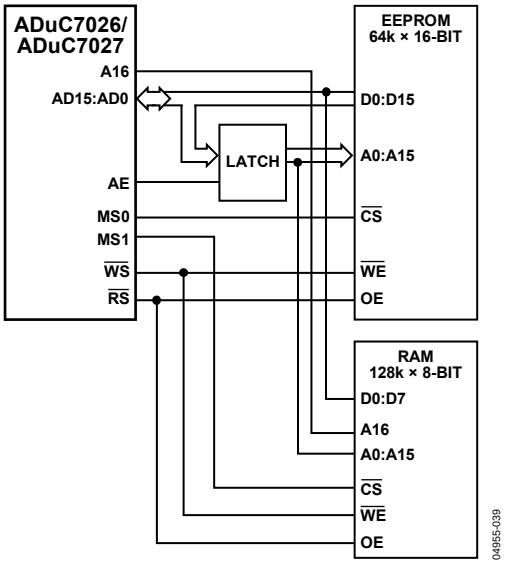


Figure 82. Interfacing to External EEPROM/RAM

Table 195. XMCFG Register

Name	Address	Default Value	Access
XMCFG	0xFFFFF000	0x00	R/W

XMCFG is set to 1 to enable external memory access. This must be set to 1 before any port pins function as external memory access pins. The port pins must also be individually enabled via the GPxCON MMR.

Table 196. XMxCON Registers

Name	Address	Default Value	Access
XM0CON	0xFFFFF010	0x00	R/W
XM1CON	0xFFFFF014	0x00	R/W
XM2CON	0xFFFFF018	0x00	R/W
XM3CON	0xFFFFF01C	0x00	R/W

XMxCON are the control registers for each memory region. They allow the enabling/disabling of a memory region and control the data bus width of the memory region.

Table 197. XMxCON MMR Bit Descriptions

Bit	Description
1	Selects data bus width. Set by user to select a 16-bit data bus. Cleared by user to select an 8-bit data bus.
0	Enables memory region. Set by user to enable the memory region. Cleared by user to disable the memory region.

Table 198. XMxPAR Registers

Name	Address	Default Value	Access
XM0PAR	0xFFFFF020	0x70FF	R/W
XM1PAR	0xFFFFF024	0x70FF	R/W
XM2PAR	0xFFFFF028	0x70FF	R/W
XM3PAR	0xFFFFF02C	0x70FF	R/W

XMxPAR are registers that define the protocol used for accessing the external memory for each memory region.

Table 199. XMxPAR MMR Bit Descriptions

Bit	Description
15	Enable byte write strobe. This bit is used only for two, 8-bit memory devices sharing the same memory region. Set by the user to gate the A0 output with the $\overline{WS}$ output. This allows byte write capability without using $\overline{BHE}$ and $\overline{BLE}$ signals. Cleared by user to use $\overline{BHE}$ and $\overline{BLE}$ signals.
14:12	Number of wait states on the address latch enable STROBE.
11	Reserved.
10	Extra address hold time. Set by user to disable extra hold time. Cleared by user to enable one clock cycle of hold on the address in read and write.
9	Extra bus transition time on read. Set by user to disable extra bus transition time. Cleared by user to enable one extra clock before and after the read strobe ($\overline{RS}$).
8	Extra bus transition time on write. Set by user to disable extra bus transition time. Cleared by user to enable one extra clock before and after the write strobe ($\overline{WS}$).
7:4	Number of write wait states. Select the number of wait states added to the length of the $\overline{WS}$ pulse. 0x0 is 1 clock; 0xF is 16 clock cycles (default value).
3:0	Number of read wait states. Select the number of wait states added to the length of the $\overline{RS}$ pulse. 0x0 is 1 clock; 0xF is 16 clock cycles (default value).

Figure 83, Figure 84, Figure 85, and Figure 86 show the timing for a read cycle, a read cycle with address hold and bus turn cycles, a write cycle with address and write hold cycles, and a write cycle with wait sates, respectively.

DEVELOPMENT TOOLS

PC-BASED TOOLS

Four types of development systems are available for the ADuC7019/20/21/22/24/25/26/27/28/29 family.

- The ADuC7026 QuickStart Plus is intended for new users who want to have a comprehensive hardware development environment. Because the ADuC7026 contains the superset of functions available on the ADuC7019/20/21/22/24/25/26/27/28/29, it is suitable for users who wish to develop on any of the parts in this family. All parts are fully code compatible.
- The ADuC7019, ADuC7024, and ADuC7026 QuickStart systems are intended for users who already have an emulator.

These systems consist of the following PC-based (Windows® compatible) hardware and software development tools.

Hardware

- ADuC7019/20/21/22/24/25/26/27/28/29 evaluation board
- Serial port programming cable
- RDI-compliant JTAG emulator (included in the ADuC7026 QuickStart Plus only)

Software

- Integrated development environment, incorporating assembler, compiler, and nonintrusive JTAG-based debugger
- Serial downloader software
- Example code

Miscellaneous

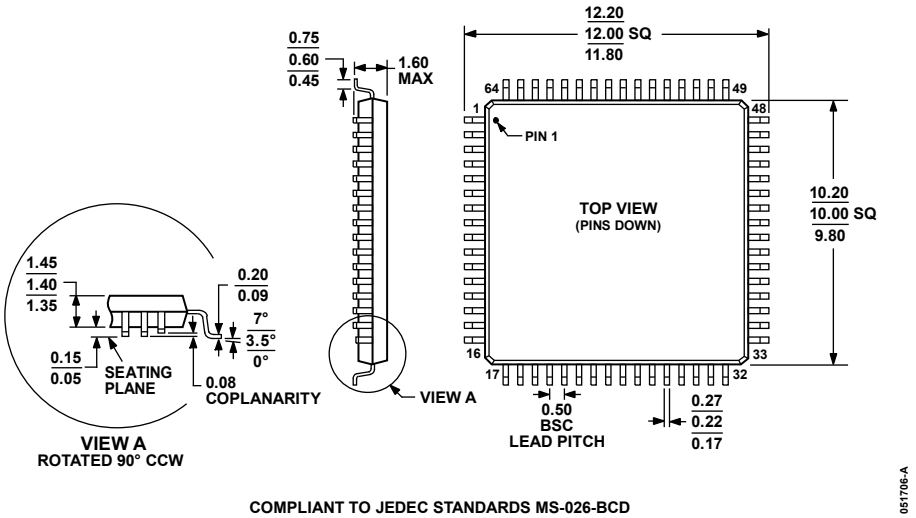
CD-ROM documentation

IN-CIRCUIT SERIAL DOWNLOADER

The serial downloader is a Windows application that allows the user to serially download an assembled program to the on-chip program Flash/EE memory via the serial port on a standard PC.

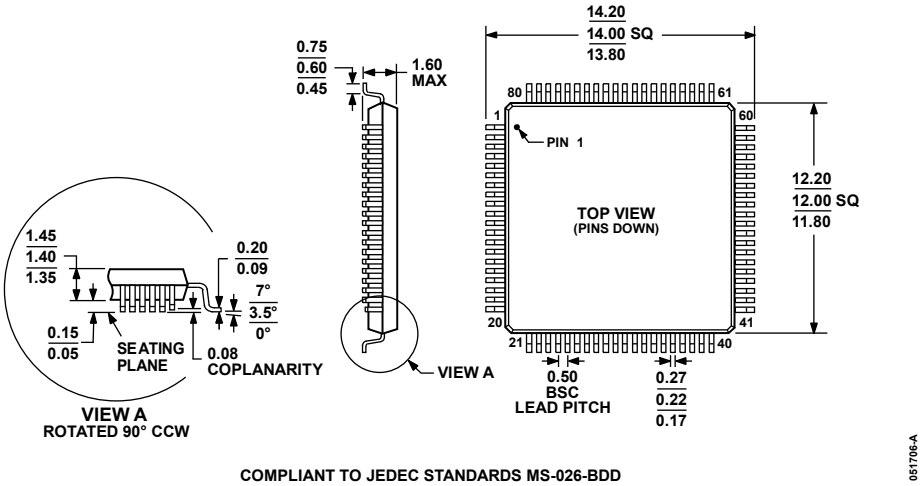
The UART-based serial downloader is included in all the development systems and is usable with the ADuC7019/20/21/22/24/25/26/27/28/29 parts that do not contain the I suffix in the Ordering Guide.

An I^2C based serial downloader and a USB-to-I^2C adaptor board, USB-EA-CONVZ, are also available at www.analog.com. The I^2C-based serial downloader is only usable with the part models containing the I suffix (see Ordering Guide).



COMPLIANT TO JEDEC STANDARDS MS-026-BCD

Figure 98. 64-Lead Low Profile Quad Flat Package [LQFP]
(ST-64-2)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-026-BDD

Figure 99. 80-Lead Low Profile Quad Flat Package [LQFP]
(ST-80-1)
Dimensions shown in millimeters

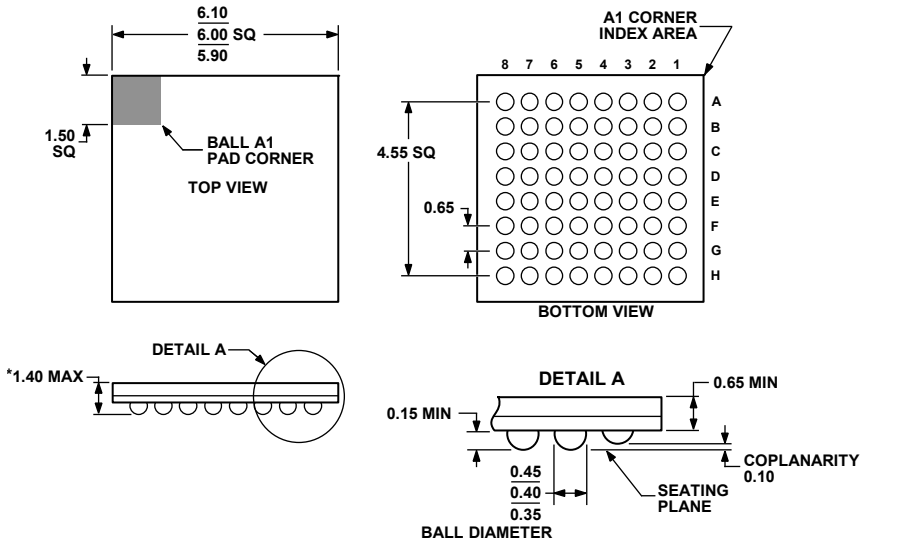


Figure 100. 64-Ball Chip Scale Package Ball Grid Array [CSP_BGA]
(BC-64-4)
Dimensions shown in millimeters

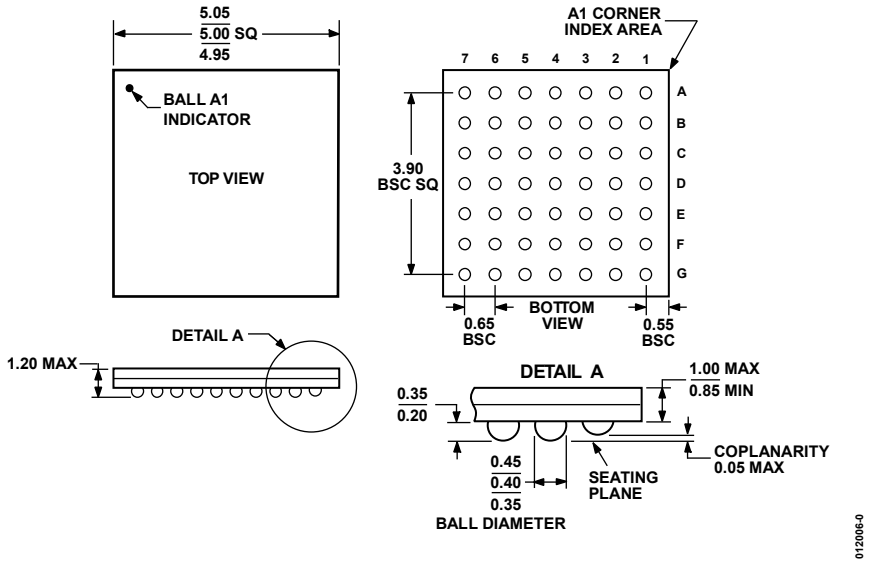


Figure 101. 49-Ball Chip Scale Package Ball Grid Array [CSP_BGA]
(BC-49-1)
Dimensions shown in millimeters

Model[1, 2]	ADC Channels[3]	DAC Channels	FLASH/ RAM	GPIO	Down-loader	Temperature Range	Package Description	Package Option	Ordering Quantity
EVAL-ADuC7020MKZ							ADuC7020 MiniKit		
EVAL-ADuC7020QSZ							ADuC7020 QuickStart Development System		
EVAL-ADuC7020QSPZ							ADuC7020 QuickStart Development System		
EVAL-ADuC7024QSZ							ADuC7024 QuickStart Development System		
EVAL-ADuC7026QSZ							ADuC7026 QuickStar Development System		
EVAL-ADuC7026QSPZ							ADuC7026 QuickStart Plus Development System		
EVAL-ADuC7028QSZ							ADuC7028 QuickStart Development System		
EVAL-ADUC7029QSZ							ADuC7029 QuickStart Development System		

[1] Z = RoHS Compliant Part.
[2] Models ADuC7026 and ADuC7027 include an external memory interface.
[3] One of the ADC channels is internally buffered for ADuC7019 models.

I²C refers to a communications protocol originally developed by Phillips Semiconductors (now NXP Semiconductors).