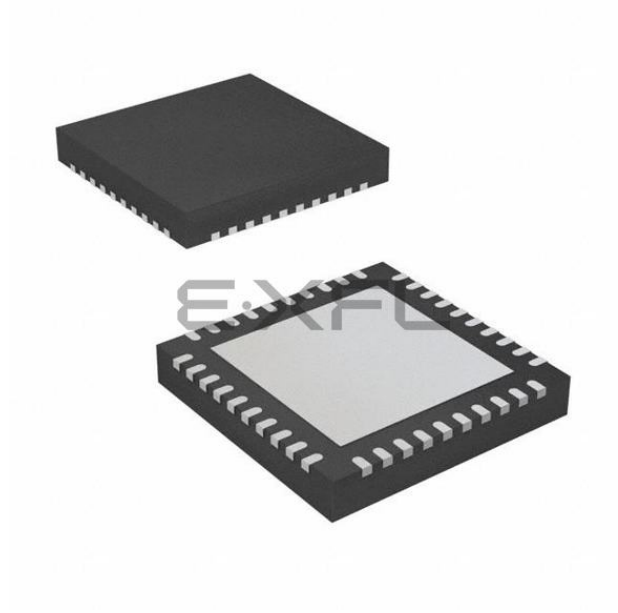

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	44MHz
Connectivity	EBI/EMI, I²C, SPI, UART/USART
Peripherals	PLA, PWM, PSM, Temp Sensor, WDT
Number of I/O	13
Program Memory Size	32KB (16K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 32
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	40-VFQFN Exposed Pad, CSP
Supplier Device Package	40-LFCSP-VQ (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/aduc7021bcpz32-rl7

GENERAL DESCRIPTION

The ADuC7019/20/21/22/24/25/26/27/28/29 are fully integrated, 1 MSPS, 12-bit data acquisition systems incorporating high performance multichannel ADCs, 16-bit/32-bit MCUs, and Flash®/EE memory on a single chip.

The ADC consists of up to 12 single-ended inputs. An additional four inputs are available but are multiplexed with the four DAC output pins. The four DAC outputs are available only on certain models (ADuC7020, ADuC7026, ADuC7028, and ADuC7029). However, in many cases where the DAC outputs are not present, these pins can still be used as additional ADC inputs, giving a maximum of 16 ADC input channels. The ADC can operate in single-ended or differential input mode. The ADC input voltage is 0 V to V_{REF}. A low drift band gap reference, temperature sensor, and voltage comparator complete the ADC peripheral set.

Depending on the part model, up to four buffered voltage output DACs are available on-chip. The DAC output range is programmable to one of three voltage ranges.

The devices operate from an on-chip oscillator and a PLL generating an internal high frequency clock of 41.78 MHz (UCLK). This clock is routed through a programmable clock divider from which the MCU core clock operating frequency is generated. The microcontroller core is an ARM7TDMI®, 16-bit/32-bit RISC machine, which offers up to 41 MIPS peak performance. Eight kilobytes of SRAM and 62 kilobytes of nonvolatile Flash/EE memory are provided on-chip. The ARM7TDMI core views all memory and registers as a single linear array.

On-chip factory firmware supports in-circuit serial download via the UART or I²C serial interface port; nonintrusive emulation is also supported via the JTAG interface. These features are incorporated into a low cost QuickStart™ development system supporting this MicroConverter® family.

The parts operate from 2.7 V to 3.6 V and are specified over an industrial temperature range of −40°C to +125°C. When operating at 41.78 MHz, the power dissipation is typically 120 mW. The ADuC7019/20/21/22/24/25/26/27/28/29 are available in a variety of memory models and packages (see Ordering Guide).

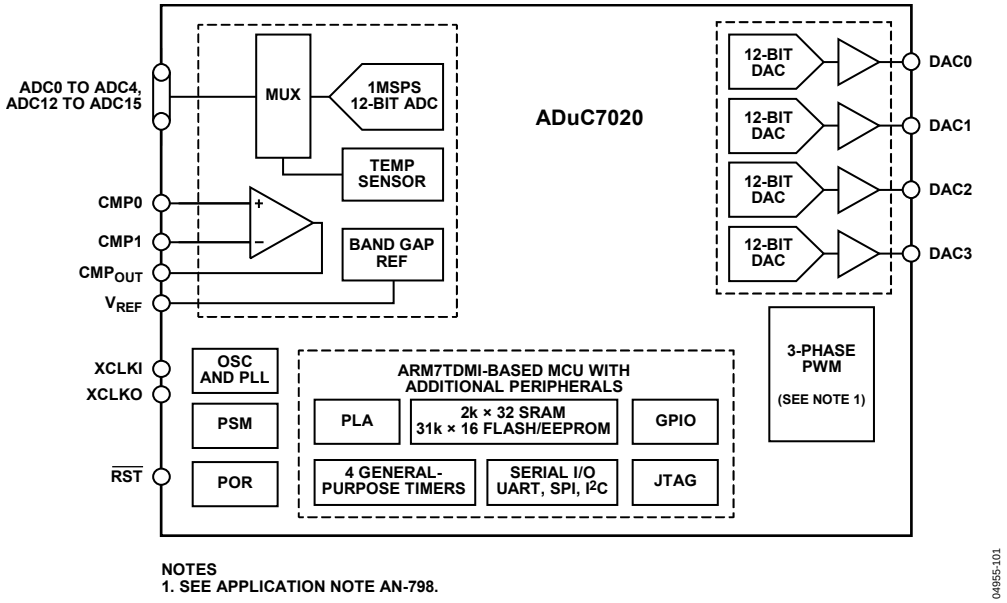


Figure 2.

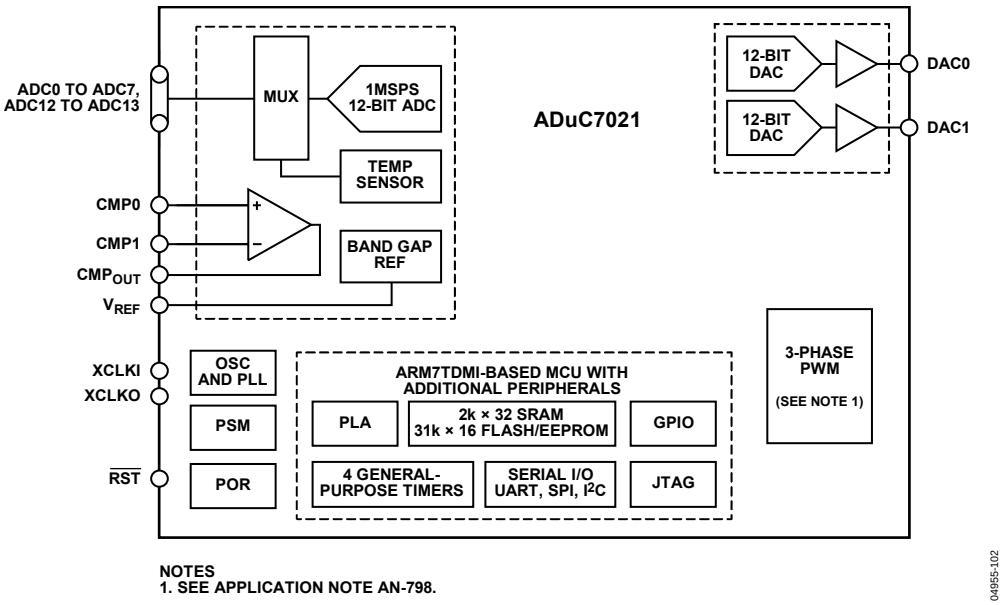


Figure 3.

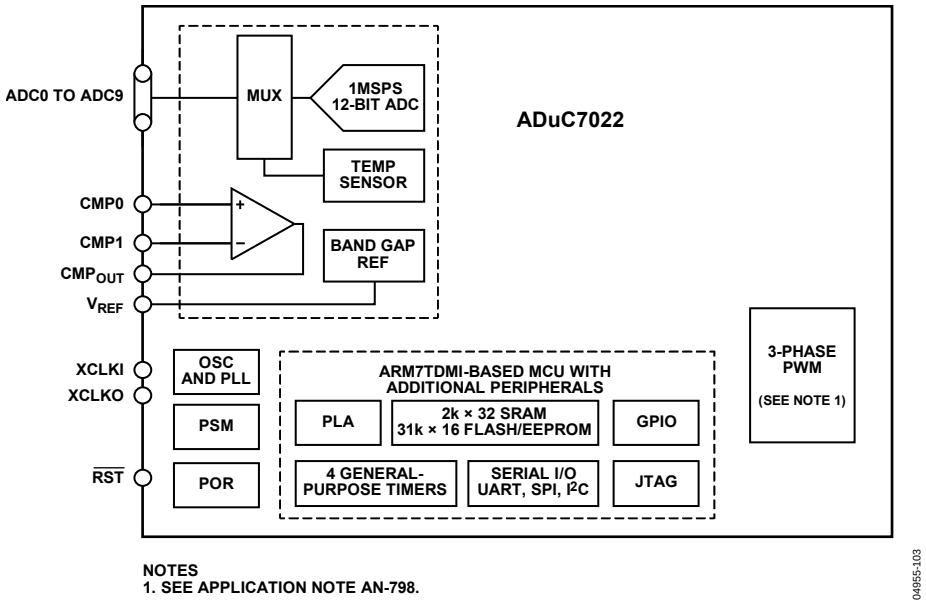


Figure 4.

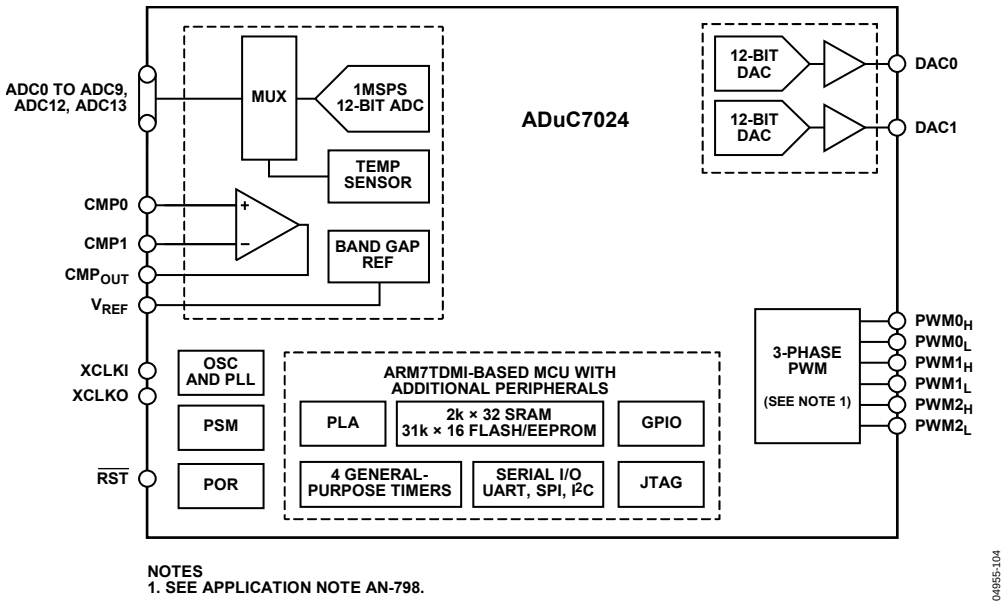


Figure 5.

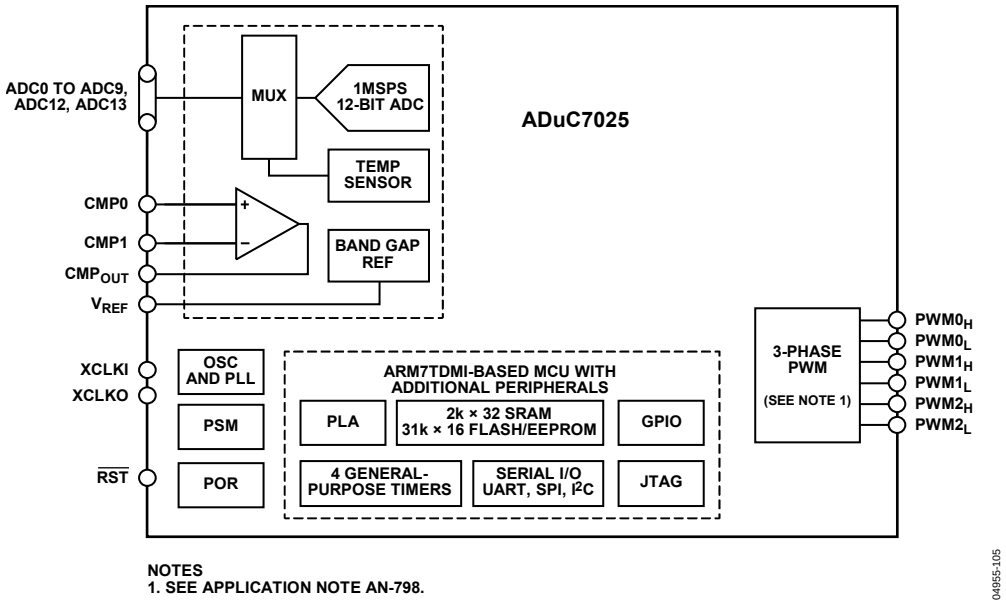


Figure 6.

SPECIFICATIONS

AV_{DD} = IOV_{DD} = 2.7 V to 3.6 V, V_{REF} = 2.5 V internal reference, f_{CORE} = 41.78 MHz, T_A = −40°C to +125°C, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
ADC CHANNEL SPECIFICATIONS					Eight acquisition clocks and fADC/2
ADC Power-Up Time		5		µs	
DC Accuracy[1, 2]					
Resolution	12			Bits	
Integral Nonlinearity		±0.6	±1.5	LSB	2.5 V internal reference
		±1.0		LSB	1.0 V external reference
Differential Nonlinearity[3, 4]		±0.5	+1/−0.9	LSB	2.5 V internal reference
		+0.7/−0.6		LSB	1.0 V external reference
DC Code Distribution		1		LSB	ADC input is a dc voltage
ENDPOINT ERRORS[5]					
Offset Error		±1	±2	LSB	
Offset Error Match		±1		LSB	
Gain Error		±2	±5	LSB	
Gain Error Match		±1		LSB	
DYNAMIC PERFORMANCE					f_{IN} = 10 kHz sine wave, f_{SAMPLE} = 1 MSPS
Signal-to-Noise Ratio (SNR)		69		dB	Includes distortion and noise components
Total Harmonic Distortion (THD)		−78		dB	
Peak Harmonic or Spurious Noise (PHSN)		−75		dB	
Channel-to-Channel Crosstalk		−80		dB	Measured on adjacent channels
ANALOG INPUT					
Input Voltage Ranges					
Differential Mode			V_{CM}[6] ± V_{REF}/2	V	
Single-Ended Mode			0 to V_{REF}	V	
Leakage Current		±1	±6	µA	
Input Capacitance		20		pF	During ADC acquisition
ON-CHIP VOLTAGE REFERENCE					0.47 µF from V_{REF} to AGND
Output Voltage		2.5		V	
Accuracy			±5	mV	T_A = 25°C
Reference Temperature Coefficient		±40		ppm/°C	
Power Supply Rejection Ratio		75		dB	
Output Impedance		70		Ω	T_A = 25°C
Internal V_{REF} Power-On Time		1		ms	
EXTERNAL REFERENCE INPUT					
Input Voltage Range	0.625		AV_{DD}	V	
DAC CHANNEL SPECIFICATIONS					R_L = 5 kΩ, C_L = 100 pF
DC Accuracy[7]					
Resolution		12		Bits	
Relative Accuracy		±2		LSB	
Differential Nonlinearity			±1	LSB	Guaranteed monotonic
Offset Error			±15	mV	2.5 V internal reference
Gain Error[8]			±1	%	
Gain Error Mismatch		0.1		%	% of full scale on DAC0
ANALOG OUTPUTS					
Output Voltage Range_0		0 to DAC_{REF}		V	DAC_{REF} range: DACGND to $DACV_{DD}$
Output Voltage Range_1		0 to 2.5		V	
Output Voltage Range_2		0 to $DACV_{DD}$		V	
Output Impedance		2		Ω	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DAC AC CHARACTERISTICS					
Voltage Output Settling Time		10		µs	
Digital-to-Analog Glitch Energy		±20		nV-sec	1 LSB change at major carry (where maximum number of bits simultaneously changes in the DACxDAT register)
COMPARATOR					
Input Offset Voltage		±15		mV	
Input Bias Current		1		µA	
Input Voltage Range	AGND		AV_{DD} – 1.2	V	
Input Capacitance		7		pF	
Hysteresis[4, 6]	2		15	mV	Hysteresis turned on or off via the CMPHYST bit in the CMPCON register
Response Time		3		µs	100 mV overdrive and configured with CMPRES = 11
TEMPERATURE SENSOR					
Voltage Output at 25°C		780		mV	
Voltage TC		−1.3		mV/°C	
Accuracy		±3		°C	
POWER SUPPLY MONITOR (PSM)					
IOV_{DD} Trip Point Selection		2.79		V	Two selectable trip points
		3.07		V	
Power Supply Trip Point Accuracy		±2.5		%	Of the selected nominal trip point voltage
POWER-ON-RESET		2.36		V	
GLITCH IMMUNITY ON RESET PIN[4]		50		µs	
WATCHDOG TIMER (WDT)					
Timeout Period	0		512	sec	
FLASH/EE MEMORY					
Endurance[9]	10,000			Cycles	
Data Retention[10]	20			Years	T_J = 85°C
DIGITAL INPUTS					All digital inputs excluding XCLKI and XCLKO
Logic 1 Input Current		±0.2	±1	µA	V_{IH} = IOV_{DD} or V_{IH} = 5 V
Logic 0 Input Current		−40	−60	µA	V_{IL} = 0 V; except TDI on ADuC7019/20/21/22/24/25/29
		−80	−120	µA	V_{IL} = 0 V; TDI on ADuC7019/20/21/22/24/25/29
Input Capacitance		10		pF	
LOGIC INPUTS[3]					All logic inputs excluding XCLKI
V_{INL}, Input Low Voltage			0.8	V	
V_{INH}, Input High Voltage	2.0			V	
LOGIC OUTPUTS					All digital outputs excluding XCLKO
V_{OH}, Output High Voltage	2.4			V	I_{SOURCE} = 1.6 mA
V_{OL}, Output Low Voltage[11]			0.4	V	I_{SINK} = 1.6 mA
CRYSTAL INPUTS XCLKI and XCLKO					
Logic Inputs, XCLKI Only					
V_{INL}, Input Low Voltage		1.1		V	
V_{INH}, Input High Voltage		1.7		V	
XCLKI Input Capacitance		20		pF	
XCLKO Output Capacitance		20		pF	
INTERNAL OSCILLATOR		32.768		kHz	
			±3	%	
			±2[4]	%	T_A = 0°C to 85°C range

Table 9. SPI Slave Mode Timing (Phase Mode = 0)

Parameter	Description	Min	Typ	Max	Unit
$t_{\overline{CS}}$	$\overline{CS}$ to SCLK edge[1]	$(2 \times t_{HCLK}) + (2 \times t_{UCLK})$			ns
t_{SL}	SCLK low pulse width[2]		$(SPIDIV + 1) \times t_{HCLK}$		ns
t_{SH}	SCLK high pulse width[2]		$(SPIDIV + 1) \times t_{HCLK}$		ns
t_{DAV}	Data output valid after SCLK edge			25	ns
t_{DSU}	Data input setup time before SCLK edge[1]	$1 \times t_{UCLK}$			ns
t_{DHD}	Data input hold time after SCLK edge[1]	$2 \times t_{UCLK}$			ns
t_{DF}	Data output fall time		5	12.5	ns
t_{DR}	Data output rise time		5	12.5	ns
t_{SR}	SCLK rise time		5	12.5	ns
t_{SF}	SCLK fall time		5	12.5	ns
t_{DOCS}	Data output valid after $\overline{CS}$ edge			25	ns
t_{SFS}	$\overline{CS}$ high after SCLK edge	0			ns

[1] t_{UCLK} = 23.9 ns. It corresponds to the 41.78 MHz internal clock from the PLL before the clock divider; see Figure 67.
[2] t_{HCLK} depends on the clock divider or CD bits in the POWCONMMR. $t_{HCLK} = t_{UCLK}/2^{CD}$; see Figure 67.

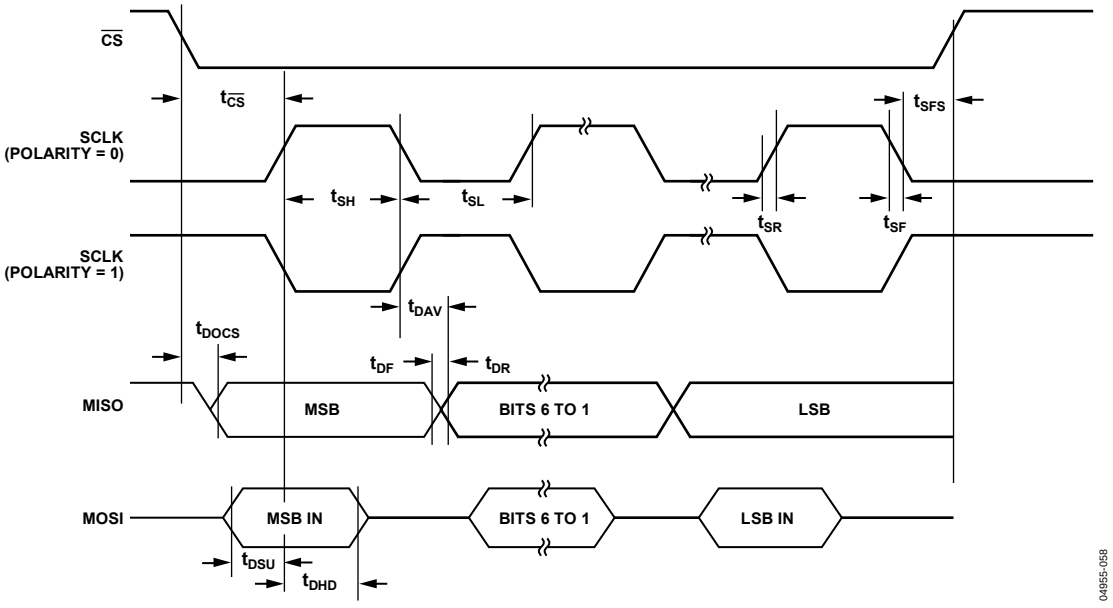


Figure 18. SPI Slave Mode Timing (Phase Mode = 0)

Pin No.	Mnemonic	Description
D7	P1.6/SPM6/PLAI[6]	Serial Port Multiplexed. General-Purpose Input and Output Port 1.6/UART, SPI/Programmable Logic Array Input Element 6.
D8	IOV_{DD}	3.3 V Supply for GPIO (see Table 78) and Input of the On-Chip Voltage Regulator.
E1	DAC3/ADC15	DAC3 Voltage Output/ADC Input 15.
E2	DAC2/ADC14	DAC2 Voltage Output/ADC Input 14.
E3	DAC1/ADC13	DAC1 Voltage Output/ADC Input 13.
E4	P3.0/$PWM0_H$/PLAI[8]	General-Purpose Input and Output Port 3.0/PWM Phase 0 High-Side Output/Programmable Logic Array Input Element 8.
E5	P3.2/$PWM1_H$/PLAI[10]	General-Purpose Input and Output Port 3.2/PWM Phase 1 High-Side Output/Programmable Logic Array Input Element 10.
E6	P1.5/SPM5/PLAI[5]/IRQ3	Serial Port Multiplexed. General-Purpose Input and Output Port 1.5/UART, SPI/Programmable Logic Array Input Element 5/External Interrupt Request 3, Active High.
E7	P3.7/PWM_{SYNC}/PLAI[15]	General-Purpose Input and Output Port 3.7/PWM Synchronization/Programmable Logic Array Input Element 15.
E8	XCLKI	Input to the Crystal Oscillator Inverter and Input to the Internal Clock Generator Circuits.
F1	P4.6/PLAO[14]	General-Purpose Input and Output Port 4.6/Programmable Logic Array Output Element 14.
F2	TDI	JTAG Test Port Input, Test Data In. Debug and download access.
F3	DAC0/ADC12	DAC0 Voltage Output/ADC Input 12.
F4	P3.1/$PWM0_L$/PLAI[9]	General-Purpose Input and Output Port 3.1/PWM Phase 0 Low-Side Output/Programmable Logic Array Input Element 9.
F5	P3.3/$PWM1_L$/PLAI[11]	General-Purpose Input and Output Port 3.3/PWM Phase 1 Low-Side Output/Programmable Logic Array Input Element 11.
F6	$\overline{RST}$	Reset Input, Active Low.
F7	P0.7/ECLK/XCLK/SPM8/PLAO[4]	Serial Port Multiplexed. General-Purpose Input and Output Port 0.7/Output for External Clock Signal/Input to the Internal Clock Generator Circuits/UART/Programmable Logic Array Output Element 4.
F8	XCLKO	Output from the Crystal Oscillator Inverter.
G1	BM/P0.0/CMP_{OUT}/PLAI[7]	Multifunction I/O Pin. Boot mode. The ADuC7028 enters UART download mode if BM is low at reset and executes code if BM is pulled high at reset through a 1 kΩ resistor/General-Purpose Input and Output Port 0.0/Voltage Comparator Output/Programmable Logic Array Input Element 7.
G2	P4.7/PLAO[15]	General-Purpose Input and Output Port 4.7/Programmable Logic Array Output Element 15.
G3	TMS	JTAG Test Port Input, Test Mode Select. Debug and download access.
G4	TDO	JTAG Test Port Output, Test Data Out. Debug and download access.
G5	P0.3/TRST/ADC_{BUSY}	General-Purpose Input and Output Port 0.3/JTAG Test Port Input, Test Reset/ADC_{BUSY} Signal Output.
G6	P3.4/$PWM2_H$/PLAI[12]	General-Purpose Input and Output Port 3.4/PWM Phase 2 High-Side Output/Programmable Logic Array Input 12.
G7	P3.5/$PWM2_L$/PLAI[13]	General-Purpose Input and Output Port 3.5/PWM Phase 2 Low-Side Output/Programmable Logic Array Input Element 13.
G8	P2.0/SPM9/PLAO[5]/$\overline{CONV_{START}}$	Serial Port Multiplexed. General-Purpose Input and Output Port 2.0/UART/Programmable Logic Array Output Element 5/Start Conversion Input Signal for ADC.
H1	P0.6/T1/MRST/PLAO[3]	Multifunction Pin, Driven Low After Reset. General-Purpose Output Port 0.6/Timer1 Input/Power-On Reset Output/Programmable Logic Array Output Element 3.
H2	TCK	JTAG Test Port Input, Test Clock. Debug and download access.
H3	IOGND	Ground for GPIO (see Table 78). Typically connected to DGND.
H4	IOV_{DD}	3.3 V Supply for GPIO (see Table 78) and Input of the On-Chip Voltage Regulator.
H5	LV_{DD}	2.6 V Output of the On-Chip Voltage Regulator. This output must be connected to a 0.47 µF capacitor to DGND only.
H6	DGND	Ground for Core Logic.
H7	IRQ0/P0.4/PWM_{TRIP}/PLAO[1]	Multifunction I/O Pin. External Interrupt Request 0, Active High/General-Purpose Input and Output Port 0.4/PWM Trip External Input/Programmable Logic Array Output Element 1.
H8	IRQ1/P0.5/ADC_{BUSY}/PLAO[2]	Multifunction I/O Pin. External Interrupt Request 1, Active High/General-Purpose Input and Output Port 0.5/ADC_{BUSY} Signal Output/Programmable Logic Array Output Element 2.

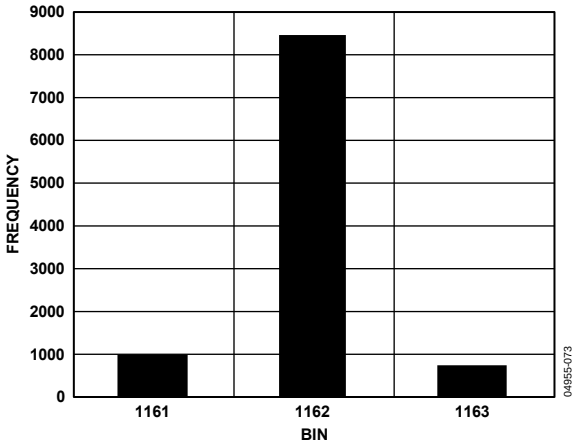


Figure 34. Code Histogram Plot, fs = 774 kSPS, V_{IN} = 0.7 V

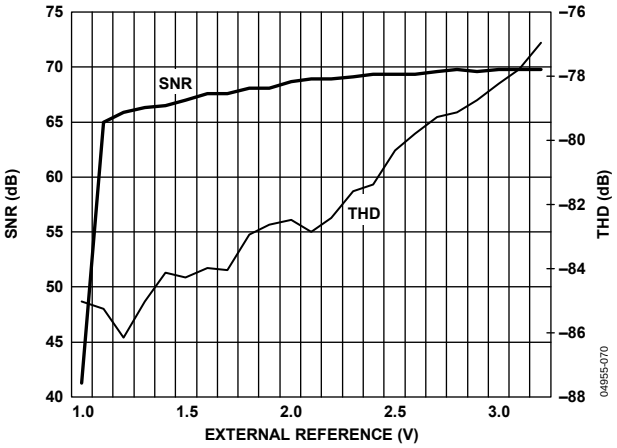


Figure 37. Typical Dynamic Performance vs. V_{REF}

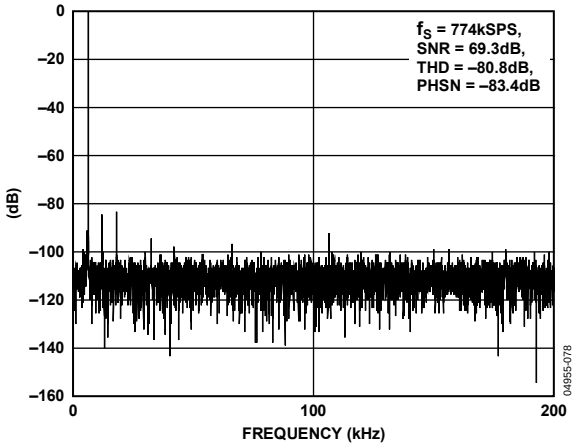


Figure 35. Dynamic Performance, f_S = 774 kSPS

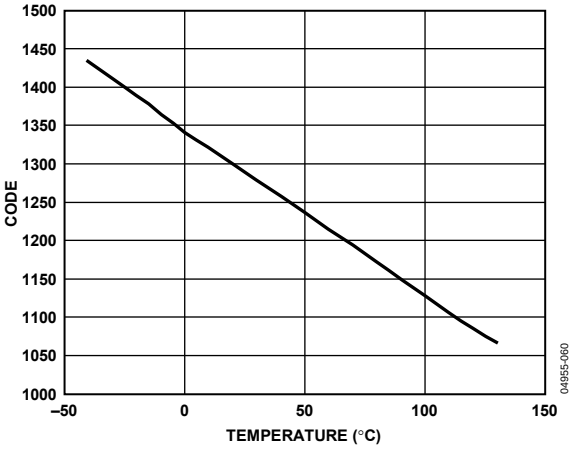


Figure 38. On-Chip Temperature Sensor Voltage Output vs. Temperature

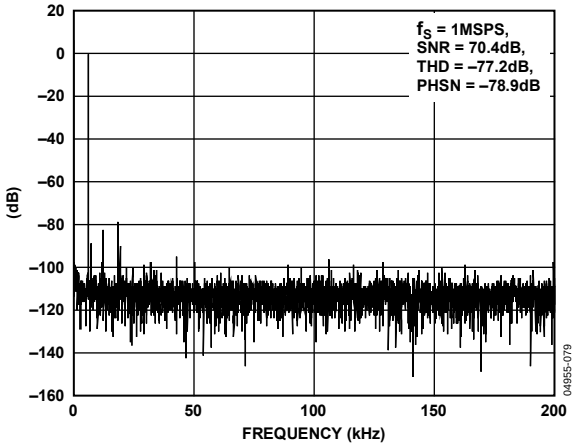


Figure 36. Dynamic Performance, f_S = 1 MSPS

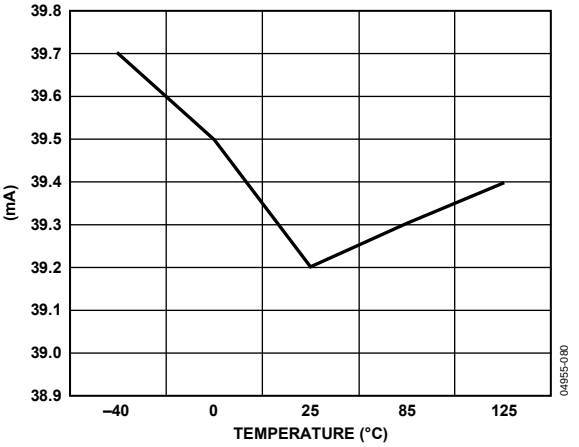


Figure 39. Current Consumption vs. Temperature @ CD = 0

Address	Name	Byte	Access Type	Default Value	Page
Reference Address Base = 0xFFFF0480					
0x048C	REFCON	1	R/W	0x00	50
ADC Address Base = 0xFFFF0500					
0x0500	ADCCON	2	R/W	0x0600	46
0x0504	ADCCP	1	R/W	0x00	47
0x0508	ADCCN	1	R/W	0x01	47
0x050C	ADCSTA	1	R	0x00	48
0x0510	ADCDAT	4	R	0x00000000	48
0x0514	ADCRST	1	R/W	0x00	48
0x0530	ADCGN	2	R/W	0x0200	48
0x0534	ADCOF	2	R/W	0x0200	48
DAC Address Base = 0xFFFF0600					
0x0600	DAC0CON	1	R/W	0x00	56
0x0604	DAC0DAT	4	R/W	0x00000000	56
0x0608	DAC1CON	1	R/W	0x00	56
0x060C	DAC1DAT	4	R/W	0x00000000	56
0x0610	DAC2CON	1	R/W	0x00	56
0x0614	DAC2DAT	4	R/W	0x00000000	56
0x0618	DAC3CON	1	R/W	0x00	56
0x061C	DAC3DAT	4	R/W	0x00000000	56
UART Base Address = 0xFFFF0700					
0x0700	COMTX	1	R/W	0x00	71
	COMRX	1	R	0x00	71
	COMDIV0	1	R/W	0x00	71
0x0704	COMIEN0	1	R/W	0x00	71
	COMDIV1	1	R/W	0x00	72
0x0708	COMIID0	1	R	0x01	72
0x070C	COMCON0	1	R/W	0x00	72
0x0710	COMCON1	1	R/W	0x00	72
0x0714	COMSTA0	1	R	0x60	72
0x0718	COMSTA1	1	R	0x00	73
0x071C	COMSCR	1	R/W	0x00	73
0x0720	COMIEN1	1	R/W	0x04	73
0x0724	COMIID1	1	R	0x01	73
0x0728	COMADR	1	R/W	0xAA	74
0x072C	COMDIV2	2	R/W	0x0000	73

Address	Name	Byte	Access Type	Default Value	Page
I2C0 Base Address = 0xFFFF0800					
0x0800	I2C0MSTA	1	R/W	0x00	76
0x0804	I2C0SSTA	1	R	0x01	76
0x0808	I2C0SRX	1	R	0x00	77
0x080C	I2C0STX	1	W	0x00	77
0x0810	I2C0MRX	1	R	0x00	77
0x0814	I2C0MTX	1	W	0x00	77
0x0818	I2C0CNT	1	R/W	0x00	77
0x081C	I2C0ADR	1	R/W	0x00	77
0x0824	I2C0BYTE	1	R/W	0x00	77
0x0828	I2C0ALT	1	R/W	0x00	78
0x082C	I2C0CFG	1	R/W	0x00	78
0x0830	I2C0DIV	2	R/W	0x1F1F	79
0x0838	I2C0ID0	1	R/W	0x00	79
0x083C	I2C0ID1	1	R/W	0x00	79
0x0840	I2C0ID2	1	R/W	0x00	79
0x0844	I2C0ID3	1	R/W	0x00	79
0x0848	I2C0CCNT	1	R/W	0x01	79
0x084C	I2C0FSTA	2	R/W	0x0000	79
I2C1 Base Address = 0xFFFF0900					
0x0900	I2C1MSTA	1	R/W	0x00	76
0x0904	I2C1SSTA	1	R	0x01	76
0x0908	I2C1SRX	1	R	0x00	77
0x090C	I2C1STX	1	W	0x00	77
0x0910	I2C1MRX	1	R	0x00	77
0x0914	I2C1MTX	1	W	0x00	77
0x0918	I2C1CNT	1	R/W	0x00	77
0x091C	I2C1ADR	1	R/W	0x00	77
0x0924	I2C1BYTE	1	R/W	0x00	77
0x0928	I2C1ALT	1	R/W	0x00	78
0x092C	I2C1CFG	1	R/W	0x00	78
0x0930	I2C1DIV	2	R/W	0x1F1F	79
0x0938	I2C1ID0	1	R/W	0x00	79
0x093C	I2C1ID1	1	R/W	0x00	79
0x0940	I2C1ID2	1	R/W	0x00	79
0x0944	I2C1ID3	1	R/W	0x00	79
0x0948	I2C1CCNT	1	R/W	0x01	79
0x094C	I2C1FSTA	2	R/W	0x0000	79
SPI Base Address = 0xFFFF0A00					
0x0A00	SPISTA	1	R	0x00	75
0x0A04	SPIRX	1	R	0x00	75
0x0A08	SPITX	1	W	0x00	75
0x0A0C	SPIDIV	1	R/W	0x1B	75
0x0A10	SPICON	2	R/W	0x0000	75

Address	Name	Byte	Access Type	Default Value	Page
PLA Base Address = 0xFFFF0B00					
0x0B00	PLAELM0	2	R/W	0x0000	80
0x0B04	PLAELM1	2	R/W	0x0000	80
0x0B08	PLAELM2	2	R/W	0x0000	80
0x0B0C	PLAELM3	2	R/W	0x0000	80
0x0B10	PLAELM4	2	R/W	0x0000	80
0x0B14	PLAELM5	2	R/W	0x0000	80
0x0B18	PLAELM6	2	R/W	0x0000	80
0x0B1C	PLAELM7	2	R/W	0x0000	80
0x0B20	PLAELM8	2	R/W	0x0000	80
0x0B24	PLAELM9	2	R/W	0x0000	80
0x0B28	PLAELM10	2	R/W	0x0000	80
0x0B2C	PLAELM11	2	R/W	0x0000	80
0x0B30	PLAELM12	2	R/W	0x0000	80
0x0B34	PLAELM13	2	R/W	0x0000	80
0x0B38	PLAELM14	2	R/W	0x0000	80
0x0B3C	PLAELM15	2	R/W	0x0000	80
0x0B40	PLACLK	1	R/W	0x00	81
0x0B44	PLAIRQ	4	R/W	0x00000000	81
0x0B48	PLAADC	4	R/W	0x00000000	82
0x0B4C	PLADIN	4	R/W	0x00000000	82
0x0B50	PLADOUT	4	R	0x00000000	82
0x0B54	PLALCK	1	W	0x00	82
External Memory Base Address = 0xFFFFF000					
0xF000	XMCFG	1	R/W	0x00	90
0xF010	XM0CON	1	R/W	0x00	90
0xF014	XM1CON	1	R/W	0x00	90
0xF018	XM2CON	1	R/W	0x00	90
0xF01C	XM3CON	1	R/W	0x00	90
0xF020	XM0PAR	2	R/W	0x70FF	90
0xF024	XM1PAR	2	R/W	0x70FF	90
0xF028	XM2PAR	2	R/W	0x70FF	90
0xF02C	XM3PAR	2	R/W	0x70FF	90

Address	Name	Byte	Access Type	Default Value	Page
GPIO Base Address = 0xFFFFF400					
0xF400	GP0CON	4	R/W	0x00000000	68
0xF404	GP1CON	4	R/W	0x00000000	68
0xF408	GP2CON	4	R/W	0x00000000	68
0xF40C	GP3CON	4	R/W	0x00000000	68
0xF410	GP4CON	4	R/W	0x00000000	68
0xF420	GP0DAT	4	R/W	0x000000XX[1]	70
0xF424	GP0SET	4	W	0x000000XX[1]	70
0xF428	GP0CLR	4	W	0x000000XX[1]	70
0xF42C	GP0PAR	4	R/W	0x20000000	68
0xF430	GP1DAT	4	R/W	0x000000XX[1]	69
0xF434	GP1SET	4	W	0x000000XX[1]	70
0xF438	GP1CLR	4	W	0x000000XX[1]	70
0xF43C	GP1PAR	4	R/W	0x00000000	68
0xF440	GP2DAT	4	R/W	0x000000XX[1]	69
0xF444	GP2SET	4	W	0x000000XX[1]	70
0xF448	GP2CLR	4	W	0x000000XX[1]	70
0xF450	GP3DAT	4	R/W	0x000000XX[1]	69
0xF454	GP3SET	4	W	0x000000XX[1]	70
0xF458	GP3CLR	4	W	0x000000XX[1]	70
0xF460	GP4DAT	4	R/W	0x000000XX[1]	69
0xF464	GP4SET	4	W	0x000000XX[1]	70
0xF468	GP4CLR	4	W	0x000000XX[1]	70

[1] X = 0, 1, 2, or 3.

Flash/EE Base Address = 0xFFFFF800					
0xF800	FEESTA	1	R	0x20	52
0xF804	FEEMOD	2	R/W	0x0000	52
0xF808	FEECON	1	R/W	0x07	53
0xF80C	FEEDAT	2	R/W	0xXXXX[1]	53
0xF810	FEEADR	2	R/W	0x0000	53
0xF818	FEESIGN	3	R	0xFFFFFF	53
0xF81C	FEEPRO	4	R/W	0x00000000	53
0xF820	FEEHIDE	4	R/W	0xFFFFFFFF	53

[1] X = 0, 1, 2, or 3.

PWM Base Address = 0xFFFFFC00					
0xFC00	PWMCON	2	R/W	0x0000	66
0xFC04	PWMSTA	2	R/W	0x0000	66
0xFC08	PWMDAT0	2	R/W	0x0000	67
0xFC0C	PWMDAT1	2	R/W	0x0000	67
0xFC10	PWMCFG	2	R/W	0x0000	67
0xFC14	PWMCH0	2	R/W	0x0000	67
0xFC18	PWMCH1	2	R/W	0x0000	67
0xFC1C	PWMCH2	2	R/W	0x0000	67
0xFC20	PWMEN	2	R/W	0x0000	67
0xFC24	PWMDAT2	2	R/W	0x0000	67

Table 22. ADCCN MMR Bit Designation

Bit	Value	Description
7:5		Reserved.
4:0		Negative channel selection bits.
	00000	ADC0.
	00001	ADC1.
	00010	ADC2.
	00011	ADC3.
	00100	ADC4.
	00101	ADC5.
	00110	ADC6.
	00111	ADC7.
	01000	ADC8.
	01001	ADC9.
	01010	ADC10.
	01011	ADC11.
	01100	DAC0/ADC12.
	01101	DAC1/ADC13.
	01110	DAC2/ADC14.
	01111	DAC3/ADC15.
	10000	Internal reference (self-diagnostic feature).
	Others	Reserved.

Table 23. ADCSTA Register

Name	Address	Default Value	Access
ADCSTA	0xFFFF050C	0x00	R

ADCSTA is an ADC status register that indicates when an ADC conversion result is ready. The ADCSTA register contains only one bit, ADCReady (Bit 0), representing the status of the ADC. This bit is set at the end of an ADC conversion, generating an ADC interrupt. It is cleared automatically by reading the ADCDAT MMR. When the ADC is performing a conversion, the status of the ADC can be read externally via the ADC_{BUSY} pin. This pin is high during a conversion. When the conversion is finished, ADC_{BUSY} goes back low. This information can be available on P0.5 (see the General-Purpose Input/Output section) if enabled in the ADCCON register.

Table 24. ADCDAT Register

Name	Address	Default Value	Access
ADCDAT	0xFFFF0510	0x00000000	R

ADCDAT is an ADC data result register. It holds the 12-bit ADC result as shown in Figure 51.

Table 25. ADCRST Register

Name	Address	Default Value	Access
ADCRST	0xFFFF0514	0x00	R/W

ADCRST resets the digital interface of the ADC. Writing any value to this register resets all the ADC registers to their default values.

Table 26. ADCGN Register

Name	Address	Default Value	Access
ADCGN	0xFFFF0530	0x0200	R/W

ADCGN is a 10-bit gain calibration register.

Table 27. ADCOF Register

Name	Address	Default Value	Access
ADCOF	0xFFFF0534	0x0200	R/W

ADCOF is a 10-bit offset calibration register.

CONVERTER OPERATION

The ADC incorporates a successive approximation (SAR) architecture involving a charge-sampled input stage. This architecture can operate in three modes: differential, pseudo differential, and single-ended.

Differential Mode

The ADuC7019/20/21/22/24/25/26/27/28/29 each contain a successive approximation ADC based on two capacitive DACs. Figure 54 and Figure 55 show simplified schematics of the ADC in acquisition and conversion phase, respectively. The ADC comprises control logic, a SAR, and two capacitive DACs. In Figure 54 (the acquisition phase), SW3 is closed and SW1 and SW2 are in Position A. The comparator is held in a balanced condition, and the sampling capacitor arrays acquire the differential signal on the input.

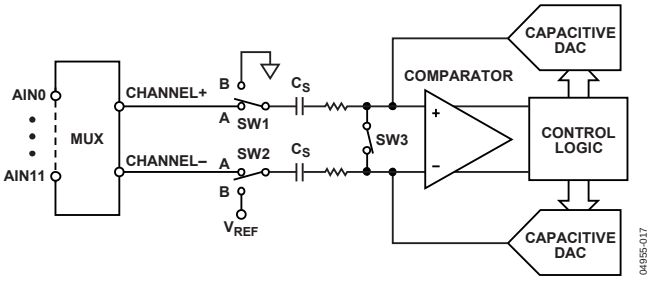


Figure 54. ADC Acquisition Phase

When the ADC starts a conversion, as shown in Figure 55, SW3 opens, and then SW1 and SW2 move to Position B. This causes the comparator to become unbalanced. Both inputs are disconnected once the conversion begins. The control logic and the charge redistribution DACs are used to add and subtract fixed amounts of charge from the sampling capacitor arrays to bring the comparator back into a balanced condition. When the comparator is rebalanced, the conversion is complete. The control logic generates the ADC output code. The output impedances of the sources driving the V_{IN+} and V_{IN-} input voltage pins must be matched; otherwise, the two inputs have different settling times, resulting in errors.

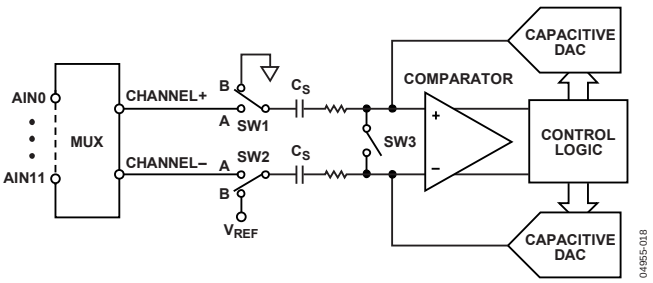


Figure 55. ADC Conversion Phase

Table 35. FEECON Register

Name	Address	Default Value	Access
FEECON	0xFFFFF808	0x07	R/W

FEECON is an 8-bit command register. The commands are described in Table 36.

Table 36. Command Codes in FEECON

Code	Command	Description
0x00[1]	Null	Idle state.
0x01[1]	Single read	Load FEEDAT with the 16-bit data. Indexed by FEEADR.
0x02[1]	Single write	Write FEEDAT at the address pointed to by FEEADR. This operation takes 50 μs.
0x03[1]	Erase/write	Erase the page indexed by FEEADR and write FEEDAT at the location pointed by FEEADR. This operation takes approximately 24 ms.
0x04[1]	Single verify	Compare the contents of the location pointed by FEEADR to the data in FEEDAT. The result of the comparison is returned in FEESTA, Bit 1.
0x05[1]	Single erase	Erase the page indexed by FEEADR.
0x06[1]	Mass erase	Erase 62 kB of user space. The 2 kB of kernel are protected. This operation takes 2.48 sec. To prevent accidental execution, a command sequence is required to execute this instruction. See the Command Sequence for Executing a Mass Erase section.
0x07	Reserved	Reserved.
0x08	Reserved	Reserved.
0x09	Reserved	Reserved.
0x0A	Reserved	Reserved.
0x0B	Signature	Give a signature of the 64 kB of Flash/EE in the 24-bit FEESIGN MMR. This operation takes 32,778 clock cycles.
0x0C	Protect	This command can run only once. The value of FEEPRO is saved and removed only with a mass erase (0x06) of the key.
0x0D	Reserved	Reserved.
0x0E	Reserved	Reserved.
0x0F	Ping	No operation; interrupt generated.

[1] The FEECON register always reads 0x07 immediately after execution of any of these commands.

Table 37. FEEDAT Register

Name	Address	Default Value	Access
FEEDAT	0xFFFFF80C	0xXXXX[1]	R/W

[1] X = 0, 1, 2, or 3.

FEEDAT is a 16-bit data register.

Table 38. FEEADR Register

Name	Address	Default Value	Access
FEEADR	0xFFFFF810	0x0000	R/W

FEEADR is another 16-bit address register.

Table 39. FEESIGN Register

Name	Address	Default Value	Access
FEESIGN	0xFFFFF818	0xFFFFFF	R

FEESIGN is a 24-bit code signature.

Table 40. FEEPRO Register

Name	Address	Default Value	Access
FEEPRO	0xFFFFF81C	0x00000000	R/W

FEEPRO MMR provides protection following a subsequent reset of the MMR. It requires a software key (see Table 42).

Table 41. FEEHIDE Register

Name	Address	Default Value	Access
FEEHIDE	0xFFFFF820	0xFFFFFFFF	R/W

FEEHIDE MMR provides immediate protection. It does not require any software key. Note that the protection settings in FEEHIDE are cleared by a reset (see Table 42).

Table 42. FEEPRO and FEEHIDE MMR Bit Designations

Bit	Description
31	Read protection. Cleared by user to protect all code. Set by user to allow reading the code.
30:0	Write protection for Page 123 to Page 120, Page 119 to Page 116, and Page 0 to Page 3. Cleared by user to protect the pages from writing. Set by user to allow writing the pages.

Command Sequence for Executing a Mass Erase

```
FEEDAT=0x3CFF;
FEEADR = 0xFFC3;
FEEMOD= FEEMOD|0x8;    //Erase key enable
FEECON=0x06;           //Mass erase command
```

MMRs and Keys

The operating mode, clocking mode, and programmable clock divider are controlled via two MMRs: PLLCON (see Table 61) and POWCON (see Table 64). PLLCON controls the operating mode of the clock system, whereas POWCON controls the core clock frequency and the power-down mode.

To prevent accidental programming, a certain sequence (see Table 65) must be followed to write to the PLLCON and POWCON registers.

Table 59. PLLKEYx Registers

Name	Address	Default Value	Access
PLLKEY1	0xFFFF0410	0x0000	W
PLLKEY2	0xFFFF0418	0x0000	W

Table 60. PLLCON Register

Name	Address	Default Value	Access
PLLCON	0xFFFF0414	0x21	R/W

Table 61. PLLCON MMR Bit Designations

Bit	Name	Value	Description
7:6			Reserved.
5	OSEL		32 kHz PLL input selection. Set by user to select the internal 32 kHz oscillator. Set by default. Cleared by user to select the external 32 kHz crystal.
4:2			Reserved.
1:0	MDCLK		Clocking modes.
		00	Reserved.
		01	PLL. Default configuration.
		10	Reserved.
		11	External clock on the P0.7 pin.

Table 62. POWKEYx Registers

Name	Address	Default Value	Access
POWKEY1	0xFFFF0404	0x0000	W
POWKEY2	0xFFFF040C	0x0000	W

Table 63. POWCON Register

Name	Address	Default Value	Access
POWCON	0xFFFF0408	0x0003	R/W

Table 64. POWCON MMR Bit Designations

Bit	Name	Value	Description
7			Reserved.
6:4	PC		Operating modes.
		000	Active mode.
		001	Pause mode.
		010	Nap.
		011	Sleep mode. IRQ0 to IRQ3 and Timer2 can wake up the part.
		100	Stop mode. IRQ0 to IRQ3 can wake up the part.
		Others	Reserved.
3			Reserved.
2:0	CD		CPU clock divider bits.
		000	41.78 MHz.
		001	20.89 MHz.
		010	10.44 MHz.
		011	5.22 MHz.
		100	2.61 MHz.
		101	1.31 MHz.
		110	653 kHz.
		111	326 kHz.

Table 65. PLLCON and POWCON Write Sequence

PLLCON	POWCON
PLLKEY1 = 0xAA	POWKEY1 = 0x01
PLLCON = 0x01	POWCON = user value
PLLKEY2 = 0x55	POWKEY2 = 0xF4

Table 99. COMDIV1 Register

Name	Address	Default Value	Access
COMDIV1	0xFFFF0704	0x00	R/W

COMDIV1 is a divisor latch (high byte) register.

Table 100. COMIID0 Register

Name	Address	Default Value	Access
COMIID0	0xFFFF0708	0x01	R

COMIID0 is the interrupt identification register.

Table 101. COMIID0 MMR Bit Descriptions

Bit 2:1 Status Bits	Bit 0 NINT	Priority	Definition	Clearing Operation
00	1	N/A	No interrupt	N/A
11	0	1 (Highest)	Receive line status interrupt	Read COMSTA0
10	0	2	Receive buffer full interrupt	Read COMRX
01	0	3	Transmit buffer empty interrupt	Write data to COMTX or read COMIID0
00	0	4 (Lowest)	Modem status interrupt	Read COMSTA1

Table 102. COMCON0 Register

Name	Address	Default Value	Access
COMCON0	0xFFFF070C	0x00	R/W

COMCON0 is the line control register.

Table 103. COMCON0 MMR Bit Descriptions

Bit	Name	Description
7	DLAB	Divisor latch access. Set by user to enable access to the COMDIV0 and COMDIV1 registers. Cleared by user to disable access to COMDIV0 and COMDIV1 and enable access to COMRX and COMTX.
6	BRK	Set break. Set by user to force SOUT to 0. Cleared to operate in normal mode.
5	SP	Stick parity. Set by user to force parity to defined values: 1 if EPS = 1 and PEN = 1, 0 if EPS = 0 and PEN = 1.
4	EPS	Even parity select bit. Set for even parity. Cleared for odd parity.
3	PEN	Parity enable bit. Set by user to transmit and check the parity bit. Cleared by user for no parity transmission or checking.
2	STOP	Stop bit. Set by user to transmit 1.5 stop bits if the word length is five bits or 2 stop bits if the word length is six bits, seven bits, or eight bits. The receiver checks the first stop bit only, regardless of the number of stop bits selected. Cleared by user to generate 1 stop bit in the transmitted data.
1:0	WLS	Word length select: 00 = five bits, 01 = six bits, 10 = seven bits, 11 = eight bits.

Table 104. COMCON1 Register

Name	Address	Default Value	Access
COMCON1	0xFFFF0710	0x00	R/W

COMCON1 is the modem control register.

Table 105. COMCON1 MMR Bit Descriptions

Bit	Name	Description
7:5		Reserved.
4	LOOPBACK	Loopback. Set by user to enable loopback mode. In loopback mode, SOUT (see Table 78) is forced high. The modem signals are also directly connected to the status inputs (RTS to CTS and DTR to DSR). Cleared by user to be in normal mode.
3	PEN	Parity enable bit. Set by user to transmit and check the parity bit. Cleared by user for no parity transmission or checking.
2	STOP	Stop bit. Set by user to transmit 1.5 stop bits if the word length is five bits, or 2 stop bits if the word length is six bits, seven bits, or eight bits. The receiver checks the first stop bit only, regardless of the number of stop bits selected. Cleared by user to generate 1 stop bit in the transmitted data.
1	RTS	Request to send. Set by user to force the RTS output to 0. Cleared by user to force the RTS output to 1.
0	DTR	Data terminal ready. Set by user to force the DTR output to 0. Cleared by user to force the DTR output to 1.

Table 106. COMSTA0 Register

Name	Address	Default Value	Access
COMSTA0	0xFFFF0714	0x60	R

COMSTA0 is the line status register.

Table 107. COMSTA0 MMR Bit Descriptions

Bit	Name	Description
7		Reserved.
6	TEMT	COMTX and shift register empty status bit. Set automatically if COMTX and shift register are empty. Cleared automatically when writing to COMTX.
5	THRE	COMTX empty. Set automatically if COMTX is empty. Cleared automatically when writing to COMTX.
4	BI	Break error. Set when SIN is held low for more than the maximum word length. Cleared automatically.
3	FE	Framing error. Set when an invalid stop bit occurs. Cleared automatically.
2	PE	Parity error. Set when a parity error occurs. Cleared automatically.
1	OE	Overrun error. Set automatically if data is over-written before being read. Cleared automatically.
0	DR	Data ready. Set automatically when COMRX is full. Cleared by reading COMRX.

Table 129. I2C0SSTA MMR Bit Descriptions

Bit	Value	Description
31:15		Reserved. These bits should be written as 0.
14		Start decode bit. Set by hardware if the device receives a valid start plus matching address. Cleared by an I²C stop condition or an I²C general call reset.
13		Repeated start decode bit. Set by hardware if the device receives a valid repeated start and matching address. Cleared by an I²C stop condition, a read of the I2CSSTA register, or an I²C general call reset.
12:11		ID decode bits.
	00	Received Address Matched ID Register 0.
	01	Received Address Matched ID Register 1.
	10	Received Address Matched ID Register 2.
	11	Received Address Matched ID Register 3.
10		Stop after start and matching address interrupt. Set by hardware if the slave device receives an I²C stop condition after a previous I²C start condition and matching address. Cleared by a read of the I2C0SSTA register.
9:8		General call ID.
	00	No general call.
	01	General call reset and program address.
	10	General call program address.
	11	General call matching alternative ID.
7		General call interrupt. Set if the slave device receives a general call of any type. Cleared by setting Bit 8 of the I2CxCFG register. If it is a general call reset, all registers are at their default values. If it is a hardware general call, the Rx FIFO holds the second byte of the general call. This is similar to the I2C0ALT register (unless it is a general call to reprogram the device address). For more details, see the I²C bus specification, Version 2.1, January 2000.
6		Slave busy. Set automatically if the slave is busy. Cleared automatically.
5		No ACK. Set if master asking for data and no data is available. Cleared automatically by reading the I2C0SSTA register.
4		Slave receive FIFO overflow. Set automatically if the slave receive FIFO is overflowing. Cleared automatically by reading the I2C0SSTA register.
3		Slave receive IRQ. Set after receiving data. Cleared automatically by reading the I2C0SRX register or flushing the FIFO.
2		Slave transmit IRQ. Set at the end of a transmission. Cleared automatically by writing to the I2C0STX register.
1		Slave transmit FIFO underflow. Set automatically if the slave transmit FIFO is underflowing. Cleared automatically by writing to the I2C0SSTA register.
0		Slave transmit FIFO not full. Set automatically if the slave transmit FIFO is not full. Cleared automatically by writing twice to the I2C0STX register.

Table 130. I2CxSRX Registers

Name	Address	Default Value	Access
I2C0SRX	0xFFFF0808	0x00	R
I2C1SRX	0xFFFF0908	0x00	R

I2CxSRX are receive registers for the slave channel.

Table 131. I2CxSTX Registers

Name	Address	Default Value	Access
I2C0STX	0xFFFF080C	0x00	W
I2C1STX	0xFFFF090C	0x00	W

I2CxSTX are transmit registers for the slave channel.

Table 132. I2CxMRX Registers

Name	Address	Default Value	Access
I2C0MRX	0xFFFF0810	0x00	R
I2C1MRX	0xFFFF0910	0x00	R

I2CxMRX are receive registers for the master channel.

Table 133. I2CxMTX Registers

Name	Address	Default Value	Access
I2C0MTX	0xFFFF0814	0x00	W
I2C1MTX	0xFFFF0914	0x00	W

I2CxMTX are transmit registers for the master channel.

Table 134. I2CxCNT Registers

Name	Address	Default Value	Access
I2C0CNT	0xFFFF0818	0x00	R/W
I2C1CNT	0xFFFF0918	0x00	R/W

I2CxCNT are 3-bit, master receive, data count registers. If a master read transfer sequence is initiated, the I2CxCNT registers denote the number of bytes (−1) to be read from the slave device. By default, this counter is 0, which corresponds to the one byte expected.

Table 135. I2CxADR Registers

Name	Address	Default Value	Access
I2C0ADR	0xFFFF081C	0x00	R/W
I2C1ADR	0xFFFF091C	0x00	R/W

I2CxADR are master address byte registers. The I2CxADR value is the device address that the master wants to communicate with. It automatically transmits at the start of a master transfer sequence if there is no valid data in the I2CxMTX register when the master enable bit is set.

Table 136. I2CxBYTE Registers

Name	Address	Default Value	Access
I2C0BYTE	0xFFFF0824	0x00	R/W
I2C1BYTE	0xFFFF0924	0x00	R/W

I2CxBYTE are broadcast byte registers. Data written to these registers does not go through the TxFIFO. This data is transmitted at the start of a transfer sequence before the address. After the byte is transmitted and acknowledged, the I²C expects another byte written in I2CxBYTE or an address written to the address register.

Table 137. I2CxALT Registers

Name	Address	Default Value	Access
I2C0ALT	0xFFFF0828	0x00	R/W
I2C1ALT	0xFFFF0928	0x00	R/W

I2CxALT are hardware general call ID registers used in slave mode.

Table 138. I2CxCFG Registers

Name	Address	Default Value	Access
I2C0CFG	0xFFFF082C	0x00	R/W
I2C1CFG	0xFFFF092C	0x00	R/W

I2CxCFG are configuration registers.

Table 139. I2C0CFG MMR Bit Descriptions

Bit	Description
31:5	Reserved. These bits should be written by the user as 0.
14	Enable stop interrupt. Set by the user to generate an interrupt upon receiving a stop condition and after receiving a valid start condition and matching address. Cleared by the user to disable the generation of an interrupt upon receiving a stop condition.
13	Reserved.
12	Reserved.
11	Enable stretch SCL (holds SCL low). Set by the user to stretch the SCL line. Cleared by the user to disable stretching of the SCL line.
10	Reserved.
9	Slave Tx FIFO request interrupt enable. Set by the user to disable the slave Tx FIFO request interrupt. Cleared by the user to generate an interrupt request just after the negative edge of the clock for the R/W bit. This allows the user to input data into the slave Tx FIFO if it is empty. At 400 ksps and the core clock running at 41.78 MHz, the user has 45 clock cycles to take appropriate action, taking interrupt latency into account.
8	General call status bit clear. Set by the user to clear the general call status bits. Cleared automatically by hardware after the general call status bits are cleared.
7	Master serial clock enable bit. Set by user to enable generation of the serial clock in master mode. Cleared by user to disable serial clock in master mode.
6	Loopback enable bit. Set by user to internally connect the transition to the reception to test user software. Cleared by user to operate in normal mode.
5	Start backoff disable bit. Set by user in multimaster mode. If losing arbitration, the master immediately tries to retransmit. Cleared by user to enable start backoff. After losing arbitration, the master waits before trying to retransmit.
4	Hardware general call enable. When this bit and Bit 3 are set and have received a general call (Address 0x00) and a data byte, the device checks the contents of I2C0ALT against the receive register. If the contents match, the device has received a hardware general call. This is used if a device needs urgent attention from a master device without knowing which master it needs to turn to. This is a "to whom it may concern" call. The ADuC7019/20/21/22/24/25/26/27/28/29 watch for these addresses. The device that requires attention embeds its own address into the message. All masters listen, and the one that can handle the device contacts its slave and acts appropriately. The LSB of the I2C0ALT register should always be written to 1, as indicated in *The I²C-Bus Specification*, January 2000, from NXP.
3	General call enable bit. This bit is set by the user to enable the slave device to acknowledge (ACK) an I²C general call, Address 0x00 (write). The device then recognizes a data bit. If it receives a 0x06 (reset and write programmable part of slave address by hardware) as the data byte, the I²C interface resets as as indicated in *The I²C-Bus Specification,* January 2000, from NXP. This command can be used to reset an entire I²C system. The general call interrupt status bit sets on any general call. The user must take corrective action by setting up the I²C interface after a reset. If it receives a 0x04 (write programmable part of slave address by hardware) as the data byte, the general call interrupt status bit sets on any general call. The user must take corrective action by reprogramming the device address.
2	Reserved.
1	Master enable bit. Set by user to enable the master I²C channel. Cleared by user to disable the master I²C channel.
0	Slave enable bit. Set by user to enable the slave I²C channel. A slave transfer sequence is monitored for the device address in I2C0ID0, I2C0ID1, I2C0ID2, and I2C0ID3. At 400 kSPs, the core clock should run at 41.78 MHz because the interrupt latency could be up to 45 clock cycles alone. After the I²C read bit, the user has 0.5 of an I²C clock cycle to load the Tx FIFO. AT 400 kSPS, this is 1.26 µs, the interrupt latency.

PROGRAMMABLE LOGIC ARRAY (PLA)

Every ADuC7019/20/21/22/24/25/26/27/28/29 integrates a fully programmable logic array (PLA) that consists of two independent but interconnected PLA blocks. Each block consists of eight PLA elements, giving each part a total of 16 PLA elements.

Each PLA element contains a two-input lookup table that can be configured to generate any logic output function based on two inputs and a flip-flop. This is represented in Figure 76.

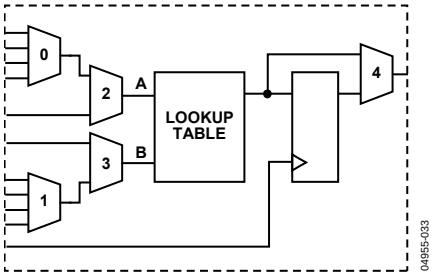


Figure 76. PLA Element

In total, 30 GPIO pins are available on each ADuC7019/20/21/22/24/25/26/27/28/29 for the PLA. These include 16 input pins and 14 output pins, which msut be configured in the GPxCON register as PLA pins before using the PLA. Note that the comparator output is also included as one of the 16 input pins.

The PLA is configured via a set of user MMRs. The output(s) of the PLA can be routed to the internal interrupt system, to the $\overline{\text{CONV}}_{\text{START}}$ signal of the ADC, to an MMR, or to any of the 16 PLA output pins.

The two blocks can be interconnected as follows:

- Output of Element 15 (Block 1) can be fed back to Input 0 of Mux 0 of Element 0 (Block 0).
- Output of Element 7 (Block 0) can be fed back to the Input 0 of Mux 0 of Element 8 (Block 1).

Table 145. Element Input/Output

PLA Block 0			PLA Block 1		
Element	**Input**	**Output**	**Element**	**Input**	**Output**
0	P1.0	P1.7	8	P3.0	P4.0
1	P1.1	P0.4	9	P3.1	P4.1
2	P1.2	P0.5	10	P3.2	P4.2
3	P1.3	P0.6	11	P3.3	P4.3
4	P1.4	P0.7	12	P3.4	P4.4
5	P1.5	P2.0	13	P3.5	P4.5
6	P1.6	P2.1	14	P3.6	P4.6
7	P0.0	P2.2	15	P3.7	P4.7

PLA MMRs Interface

The PLA peripheral interface consists of the 22 MMRs described in this section.

Table 146. PLAELMx Registers

Name	Address	Default Value	Access
PLAELM0	0xFFFF0B00	0x0000	R/W
PLAELM1	0xFFFF0B04	0x0000	R/W
PLAELM2	0xFFFF0B08	0x0000	R/W
PLAELM3	0xFFFF0B0C	0x0000	R/W
PLAELM4	0xFFFF0B10	0x0000	R/W
PLAELM5	0xFFFF0B14	0x0000	R/W
PLAELM6	0xFFFF0B18	0x0000	R/W
PLAELM7	0xFFFF0B1C	0x0000	R/W
PLAELM8	0xFFFF0B20	0x0000	R/W
PLAELM9	0xFFFF0B24	0x0000	R/W
PLAELM10	0xFFFF0B28	0x0000	R/W
PLAELM11	0xFFFF0B2C	0x0000	R/W
PLAELM12	0xFFFF0B30	0x0000	R/W
PLAELM13	0xFFFF0B34	0x0000	R/W
PLAELM14	0xFFFF0B38	0x0000	R/W
PLAELM15	0xFFFF0B3C	0x0000	R/W

PLAELMx are Element 0 to Element 15 control registers. They configure the input and output mux of each element, select the function in the lookup table, and bypass/use the flip-flop. See Table 147 and Table 152.

Table 147. PLAELMx MMR Bit Descriptions

Bit	Value	Description
31:11		Reserved.
10:9		Mux 0 control (see Table 152).
8:7		Mux 1 control (see Table 152).
6		Mux 2 control. Set by user to select the output of Mux 0. Cleared by user to select the bit value from PLADIN.
5		Mux 3 control. Set by user to select the input pin of the particular element. Cleared by user to select the output of Mux 1.
4:1		Lookup table control.
	0000	0.
	0001	NOR.
	0010	B AND NOT A.
	0011	NOT A.
	0100	A AND NOT B.
	0101	NOT B.
	0110	EXOR.
	0111	NAND.
	1000	AND.
	1001	EXNOR.
	1010	B.
	1011	NOT A OR B.
	1100	A.
	1101	A OR NOT B.
	1110	OR.
	1111	1.
0		Mux 4 control. Set by user to bypass the flip-flop. Cleared by user to select the flip-flop (cleared by default).

Timer1 (General-Purpose Timer)

Timer1 is a general-purpose, 32-bit timer (count down or count up) with a programmable prescaler. The source can be the 32 kHz external crystal, the core clock frequency, or an external GPIO (P1.0 or P0.6). The maximum frequency of the clock input is 44 Mhz). This source can be scaled by a factor of 1, 16, 256, or 32,768.

The counter can be formatted as a standard 32-bit value or as hours: minutes: seconds: hundredths.

Timer1 has a capture register (T1CAP) that can be triggered by a selected IRQ source initial assertion. This feature can be used to determine the assertion of an event more accurately than the precision allowed by the RTOS timer when the IRQ is serviced.

Timer1 can be used to start ADC conversions as shown in the block diagram in Figure 78.

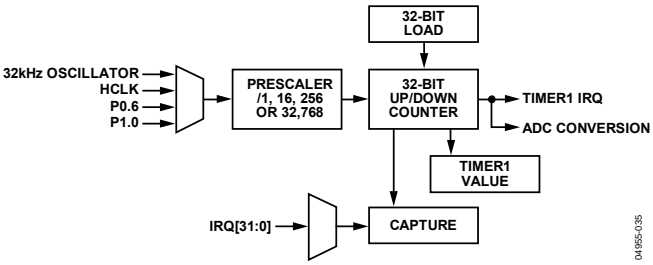


Figure 78. Timer1 Block Diagram

The Timer1 interface consists of five MMRs: T1LD, T1VAL, T1CON, T1CLRI, and T1CAP.

Table 177. T1LD Register

Name	Address	Default Value	Access
T1LD	0xFFFF0320	0x00000000	R/W

T1LD is a 32-bit load register.

Table 178. T1VAL Register

Name	Address	Default Value	Access
T1VAL	0xFFFF0324	0xFFFFFFFF	R

T1VAL is a 32-bit read-only register that represents the current state of the counter.

Table 179. T1CON Register

Name	Address	Default Value	Access
T1CON	0xFFFF0328	0x0000	R/W

T1CON is the configuration MMR described in Table 180.

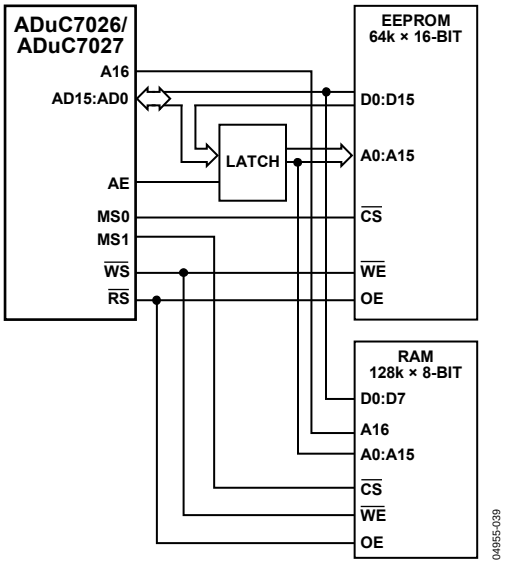


Figure 82. Interfacing to External EEPROM/RAM

Table 195. XMCFG Register

Name	Address	Default Value	Access
XMCFG	0xFFFFF000	0x00	R/W

XMCFG is set to 1 to enable external memory access. This must be set to 1 before any port pins function as external memory access pins. The port pins must also be individually enabled via the GPxCON MMR.

Table 196. XMxCON Registers

Name	Address	Default Value	Access
XM0CON	0xFFFFF010	0x00	R/W
XM1CON	0xFFFFF014	0x00	R/W
XM2CON	0xFFFFF018	0x00	R/W
XM3CON	0xFFFFF01C	0x00	R/W

XMxCON are the control registers for each memory region. They allow the enabling/disabling of a memory region and control the data bus width of the memory region.

Table 197. XMxCON MMR Bit Descriptions

Bit	Description
1	Selects data bus width. Set by user to select a 16-bit data bus. Cleared by user to select an 8-bit data bus.
0	Enables memory region. Set by user to enable the memory region. Cleared by user to disable the memory region.

Table 198. XMxPAR Registers

Name	Address	Default Value	Access
XM0PAR	0xFFFFF020	0x70FF	R/W
XM1PAR	0xFFFFF024	0x70FF	R/W
XM2PAR	0xFFFFF028	0x70FF	R/W
XM3PAR	0xFFFFF02C	0x70FF	R/W

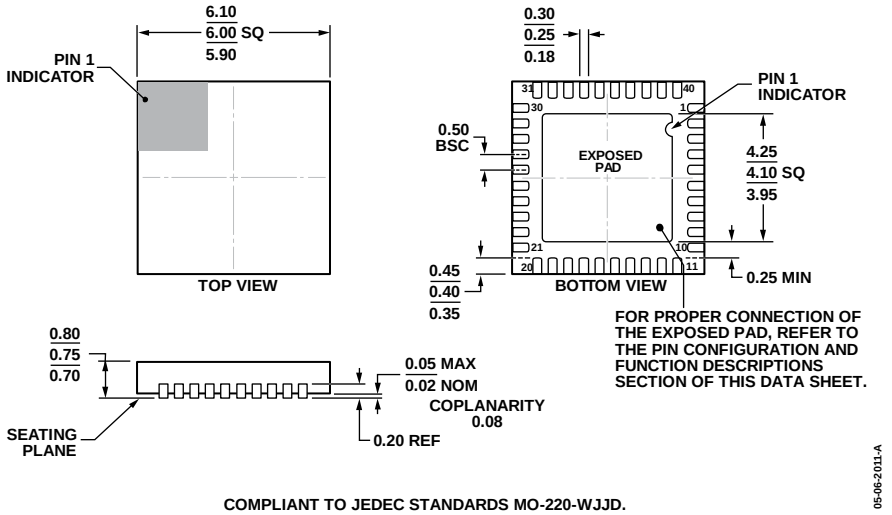
XMxPAR are registers that define the protocol used for accessing the external memory for each memory region.

Table 199. XMxPAR MMR Bit Descriptions

Bit	Description
15	Enable byte write strobe. This bit is used only for two, 8-bit memory devices sharing the same memory region. Set by the user to gate the A0 output with the $\overline{WS}$ output. This allows byte write capability without using $\overline{BHE}$ and $\overline{BLE}$ signals. Cleared by user to use $\overline{BHE}$ and $\overline{BLE}$ signals.
14:12	Number of wait states on the address latch enable STROBE.
11	Reserved.
10	Extra address hold time. Set by user to disable extra hold time. Cleared by user to enable one clock cycle of hold on the address in read and write.
9	Extra bus transition time on read. Set by user to disable extra bus transition time. Cleared by user to enable one extra clock before and after the read strobe ($\overline{RS}$).
8	Extra bus transition time on write. Set by user to disable extra bus transition time. Cleared by user to enable one extra clock before and after the write strobe ($\overline{WS}$).
7:4	Number of write wait states. Select the number of wait states added to the length of the $\overline{WS}$ pulse. 0x0 is 1 clock; 0xF is 16 clock cycles (default value).
3:0	Number of read wait states. Select the number of wait states added to the length of the $\overline{RS}$ pulse. 0x0 is 1 clock; 0xF is 16 clock cycles (default value).

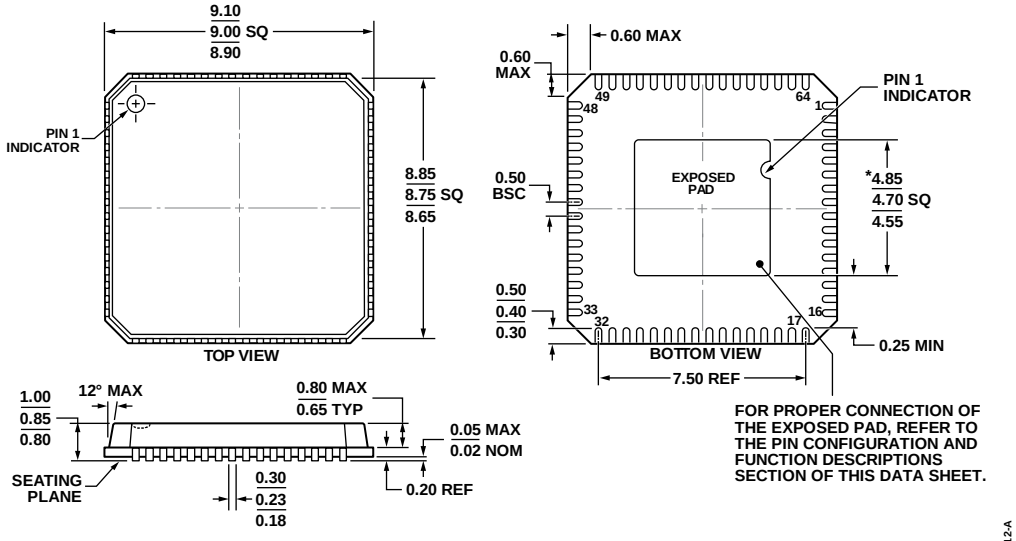
Figure 83, Figure 84, Figure 85, and Figure 86 show the timing for a read cycle, a read cycle with address hold and bus turn cycles, a write cycle with address and write hold cycles, and a write cycle with wait sates, respectively.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WJJD.

Figure 96. 40-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
6 × 6 mm Body, Very Very Thin Quad
(CP-40-9)
Dimensions shown in millimeters



*COMPLIANT TO JEDEC STANDARDS MO-220-VMMD-4
EXCEPT FOR EXPOSED PAD DIMENSION

Figure 97. 64-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
9 mm × 9 mm Body, Very Thin Quad
(CP-64-1)
Dimensions shown in millimeters