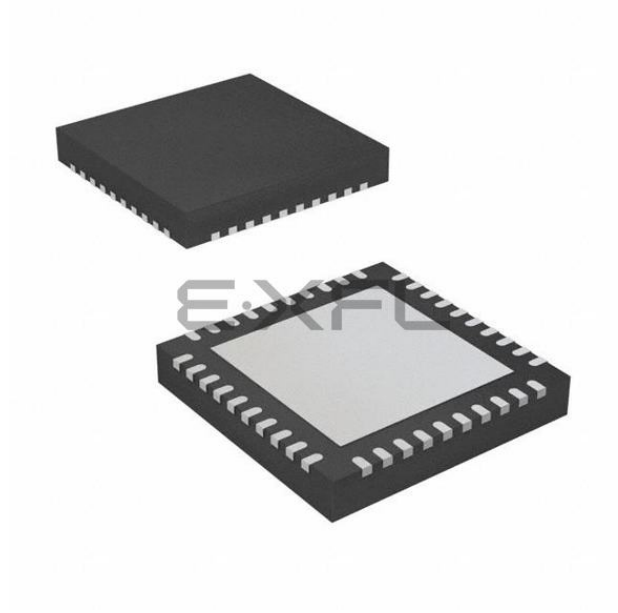

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Speed	44MHz
Connectivity	EBI/EMI, I²C, SPI, UART/USART
Peripherals	PLA, PWM, PSM, Temp Sensor, WDT
Number of I/O	13
Program Memory Size	32KB (16K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 32
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	40-VFQFN Exposed Pad, CSP
Supplier Device Package	40-LFCSP-VQ (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/aduc7021bcpz32

Table 3. External Memory Read Cycle

Parameter	Min	Typ	Max	Unit
CLK[1]	1/MD clock	ns typ × (POWCON[2:0] + 1)		
$t_{MS\_AFTER\_CLKH}$	4		8	ns
$t_{ADDR\_AFTER\_CLKH}$	4		16	ns
$t_{AE\_H\_AFTER\_MS}$		½ CLK		
t_{AE}		(XMxPAR[14:12] + 1) × CLK		
$t_{HOLD\_ADDR\_AFTER\_AE\_L}$		½ CLK + (! XMxPAR[10]) × CLK		
$t_{RD\_L\_AFTER\_AE\_L}$		½ CLK + (! XMxPAR[10]+ ! XMxPAR[9]) × CLK		
$t_{RD\_H\_AFTER\_CLKH}$	0		4	
t_{RD}		(XMxPAR[3:0] + 1) × CLK		
$t_{DATA\_BEFORE\_RD\_H}$	16			ns
$t_{DATA\_AFTER\_RD\_H}$	8	+ (! XMxPAR[9]) × CLK		
$t_{RELEASE\_MS\_AFTER\_RD\_H}$		1 × CLK		

[1] See Table 78.

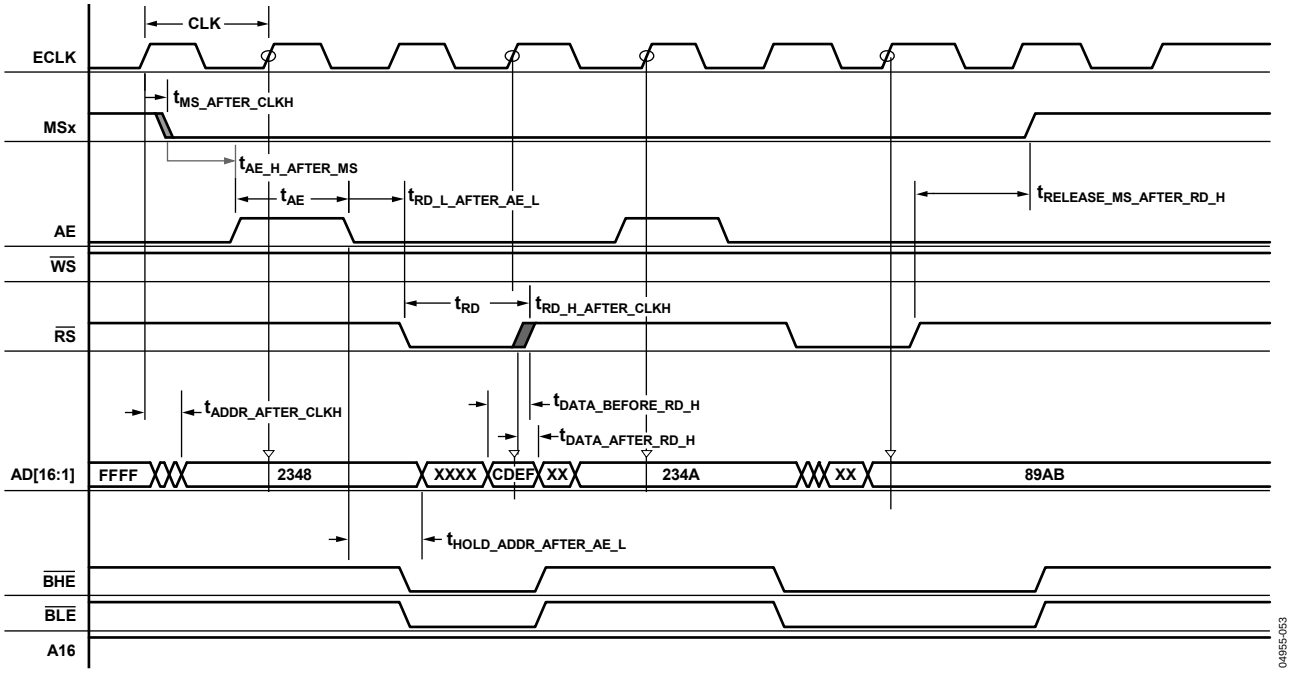


Figure 13. External Memory Read Cycle (See Table 78)

Table 6. SPI Master Mode Timing (Phase Mode = 1)

Parameter	Description	Min	Typ	Max	Unit
t_{SL}	SCLK low pulse width[1]		(SPIDIV + 1) × t_{HCLK}		ns
t_{SH}	SCLK high pulse width[1]		(SPIDIV + 1) × t_{HCLK}		ns
t_{DAV}	Data output valid after SCLK edge			25	ns
t_{DSU}	Data input setup time before SCLK edge[2]	1 × t_{UCLK}			ns
t_{DHD}	Data input hold time after SCLK edge[2]	2 × t_{UCLK}			ns
t_{DF}	Data output fall time		5	12.5	ns
t_{DR}	Data output rise time		5	12.5	ns
t_{SR}	SCLK rise time		5	12.5	ns
t_{SF}	SCLK fall time		5	12.5	ns

[1] t_{HCLK} depends on the clock divider or CD bits in the POWCONMMR. $t_{HCLK} = t_{UCLK}/2^{CD}$; see Figure 67.
[2] t_{UCLK} = 23.9 ns. It corresponds to the 41.78 MHz internal clock from the PLL before the clock divider; see Figure 67.

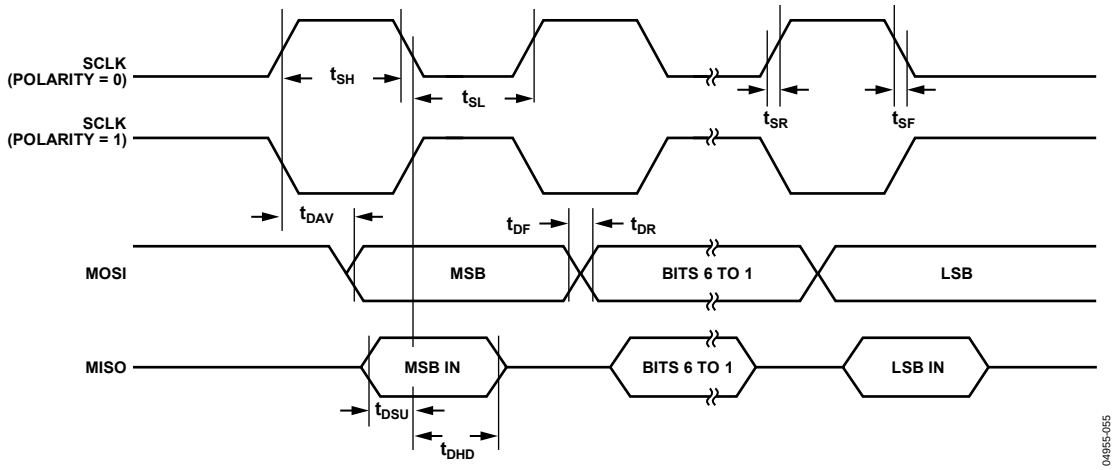
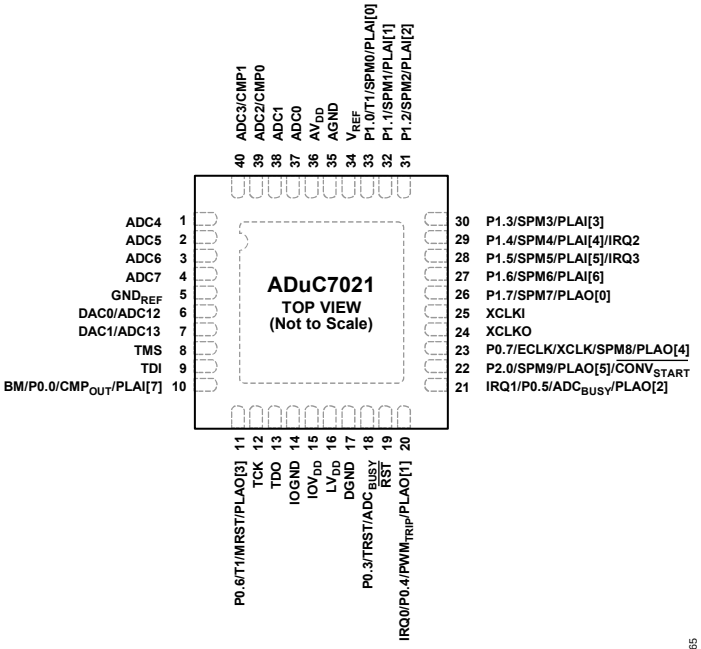


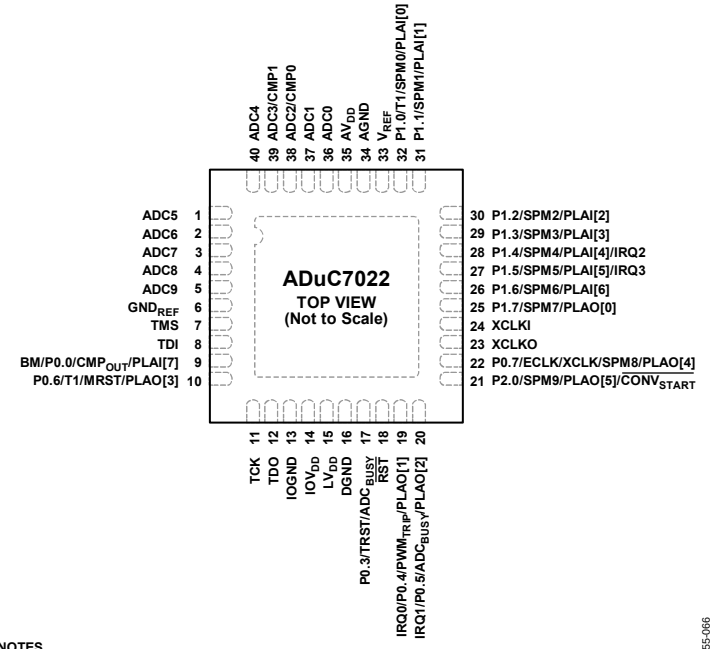
Figure 15. SPI Master Mode Timing (Phase Mode = 1)



NOTES
1. THE EXPOSED PAD MUST BE SOLDERED FOR MECHANICAL PURPOSES AND LEFT UNCONNECTED.

04955-065

Figure 21. 40-Lead LFCSP_WQ Pin Configuration (ADuC7021)



NOTES
1. THE EXPOSED PAD MUST BE SOLDERED FOR MECHANICAL PURPOSES AND LEFT UNCONNECTED.

04955-066

Figure 22. 40-Lead LFCSP_WQ Pin Configuration (ADuC7022)

Table 12. Pin Function Descriptions (ADuC7024/ADuC7025 64-Lead LFCSP_VQ and 64-Lead LQFP)

Pin No.	Mnemonic	Description
1	ADC4	Single-Ended or Differential Analog Input 4.
2	ADC5	Single-Ended or Differential Analog Input 5.
3	ADC6	Single-Ended or Differential Analog Input 6.
4	ADC7	Single-Ended or Differential Analog Input 7.
5	ADC8	Single-Ended or Differential Analog Input 8.
6	ADC9	Single-Ended or Differential Analog Input 9.
7	GND_{REF}	Ground Voltage Reference for the ADC. For optimal performance, the analog power supply should be separated from IOGND and DGND.
8	ADCNEG	Bias Point or Negative Analog Input of the ADC in Pseudo Differential Mode. Must be connected to the ground of the signal to convert. This bias point must be between 0 V and 1 V.
9	DAC0/ADC12	DAC0 Voltage Output/Single-Ended or Differential Analog Input 12. DAC outputs are not present on the ADuC7025.
10	DAC1/ADC13	DAC1 Voltage Output/Single-Ended or Differential Analog Input 13. DAC outputs are not present on the ADuC7025.
11	TMS	JTAG Test Port Input, Test Mode Select. Debug and download access.
12	TDI	JTAG Test Port Input, Test Data In. Debug and download access
13	P4.6/PLAO[14]	General-Purpose Input and Output Port 4.6/Programmable Logic Array Output Element 14.
14	P4.7/PLAO[15]	General-Purpose Input and Output Port 4.7/Programmable Logic Array Output Element 15.
15	BM/P0.0/CMP_{OUT}/PLAI[7]	Multifunction I/O Pin. Boot mode. The ADuC7024/ADuC7025 enter download mode if BM is low at reset and execute code if BM is pulled high at reset through a 1 kΩ resistor/General-Purpose Input and Output Port 0.0/Voltage Comparator Output/Programmable Logic Array Input Element 7.
16	P0.6/T1/MRST/PLAO[3]	Multifunction Pin, Driven Low After Reset. General-Purpose Output Port 0.6/Timer1 Input/Power-On Reset Output/Programmable Logic Array Output Element 3.
17	TCK	JTAG Test Port Input, Test Clock. Debug and download access.
18	TDO	JTAG Test Port Output, Test Data Out. Debug and download access.
19	IOGND	Ground for GPIO (see Table 78). Typically connected to DGND.
20	IOV_{DD}	3.3 V Supply for GPIO (see Table 78) and Input of the On-Chip Voltage Regulator.
21	LV_{DD}	2.6 V Output of the On-Chip Voltage Regulator. This output must be connected to a 0.47 µF capacitor to DGND only.
22	DGND	Ground for Core Logic.
23	P3.0/$PWM0_H$/PLAI[8]	General-Purpose Input and Output Port 3.0/PWM Phase 0 High-Side Output/Programmable Logic Array Input Element 8.
24	P3.1/$PWM0_L$/PLAI[9]	General-Purpose Input and Output Port 3.1/PWM Phase 0 Low-Side Output/Programmable Logic Array Input Element 9.
25	P3.2/$PWM1_H$/PLAI[10]	General-Purpose Input and Output Port 3.2/PWM Phase 1 High-Side Output/Programmable Logic Array Input Element 10.
26	P3.3/$PWM1_L$/PLAI[11]	General-Purpose Input and Output Port 3.3/PWM Phase 1 Low-Side Output/Programmable Logic Array Input Element 11.
27	P0.3/TRST/ADC_{BUSY}	General-Purpose Input and Output Port 0.3/JTAG Test Port Input, Test Reset/ADC_{BUSY} Signal Output.
28	$\overline{RST}$	Reset Input, Active Low.
29	P3.4/$PWM2_H$/PLAI[12]	General-Purpose Input and Output Port 3.4/PWM Phase 2 High-Side Output/Programmable Logic Array Input 12.
30	P3.5/$PWM2_L$/PLAI[13]	General-Purpose Input and Output Port 3.5/PWM Phase 2 Low-Side Output/Programmable Logic Array Input Element 13.
31	IRQ0/P0.4/PWM_{TRIP}/PLAO[1]	Multifunction I/O Pin. External Interrupt Request 0, Active High/General-Purpose Input and Output Port 0.4/PWM Trip External Input/Programmable Logic Array Output Element 1.
32	IRQ1/P0.5/ADC_{BUSY}/PLAO[2]	Multifunction I/O Pin. External Interrupt Request 1, Active High/General-Purpose Input and Output Port 0.5/ADC_{BUSY} Signal Output/Programmable Logic Array Output Element 2.
33	P2.0/SPM9/PLAO[5]/$\overline{CONV_{START}}$	Serial Port Multiplexed. General-Purpose Input and Output Port 2.0/UART/Programmable Logic Array Output Element 5/Start Conversion Input Signal for ADC.
34	P0.7/ECLK/XCLK/SPM8/PLAO[4]	Serial Port Multiplexed. General-Purpose Input and Output Port 0.7/Output for External Clock Signal/Input to the Internal Clock Generator Circuits/UART/Programmable Logic Array Output Element 4.
35	XCLKO	Output from the Crystal Oscillator Inverter.
36	XCLKI	Input to the Crystal Oscillator Inverter and Input to the Internal Clock Generator Circuits.

Pin No.	Mnemonic	Description
46	P3.6/AD6/PWM_{TRIP}/PLAI[14]	General-Purpose Input and Output Port 3.6/External Memory Interface/PWM Safety Cutoff/ Programmable Logic Array Input Element 14.
47	P3.7/AD7/PWM_{SYNC}/PLAI[15]	General-Purpose Input and Output Port 3.7/External Memory Interface/PWM Synchronization/ Programmable Logic Array Input Element 15.
48	P2.7/$PWM1_L$/MS3	General-Purpose Input and Output Port 2.7/PWM Phase 1 Low-Side Output/External Memory Select 3.
49	P2.1/$\overline{WS}$/$PWM0_H$/PLAO[6]	General-Purpose Input and Output Port 2.1/External Memory Write Strobe/PWM Phase 0 High-Side Output/Programmable Logic Array Output Element 6.
50	P2.2/$\overline{RS}$/$PWM0_L$/PLAO[7]	General-Purpose Input and Output Port 2.2/External Memory Read Strobe/PWM Phase 0 Low-Side Output/Programmable Logic Array Output Element 7.
51	P1.7/SPM7/PLAO[0]	Serial Port Multiplexed. General-Purpose Input and Output Port 1.7/UART, SPI/Programmable Logic Array Output Element 0.
52	P1.6/SPM6/PLAI[6]	Serial Port Multiplexed. General-Purpose Input and Output Port 1.6/UART, SPI/Programmable Logic Array Input Element 6.
53	IOGND	Ground for GPIO (see Table 78). Typically connected to DGND.
54	IOV_{DD}	3.3 V Supply for GPIO (see Table 78) and Input of the On-Chip Voltage Regulator.
55	P4.0/AD8/PLAO[8]	General-Purpose Input and Output Port 4.0/External Memory Interface/Programmable Logic Array Output Element 8.
56	P4.1/AD9/PLAO[9]	General-Purpose Input and Output Port 4.1/External Memory Interface/Programmable Logic Array Output Element 9.
57	P1.5/SPM5/PLAI[5]/IRQ3	Serial Port Multiplexed. General-Purpose Input and Output Port 1.5/UART, SPI/Programmable Logic Array Input Element 5/External Interrupt Request 3, Active High.
58	P1.4/SPM4/PLAI[4]/IRQ2	Serial Port Multiplexed. General-Purpose Input and Output Port 1.4/UART, SPI/Programmable Logic Array Input Element 4/External Interrupt Request 2, Active High.
59	P1.3/SPM3/PLAI[3]	Serial Port Multiplexed. General-Purpose Input and Output Port 1.3/UART, I2C1/Programmable Logic Array Input Element 3.
60	P1.2/SPM2/PLAI[2]	Serial Port Multiplexed. General-Purpose Input and Output Port 1.2/UART, I2C1/Programmable Logic Array Input Element 2.
61	P1.1/SPM1/PLAI[1]	Serial Port Multiplexed. General-Purpose Input and Output Port 1.1/UART, I2C0/Programmable Logic Array Input Element 1.
62	P1.0/T1/SPM0/PLAI[0]	Serial Port Multiplexed. General-Purpose Input and Output Port 1.0/Timer1 Input/UART, I2C0/ Programmable Logic Array Input Element 0.
63	P4.2/AD10/PLAO[10]	General-Purpose Input and Output Port 4.2/External Memory Interface/Programmable Logic Array Output Element 10.
64	P4.3/AD11/PLAO[11]	General-Purpose Input and Output Port 4.3/External Memory Interface/Programmable Logic Array Output Element 11.
65	P4.4/AD12/PLAO[12]	General-Purpose Input and Output Port 4.4/External Memory Interface/Programmable Logic Array Output Element 12.
66	P4.5/AD13/PLAO[13]	General-Purpose Input and Output Port 4.5/External Memory Interface/Programmable Logic Array Output Element 13.
67	REFGND	Ground for the Reference. Typically connected to AGND.
68	V_{REF}	2.5 V Internal Voltage Reference. Must be connected to a 0.47 µF capacitor when using the internal reference.
69	DAC_{REF}	External Voltage Reference for the DACs. Range: DACGND to $DACV_{DD}$.
70	DACGND	Ground for the DAC. Typically connected to AGND.
71, 72	AGND	Analog Ground. Ground reference point for the analog circuitry.
73, 74	AV_{DD}	3.3 V Analog Power.
75	$DACV_{DD}$	3.3 V Power Supply for the DACs. Must be connected to AV_{DD}.
76	ADC11	Single-Ended or Differential Analog Input 11.
77	ADC0	Single-Ended or Differential Analog Input 0.
78	ADC1	Single-Ended or Differential Analog Input 1.
79	ADC2/CMP0	Single-Ended or Differential Analog Input 2/Comparator Positive Input.
80	ADC3/CMP1	Single-Ended or Differential Analog Input 3/Comparator Negative Input.

Pin No.	Mnemonic	Description
E1	TMS	JTAG Test Port Input, Test Mode Select. Debug and download access.
E2	BM/P0.0/CMP_{OUT}/PLAI[7]	Multifunction I/O Pin. Boot mode. The ADuC7029 enters UART download mode if BM is low at reset and executes code if BM is pulled high at reset through a 1 kΩ resistor/General-Purpose Input and Output Port 0.0/Voltage Comparator Output/Programmable Logic Array Input Element 7.
E3	DAC2/ADC14	DAC2 Voltage Output/ADC Input 14.
E4	IOV_{DD}	3.3 V Supply for GPIO (see Table 78) and Input of the On-Chip Voltage Regulator.
E5	P3.2/$PWM1_H$/PLAI[10]	General-Purpose Input and Output Port 3.2/PWM Phase 1 High-Side Output/Programmable Logic Array Input Element 10.
E6	P3.5/$PWM2_L$/PLAI[13]	General-Purpose Input and Output Port 3.5/PWM Phase 2 Low-Side Output/Programmable Logic Array Input Element 13.
E7	P0.7/ECLK/XCLK/SPM8/PLAO[4]	Serial Port Multiplexed. General-Purpose Input and Output Port 0.7/Output for External Clock Signal/Input to the Internal Clock Generator Circuits/UART/Programmable Logic Array Output Element 4.
F1	TDI	JTAG Test Port Input, Test Data In. Debug and download access.
F2	P0.6/T1/MRST/PLAO[3]	Multifunction Pin, Driven Low After Reset. General-Purpose Output Port 0.6/Timer1 Input/Power-On Reset Output/Programmable Logic Array Output Element 3.
F3	IOGND	Ground for GPIO (see Table 78). Typically connected to DGND.
F4	P3.1/$PWM0_L$/PLAI[9]	General-Purpose Input and Output Port 3.1/PWM Phase 0 Low-Side Output/Programmable Logic Array Input Element 9.
F5	P3.0/$PWM0_H$/PLAI[8]	General-Purpose Input and Output Port 3.0/PWM Phase 0 High-Side Output/Programmable Logic Array Input Element 8.
F6	$\overline{RST}$	Reset Input, Active Low.
F7	P2.0/SPM9/PLAO[5]/$\overline{CONV_{START}}$	Serial Port Multiplexed. General-Purpose Input and Output Port 2.0/UART/Programmable Logic Array Output Element 5/Start Conversion Input Signal for ADC.
G1	TCK	JTAG Test Port Input, Test Clock. Debug and download access.
G2	TDO	JTAG Test Port Output, Test Data Out. Debug and download access.
G3	LV_{DD}	2.6 V Output of the On-Chip Voltage Regulator. This output must be connected to a 0.47 µF capacitor to DGND only.
G4	DGND	Ground for Core Logic.
G5	P0.3/TRST/ADC_{BUSY}	General-Purpose Input and Output Port 0.3/JTAG Test Port Input, Test Reset/ADC_{BUSY} Signal Output.
G6	IRQ0/P0.4/PWM_{TRIP}/PLAO[1]	Multifunction I/O Pin. External Interrupt Request 0, Active High/General-Purpose Input and Output Port 0.4/PWM Trip External Input/Programmable Logic Array Output Element 1.
G7	IRQ1/P0.5/ADC_{BUSY}/PLAO[2]	Multifunction I/O Pin. External Interrupt Request 1, Active High/General-Purpose Input and Output Port 0.5/ADC_{BUSY} Signal Output/Programmable Logic Array Output Element 2.

Address	Name	Byte	Access Type	Default Value	Page
PLA Base Address = 0xFFFF0B00					
0x0B00	PLAELM0	2	R/W	0x0000	80
0x0B04	PLAELM1	2	R/W	0x0000	80
0x0B08	PLAELM2	2	R/W	0x0000	80
0x0B0C	PLAELM3	2	R/W	0x0000	80
0x0B10	PLAELM4	2	R/W	0x0000	80
0x0B14	PLAELM5	2	R/W	0x0000	80
0x0B18	PLAELM6	2	R/W	0x0000	80
0x0B1C	PLAELM7	2	R/W	0x0000	80
0x0B20	PLAELM8	2	R/W	0x0000	80
0x0B24	PLAELM9	2	R/W	0x0000	80
0x0B28	PLAELM10	2	R/W	0x0000	80
0x0B2C	PLAELM11	2	R/W	0x0000	80
0x0B30	PLAELM12	2	R/W	0x0000	80
0x0B34	PLAELM13	2	R/W	0x0000	80
0x0B38	PLAELM14	2	R/W	0x0000	80
0x0B3C	PLAELM15	2	R/W	0x0000	80
0x0B40	PLACLK	1	R/W	0x00	81
0x0B44	PLAIRQ	4	R/W	0x00000000	81
0x0B48	PLAADC	4	R/W	0x00000000	82
0x0B4C	PLADIN	4	R/W	0x00000000	82
0x0B50	PLADOUT	4	R	0x00000000	82
0x0B54	PLALCK	1	W	0x00	82
External Memory Base Address = 0xFFFFF000					
0xF000	XMCFG	1	R/W	0x00	90
0xF010	XM0CON	1	R/W	0x00	90
0xF014	XM1CON	1	R/W	0x00	90
0xF018	XM2CON	1	R/W	0x00	90
0xF01C	XM3CON	1	R/W	0x00	90
0xF020	XM0PAR	2	R/W	0x70FF	90
0xF024	XM1PAR	2	R/W	0x70FF	90
0xF028	XM2PAR	2	R/W	0x70FF	90
0xF02C	XM3PAR	2	R/W	0x70FF	90

Address	Name	Byte	Access Type	Default Value	Page
GPIO Base Address = 0xFFFFF400					
0xF400	GP0CON	4	R/W	0x00000000	68
0xF404	GP1CON	4	R/W	0x00000000	68
0xF408	GP2CON	4	R/W	0x00000000	68
0xF40C	GP3CON	4	R/W	0x00000000	68
0xF410	GP4CON	4	R/W	0x00000000	68
0xF420	GP0DAT	4	R/W	0x000000XX[1]	70
0xF424	GP0SET	4	W	0x000000XX[1]	70
0xF428	GP0CLR	4	W	0x000000XX[1]	70
0xF42C	GP0PAR	4	R/W	0x20000000	68
0xF430	GP1DAT	4	R/W	0x000000XX[1]	69
0xF434	GP1SET	4	W	0x000000XX[1]	70
0xF438	GP1CLR	4	W	0x000000XX[1]	70
0xF43C	GP1PAR	4	R/W	0x00000000	68
0xF440	GP2DAT	4	R/W	0x000000XX[1]	69
0xF444	GP2SET	4	W	0x000000XX[1]	70
0xF448	GP2CLR	4	W	0x000000XX[1]	70
0xF450	GP3DAT	4	R/W	0x000000XX[1]	69
0xF454	GP3SET	4	W	0x000000XX[1]	70
0xF458	GP3CLR	4	W	0x000000XX[1]	70
0xF460	GP4DAT	4	R/W	0x000000XX[1]	69
0xF464	GP4SET	4	W	0x000000XX[1]	70
0xF468	GP4CLR	4	W	0x000000XX[1]	70

[1] X = 0, 1, 2, or 3.

Flash/EE Base Address = 0xFFFFF800					
0xF800	FEESTA	1	R	0x20	52
0xF804	FEEMOD	2	R/W	0x0000	52
0xF808	FEECON	1	R/W	0x07	53
0xF80C	FEEDAT	2	R/W	0xXXXX[1]	53
0xF810	FEEADR	2	R/W	0x0000	53
0xF818	FEESIGN	3	R	0xFFFFFF	53
0xF81C	FEEPRO	4	R/W	0x00000000	53
0xF820	FEEHIDE	4	R/W	0xFFFFFFFF	53

[1] X = 0, 1, 2, or 3.

PWM Base Address = 0xFFFFFC00					
0xFC00	PWMCON	2	R/W	0x0000	66
0xFC04	PWMSTA	2	R/W	0x0000	66
0xFC08	PWMDAT0	2	R/W	0x0000	67
0xFC0C	PWMDAT1	2	R/W	0x0000	67
0xFC10	PWMCFG	2	R/W	0x0000	67
0xFC14	PWMCH0	2	R/W	0x0000	67
0xFC18	PWMCH1	2	R/W	0x0000	67
0xFC1C	PWMCH2	2	R/W	0x0000	67
0xFC20	PWMEN	2	R/W	0x0000	67
0xFC24	PWMDAT2	2	R/W	0x0000	67

TYPICAL OPERATION

Once configured via the ADC control and channel selection registers, the ADC converts the analog input and provides a 12-bit result in the ADC data register.

The top four bits are the sign bits. The 12-bit result is placed from Bit 16 to Bit 27, as shown in Figure 51. Again, it should be noted that, in fully differential mode, the result is represented in twos complement format. In pseudo differential and single-ended modes, the result is represented in straight binary format.

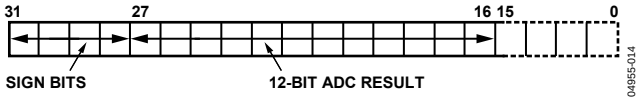


Figure 51. ADC Result Format

The same format is used in DACxDAT, simplifying the software.

Current Consumption

The ADC in standby mode, that is, powered up but not converting, typically consumes 640 μA. The internal reference adds 140 μA. During conversion, the extra current is 0.3 μA multiplied by the sampling frequency (in kilohertz (kHz)). Figure 43 shows the current consumption vs. the sampling frequency of the ADC.

Timing

Figure 52 gives details of the ADC timing. Users control the ADC clock speed and the number of acquisition clocks in the ADCCON MMR. By default, the acquisition time is eight clocks and the clock divider is 2. The number of extra clocks (such as bit trial or write) is set to 19, which gives a sampling rate of 774 kSPS. For conversion on the temperature sensor, the ADC acquisition time is automatically set to 16 clocks, and the ADC clock divider is set to 32. When using multiple channels, including the temperature sensor, the timing settings revert to the user-defined settings after reading the temperature sensor channel.

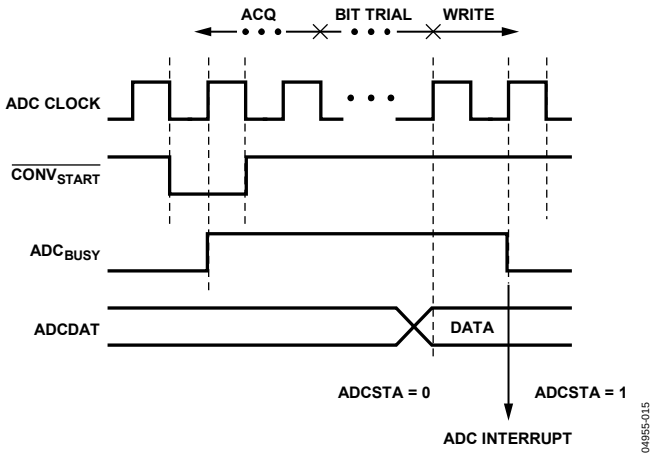


Figure 52. ADC Timing

ADuC7019

The ADuC7019 is identical to the ADuC7020 except for one buffered ADC channel, ADC3, and it has only three DACs. The output buffer of the fourth DAC is internally connected to the ADC3 channel as shown in Figure 53.

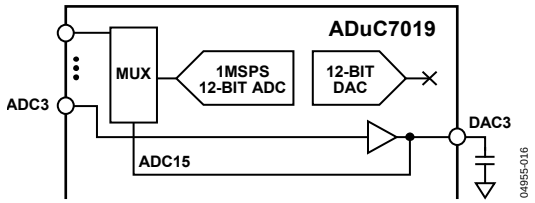


Figure 53. ADC3 Buffered Input

Note that the DAC3 output pin must be connected to a 10 nF capacitor to AGND. This channel should be used to measure dc voltages only. ADC calibration may be necessary on this channel.

MMRS INTERFACE

The ADC is controlled and configured via the eight MMRs described in this section.

Table 17. ADCCON Register

Name	Address	Default Value	Access
ADCCON	0xFFFF0500	0x0600	R/W

ADCCON is an ADC control register that allows the programmer to enable the ADC peripheral, select the mode of operation of the ADC (in single-ended mode, pseudo differential mode, or fully differential mode), and select the conversion type. This MMR is described in Table 18.

Table 18. ADCCON MMR Bit Designations

Bit	Value	Description
15:13		Reserved.
12:10		ADC clock speed.
	000	fADC/1. This divider is provided to obtain 1 MSPS ADC with an external clock <41.78 MHz.
	001	fADC/2 (default value).
	010	fADC/4.
	011	fADC/8.
	100	fADC/16.
	101	fADC/32.
9:8		ADC acquisition time.
	00	Two clocks.
	01	Four clocks.
	10	Eight clocks (default value).
	11	16 clocks.
7		Enable start conversion. Set by the user to start any type of conversion command. Cleared by the user to disable a start conversion (clearing this bit does not stop the ADC when continuously converting).
6		Reserved.
5		ADC power control. Set by the user to place the ADC in normal mode (the ADC must be powered up for at least 5 µs before it converts correctly). Cleared by the user to place the ADC in power-down mode.
4:3		Conversion mode.
	00	Single-ended mode.
	01	Differential mode.
	10	Pseudo differential mode.
	11	Reserved.
2:0		Conversion type.
	000	Enable $\overline{CONV}_{START}$ pin as a conversion input.
	001	Enable Timer1 as a conversion input.
	010	Enable Timer0 as a conversion input.
	011	Single software conversion. Sets to 000 after conversion (note that Bit 7 of ADCCON MMR should be cleared after starting a single software conversion to avoid further conversions triggered by the $\overline{CONV}_{START}$ pin).
	100	Continuous software conversion.
	101	PLA conversion.
	Other	Reserved.

Table 19. ADCCP Register

Name	Address	Default Value	Access
ADCCP	0xFFFF0504	0x00	R/W

ADCCP is an ADC positive channel selection register. This MMR is described in Table 20.

Table 20. ADCCP[1] MMR Bit Designation

Bit	Value	Description
7:5		Reserved.
4:0		Positive channel selection bits.
	00000	ADC0.
	00001	ADC1.
	00010	ADC2.
	00011	ADC3.
	00100	ADC4.
	00101	ADC5.
	00110	ADC6.
	00111	ADC7.
	01000	ADC8.
	01001	ADC9.
	01010	ADC10.
	01011	ADC11.
	01100	DAC0/ADC12.
	01101	DAC1/ADC13.
	01110	DAC2/ADC14.
	01111	DAC3/ADC15.
	10000	Temperature sensor.
	10001	AGND (self-diagnostic feature).
	10010	Internal reference (self-diagnostic feature).
	10011	$AV_{DD}/2$.
	Others	Reserved.

[1] ADC and DAC channel availability depends on the part model. See Ordering Guide for details.

Table 21. ADCCN Register

Name	Address	Default Value	Access
ADCCN	0xFFFF0508	0x01	R/W

ADCCN is an ADC negative channel selection register. This MMR is described in Table 22.

Table 22. ADCCN MMR Bit Designation

Bit	Value	Description
7:5		Reserved.
4:0		Negative channel selection bits.
	00000	ADC0.
	00001	ADC1.
	00010	ADC2.
	00011	ADC3.
	00100	ADC4.
	00101	ADC5.
	00110	ADC6.
	00111	ADC7.
	01000	ADC8.
	01001	ADC9.
	01010	ADC10.
	01011	ADC11.
	01100	DAC0/ADC12.
	01101	DAC1/ADC13.
	01110	DAC2/ADC14.
	01111	DAC3/ADC15.
	10000	Internal reference (self-diagnostic feature).
	Others	Reserved.

Table 23. ADCSTA Register

Name	Address	Default Value	Access
ADCSTA	0xFFFF050C	0x00	R

ADCSTA is an ADC status register that indicates when an ADC conversion result is ready. The ADCSTA register contains only one bit, ADCReady (Bit 0), representing the status of the ADC. This bit is set at the end of an ADC conversion, generating an ADC interrupt. It is cleared automatically by reading the ADCDAT MMR. When the ADC is performing a conversion, the status of the ADC can be read externally via the ADC_{BUSY} pin. This pin is high during a conversion. When the conversion is finished, ADC_{BUSY} goes back low. This information can be available on P0.5 (see the General-Purpose Input/Output section) if enabled in the ADCCON register.

Table 24. ADCDAT Register

Name	Address	Default Value	Access
ADCDAT	0xFFFF0510	0x00000000	R

ADCDAT is an ADC data result register. It holds the 12-bit ADC result as shown in Figure 51.

Table 25. ADCRST Register

Name	Address	Default Value	Access
ADCRST	0xFFFF0514	0x00	R/W

ADCRST resets the digital interface of the ADC. Writing any value to this register resets all the ADC registers to their default values.

Table 26. ADCGN Register

Name	Address	Default Value	Access
ADCGN	0xFFFF0530	0x0200	R/W

ADCGN is a 10-bit gain calibration register.

Table 27. ADCOF Register

Name	Address	Default Value	Access
ADCOF	0xFFFF0534	0x0200	R/W

ADCOF is a 10-bit offset calibration register.

CONVERTER OPERATION

The ADC incorporates a successive approximation (SAR) architecture involving a charge-sampled input stage. This architecture can operate in three modes: differential, pseudo differential, and single-ended.

Differential Mode

The ADuC7019/20/21/22/24/25/26/27/28/29 each contain a successive approximation ADC based on two capacitive DACs. Figure 54 and Figure 55 show simplified schematics of the ADC in acquisition and conversion phase, respectively. The ADC comprises control logic, a SAR, and two capacitive DACs. In Figure 54 (the acquisition phase), SW3 is closed and SW1 and SW2 are in Position A. The comparator is held in a balanced condition, and the sampling capacitor arrays acquire the differential signal on the input.

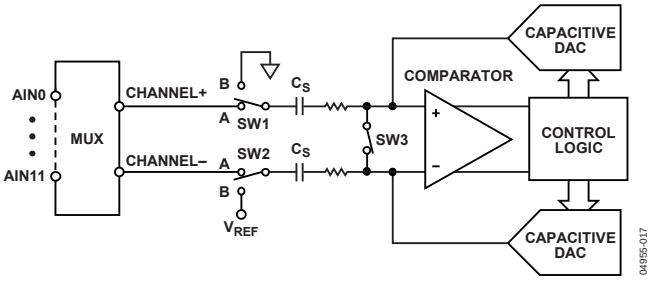


Figure 54. ADC Acquisition Phase

When the ADC starts a conversion, as shown in Figure 55, SW3 opens, and then SW1 and SW2 move to Position B. This causes the comparator to become unbalanced. Both inputs are disconnected once the conversion begins. The control logic and the charge redistribution DACs are used to add and subtract fixed amounts of charge from the sampling capacitor arrays to bring the comparator back into a balanced condition. When the comparator is rebalanced, the conversion is complete. The control logic generates the ADC output code. The output impedances of the sources driving the V_{IN+} and V_{IN-} input voltage pins must be matched; otherwise, the two inputs have different settling times, resulting in errors.

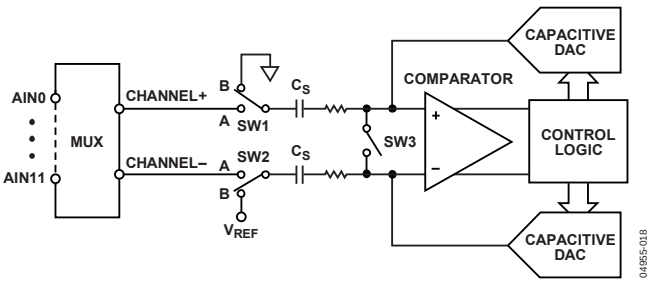


Figure 55. ADC Conversion Phase

EXECUTION TIME FROM SRAM AND FLASH/EE

Execution from SRAM

Fetching instructions from SRAM takes one clock cycle; the access time of the SRAM is 2 ns, and a clock cycle is 22 ns minimum. However, if the instruction involves reading or writing data to memory, one extra cycle must be added if the data is in SRAM (or three cycles if the data is in Flash/EE): one cycle to execute the instruction, and two cycles to get the 32-bit data from Flash/EE. A control flow instruction (a branch instruction, for example) takes one cycle to fetch but also takes two cycles to fill the pipeline with the new instructions.

Execution from Flash/EE

Because the Flash/EE width is 16 bits and access time for 16-bit words is 22 ns, execution from Flash/EE cannot be done in one cycle (as can be done from SRAM when the CD Bit = 0). Also, some dead times are needed before accessing data for any value of the CD bit.

In ARM mode, where instructions are 32 bits, two cycles are needed to fetch any instruction when CD = 0. In thumb mode, where instructions are 16 bits, one cycle is needed to fetch any instruction.

Timing is identical in both modes when executing instructions that involve using the Flash/EE for data memory. If the instruction to be executed is a control flow instruction, an extra cycle is needed to decode the new address of the program counter, and then four cycles are needed to fill the pipeline. A data-processing instruction involving only the core register does not require any extra clock cycles. However, if it involves data in Flash/EE, an extra clock cycle is needed to decode the address of the data, and two cycles are needed to get the 32-bit data from Flash/EE. An extra cycle must also be added before fetching another instruction. Data transfer instructions are more complex and are summarized in Table 43.

Table 43. Execution Cycles in ARM/Thumb Mode

Instructions	Fetch Cycles	Dead Time	Data Access	Dead Time
LD[1]	2/1	1	2	1
LDH	2/1	1	1	1
LDM/PUSH	2/1	N[2]	2 × N[2]	N[1]
STR[1]	2/1	1	2 × 20 ns	1
STRH	2/1	1	20 ns	1
STRM/POP	2/1	N[1]	2 × N × 20 ns[1]	N[1]

[1] The SWAP instruction combines an LD and STR instruction with only one fetch, giving a total of eight cycles + 40 ns.
[2] N is the amount of data to load or store in the multiple load/store instruction (1 < N ≤ 16).

RESET AND REMAP

The ARM exception vectors are all situated at the bottom of the memory array, from Address 0x00000000 to Address 0x00000020, as shown in Figure 62.

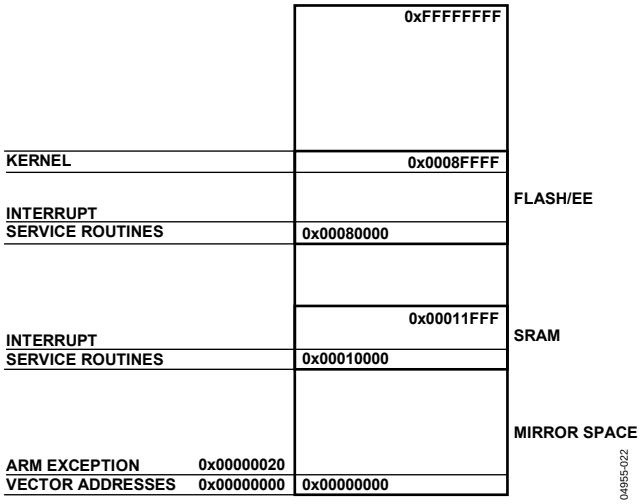


Figure 62. Remap for Exception Execution

By default, and after any reset, the Flash/EE is mirrored at the bottom of the memory array. The remap function allows the programmer to mirror the SRAM at the bottom of the memory array, which facilitates execution of exception routines from SRAM instead of from Flash/EE. This means exceptions are executed twice as fast, being executed in 32-bit ARM mode with 32-bit wide SRAM instead of 16-bit wide Flash/EE memory.

Remap Operation

When a reset occurs on the ADuC7019/20/21/22/24/25/26/27/28/29, execution automatically starts in the factory-programmed, internal configuration code. This kernel is hidden and cannot be accessed by user code. If the part is in normal mode (the BM pin is high), it executes the power-on configuration routine of the kernel and then jumps to the reset vector address, 0x00000000, to execute the user's reset exception routine.

Because the Flash/EE is mirrored at the bottom of the memory array at reset, the reset interrupt routine must always be written in Flash/EE.

The remap is done from Flash/EE by setting Bit 0 of the REMAP register. Caution must be taken to execute this command from Flash/EE, above Address 0x00080020, and not from the bottom of the array because this is replaced by the SRAM.

This operation is reversible. The Flash/EE can be remapped at Address 0x00000000 by clearing Bit 0 of the REMAP MMR. Caution must again be taken to execute the remap function from outside the mirrored area. Any type of reset remaps the Flash/EE memory at the bottom of the array.

Example source code

```
    t2val_old= T2VAL;
     T2LD = 5;
     TCON = 0x480;


  while ((T2VAL == t2val_old) || (T2VAL >
3)) //ensures timer value loaded
  IRQEN = 0x10;
//enable T2 interrupt
  PLLKEY1 = 0xAA;
  PLLCON = 0x01;
  PLLKEY2 = 0x55;

  POWKEY1 = 0x01;
  POWCON = 0x27;
// Set Core into Nap mode
  POWKEY2 = 0xF4;
```

In noisy environments, noise can couple to the external crystal pins, and PLL may lose lock momentarily. A PLL interrupt is provided in the interrupt controller. The core clock is immediately halted, and this interrupt is only serviced when the lock is restored.

In case of crystal loss, the watchdog timer should be used. During initialization, a test on the RSTSTA register can determine if the reset came from the watchdog timer.

External Clock Selection

To switch to an external clock on P0.7, configure P0.7 in Mode 1. The external clock can be up to 44 MHz, providing the tolerance is 1%.

Example source code

```
    t2val_old= T2VAL;
     T2LD = 5;
     TCON = 0x480;


  while ((T2VAL == t2val_old) || (T2VAL
> 3)) //ensures timer value loaded
  IRQEN = 0x10;
//enable T2 interrupt
  PLLKEY1 = 0xAA;
  PLLCON = 0x03; //Select external clock
  PLLKEY2 = 0x55;

  POWKEY1 = 0x01;
  POWCON = 0x27;
// Set Core into Nap mode
  POWKEY2 = 0xF4;
```

Power Control System

A choice of operating modes is available on the ADuC7019/20/21/22/24/25/26/27/28/29. Table 57 describes what part is powered on in the different modes and indicates the power-up time.

Table 58 gives some typical values of the total current consumption (analog + digital supply currents) in the different modes, depending on the clock divider bits. The ADC is turned off. Note that these values also include current consumption of the regulator and other parts on the test board where these values are measured.

Table 57. Operating Modes[1]

Mode	Core	Peripherals	PLL	XTAL/T2/T3	IRQ0 to IRQ3	Start-Up/Power-On Time
Active	X	X	X	X	X	130 ms at CD = 0
Pause		X	X	X	X	24 ns at CD = 0; 3 µs at CD = 7
Nap			X	X	X	24 ns at CD = 0; 3 µs at CD = 7
Sleep				X	X	1.58 ms
Stop					X	1.7 ms

[1] X indicates that the part is powered on.

Table 58. Typical Current Consumption at 25°C in Milliamperes

PC[2:0]	Mode	CD = 0	CD = 1	CD = 2	CD = 3	CD = 4	CD = 5	CD = 6	CD = 7
000	Active	33.1	21.2	13.8	10	8.1	7.2	6.7	6.45
001	Pause	22.7	13.3	8.5	6.1	4.9	4.3	4	3.85
010	Nap	3.8	3.8	3.8	3.8	3.8	3.8	3.8	3.8
011	Sleep	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4
100	Stop	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4

Table 70. PWMCFG Register

Name	Address	Default Value	Access
PWMCFG	0xFFFFFC10	0x0000	R/W

PWMCFG is a gate chopping register.

Table 71. PWMCFG MMR Bit Descriptions

Bit	Name	Description
15:10		Reserved.
9	CHOPLO	Low-side gate chopping enable bit.
8	CHOPHI	High-side gate chopping enable bit.
7:0	GDCLK	PWM gate chopping period (unsigned).

Table 72. PWMEN Register

Name	Address	Default Value	Access
PWMEN	0xFFFFFC20	0x0000	R/W

PWMEN allows enabling of channel outputs and crossover. See its bit definitions in Table 73.

Table 73. PWMEN MMR Bit Descriptions

Bit	Name	Description
8	0H0L_XOVR	Channel 0 output crossover enable bit. Set to 1 by user to enable Channel 0 output crossover. Cleared to 0 by user to disable Channel 0 output crossover.
7	1H1L_XOVR	Channel 1 output crossover enable bit. Set to 1 by user to enable Channel 1 output crossover. Cleared to 0 by user to disable Channel 1 output crossover.
6	2H2L_XOVR	Channel 2 output crossover enable bit. Set to 1 by user to enable Channel 2 output crossover. Cleared to 0 by user to disable Channel 2 output crossover.
5	0L_EN	0L output enable bit. Set to 1 by user to disable the 0L output of the PWM. Cleared to 0 by user to enable the 0L output of the PWM.
4	0H_EN	0H output enable bit. Set to 1 by user to disable the 0H output of the PWM. Cleared to 0 by user to enable the 0H output of the PWM.
3	1L_EN	1L output enable bit. Set to 1 by user to disable the 1L output of the PWM. Cleared to 0 by user to enable the 1L output of the PWM.
2	1H_EN	1H Output Enable Bit. Set to 1 by user to disable the 1H output of the PWM. Cleared to 0 by user to enable the 1H output of the PWM.
1	2L_EN	2L output enable bit. Set to 1 by user to disable the 2L output of the PWM. Cleared to 0 by user to enable the 2L output of the PWM.
0	2H_EN	2H output enable bit. Set to 1 by user to disable the 2H output of the PWM. Cleared to 0 by user to enable the 2H output of the PWM.

Table 74. PWMDAT0 Register

Name	Address	Default Value	Access
PWMDAT0	0xFFFFFC08	0x0000	R/W

PWMDAT0 is an unsigned 16-bit register for switching period.

Table 75. PWMDAT1 Register

Name	Address	Default Value	Access
PWMDAT1	0xFFFFFC0C	0x0000	R/W

PWMDAT1 is an unsigned 10-bit register for dead time.

Table 76. PWMCHx Registers

Name	Address	Default Value	Access
PWMCH0	0xFFFFFC14	0x0000	R/W
PWMCH1	0xFFFFFC18	0x0000	R/W
PWMCH2	0xFFFFFC1C	0x0000	R/W

PWMCH0, PWMCH1, and PWMCH2 are channel duty cycles for the three phases.

Table 77. PWMDAT2 Register

Name	Address	Default Value	Access
PWMDAT2	0xFFFFFC24	0x0000	R/W

PWMDAT2 is an unsigned 10-bit register for PWM sync pulse width.

GENERAL-PURPOSE INPUT/OUTPUT

The ADuC7019/20/21/22/24/25/26/27/28/29 provide 40 general-purpose, bidirectional I/O (GPIO) pins. All I/O pins are 5 V tolerant, meaning the GPIOs support an input voltage of 5 V.

In general, many of the GPIO pins have multiple functions (see Table 78 for the pin function definitions). By default, the GPIO pins are configured in GPIO mode.

All GPIO pins have an internal pull-up resistor (of about 100 kΩ), and their drive capability is 1.6 mA. Note that a maximum of 20 GPIOs can drive 1.6 mA at the same time. Using the GPxPAR registers, it is possible to enable/disable the pull-up resistors for the following ports: P0.0, P0.4, P0.5, P0.6, P0.7, and the eight GPIOs of P1.

The 40 GPIOs are grouped in five ports, Port 0 to Port 4 (Port x). Each port is controlled by four or five MMRs.

Note that the kernel changes P0.6 from its default configuration at reset (MRST) to GPIO mode. If MRST is used for external circuitry, an external pull-up resistor should be used to ensure that the level on P0.6 does not drop when the kernel switches mode. Otherwise, P0.6 goes low for the reset period. For example, if MRST is required for power-down, it can be reconfigured in GP0CON MMR.

The input level of any GPIO can be read at any time in the GPxDAT MMR, even when the pin is configured in a mode other than GPIO. The PLA input is always active.

When the ADuC7019/20/21/22/24/25/26/27/28/29 part enters a power-saving mode, the GPIO pins retain their state.

Table 78. GPIO Pin Function Descriptions

		Configuration			
Port	**Pin**	**00**	**01**	**10**	**11**
0	P0.0	GPIO	CMP	MS0	PLAI[7]
	P0.1	GPIO	$PWM2_H$	$\overline{BLE}$	
	P0.2	GPIO	$PWM2_L$	$\overline{BHE}$	
	P0.3	GPIO	TRST	A16	ADC_{BUSY}
	P0.4	GPIO/IRQ0	PWM_{TRIP}	MS1	PLAO[1]
	P0.5	GPIO/IRQ1	ADC_{BUSY}	MS2	PLAO[2]
	P0.6	GPIO/T1	MRST		PLAO[3]
	P0.7	GPIO	ECLK/XCLK[1]	SIN	PLAO[4]
1	P1.0	GPIO/T1	SIN	SCL0	PLAI[0]
	P1.1	GPIO	SOUT	SDA0	PLAI[1]
	P1.2	GPIO	RTS	SCL1	PLAI[2]
	P1.3	GPIO	CTS	SDA1	PLAI[3]
	P1.4	GPIO/IRQ2	RI	SCLK	PLAI[4]
	P1.5	GPIO/IRQ3	DCD	MISO	PLAI[5]
	P1.6	GPIO	DSR	MOSI	PLAI[6]
	P1.7	GPIO	DTR	$\overline{CS}$	PLAO[0]
2	P2.0	GPIO	$\overline{CONV_{START}}$[2]	SOUT	PLAO[5]
	P2.1	GPIO	$PWM0_H$	$\overline{WS}$	PLAO[6]
	P2.2	GPIO	$PWM0_L$	$\overline{RS}$	PLAO[7]
	P2.3	GPIO		AE	
	P2.4	GPIO	$PWM0_H$	MS0	
	P2.5	GPIO	$PWM0_L$	MS1	
	P2.6	GPIO	$PWM1_H$	MS2	
	P2.7	GPIO	$PWM1_L$	MS3	
3	P3.0	GPIO	$PWM0_H$	AD0	PLAI[8]
	P3.1	GPIO	$PWM0_L$	AD1	PLAI[9]
	P3.2	GPIO	$PWM1_H$	AD2	PLAI[10]
	P3.3	GPIO	$PWM1_L$	AD3	PLAI[11]
	P3.4	GPIO	$PWM2_H$	AD4	PLAI[12]
	P3.5	GPIO	$PWM2_L$	AD5	PLAI[13]
	P3.6	GPIO	PWM_{TRIP}	AD6	PLAI[14]
	P3.7	GPIO	PWM_{SYNC}	AD7	PLAI[15]
4	P4.0	GPIO		AD8	PLAO[8]
	P4.1	GPIO		AD9	PLAO[9]
	P4.2	GPIO		AD10	PLAO[10]
	P4.3	GPIO		AD11	PLAO[11]
	P4.4	GPIO		AD12	PLAO[12]
	P4.5	GPIO		AD13	PLAO[13]
	P4.6	GPIO		AD14	PLAO[14]
	P4.7	GPIO		AD15	PLAO[15]

[1] When configured in Mode 1, P0.7 is ECLK by default, or core clock output. To configure it as a clock input, the MDCLK bits in PLLCON must be set to 11.
[2] The $\overline{CONV_{START}}$ signal is active in all modes of P2.0.

Table 79. GPxCON Registers

Name	Address	Default Value	Access
GP0CON	0xFFFFF400	0x00000000	R/W
GP1CON	0xFFFFF404	0x00000000	R/W
GP2CON	0xFFFFF408	0x00000000	R/W
GP3CON	0xFFFFF40C	0x00000000	R/W
GP4CON	0xFFFFF410	0x00000000	R/W

GPxCON are the Port x control registers, which select the function of each pin of Port x as described in Table 80.

Table 80. GPxCON MMR Bit Descriptions

Bit	Description
31:30	Reserved.
29:28	Select function of the Px.7 pin.
27:26	Reserved.
25:24	Select function of the Px.6 pin.
23:22	Reserved.
21:20	Select function of the Px.5 pin.
19:18	Reserved.
17:16	Select function of the Px.4 pin.
15:14	Reserved.
13:12	Select function of the Px.3 pin.
11:10	Reserved.
9:8	Select function of the Px.2 pin.
7:6	Reserved.
5:4	Select function of the Px.1 pin.
3:2	Reserved.
1:0	Select function of the Px.0 pin.

Table 81. GPxPAR Registers

Name	Address	Default Value	Access
GP0PAR	0xFFFFF42C	0x20000000	R/W
GP1PAR	0xFFFFF43C	0x00000000	R/W

GPxPAR program the parameters for Port 0 and Port 1. Note that the GPxDAT MMR must always be written after changing the GPxPAR MMR.

Table 82. GPxPAR MMR Bit Descriptions

Bit	Description
31	Reserved.
30:29	Drive strength Px.7.
28	Pull-Up Disable Px.7.
27	Reserved.
26:25	Drive strength Px.6.
24	Pull-Up Disable Px.6.
23	Reserved.
22:21	Drive strength Px.5.
20	Pull-Up Disable Px.5.
19	Reserved.
18:17	Drive strength Px.4.
16	Pull-Up Disable Px.4.
15	Reserved.
14:13	Drive strength Px.3.
12	Pull-Up Disable Px.3.
11	Reserved.
10:9	Drive strength Px.2.
8	Pull-Up Disable Px.2.
7	Reserved.
6:5	Drive strength Px.1.
4	Pull-Up Disable Px.1.
3	Reserved.
2:1	Drive strength Px.0.
0	Pull-Up Disable Px.0.

Table 99. COMDIV1 Register

Name	Address	Default Value	Access
COMDIV1	0xFFFF0704	0x00	R/W

COMDIV1 is a divisor latch (high byte) register.

Table 100. COMIID0 Register

Name	Address	Default Value	Access
COMIID0	0xFFFF0708	0x01	R

COMIID0 is the interrupt identification register.

Table 101. COMIID0 MMR Bit Descriptions

Bit 2:1 Status Bits	Bit 0 NINT	Priority	Definition	Clearing Operation
00	1	N/A	No interrupt	N/A
11	0	1 (Highest)	Receive line status interrupt	Read COMSTA0
10	0	2	Receive buffer full interrupt	Read COMRX
01	0	3	Transmit buffer empty interrupt	Write data to COMTX or read COMIID0
00	0	4 (Lowest)	Modem status interrupt	Read COMSTA1

Table 102. COMCON0 Register

Name	Address	Default Value	Access
COMCON0	0xFFFF070C	0x00	R/W

COMCON0 is the line control register.

Table 103. COMCON0 MMR Bit Descriptions

Bit	Name	Description
7	DLAB	Divisor latch access. Set by user to enable access to the COMDIV0 and COMDIV1 registers. Cleared by user to disable access to COMDIV0 and COMDIV1 and enable access to COMRX and COMTX.
6	BRK	Set break. Set by user to force SOUT to 0. Cleared to operate in normal mode.
5	SP	Stick parity. Set by user to force parity to defined values: 1 if EPS = 1 and PEN = 1, 0 if EPS = 0 and PEN = 1.
4	EPS	Even parity select bit. Set for even parity. Cleared for odd parity.
3	PEN	Parity enable bit. Set by user to transmit and check the parity bit. Cleared by user for no parity transmission or checking.
2	STOP	Stop bit. Set by user to transmit 1.5 stop bits if the word length is five bits or 2 stop bits if the word length is six bits, seven bits, or eight bits. The receiver checks the first stop bit only, regardless of the number of stop bits selected. Cleared by user to generate 1 stop bit in the transmitted data.
1:0	WLS	Word length select: 00 = five bits, 01 = six bits, 10 = seven bits, 11 = eight bits.

Table 104. COMCON1 Register

Name	Address	Default Value	Access
COMCON1	0xFFFF0710	0x00	R/W

COMCON1 is the modem control register.

Table 105. COMCON1 MMR Bit Descriptions

Bit	Name	Description
7:5		Reserved.
4	LOOPBACK	Loopback. Set by user to enable loopback mode. In loopback mode, SOUT (see Table 78) is forced high. The modem signals are also directly connected to the status inputs (RTS to CTS and DTR to DSR). Cleared by user to be in normal mode.
3	PEN	Parity enable bit. Set by user to transmit and check the parity bit. Cleared by user for no parity transmission or checking.
2	STOP	Stop bit. Set by user to transmit 1.5 stop bits if the word length is five bits, or 2 stop bits if the word length is six bits, seven bits, or eight bits. The receiver checks the first stop bit only, regardless of the number of stop bits selected. Cleared by user to generate 1 stop bit in the transmitted data.
1	RTS	Request to send. Set by user to force the RTS output to 0. Cleared by user to force the RTS output to 1.
0	DTR	Data terminal ready. Set by user to force the DTR output to 0. Cleared by user to force the DTR output to 1.

Table 106. COMSTA0 Register

Name	Address	Default Value	Access
COMSTA0	0xFFFF0714	0x60	R

COMSTA0 is the line status register.

Table 107. COMSTA0 MMR Bit Descriptions

Bit	Name	Description
7		Reserved.
6	TEMT	COMTX and shift register empty status bit. Set automatically if COMTX and shift register are empty. Cleared automatically when writing to COMTX.
5	THRE	COMTX empty. Set automatically if COMTX is empty. Cleared automatically when writing to COMTX.
4	BI	Break error. Set when SIN is held low for more than the maximum word length. Cleared automatically.
3	FE	Framing error. Set when an invalid stop bit occurs. Cleared automatically.
2	PE	Parity error. Set when a parity error occurs. Cleared automatically.
1	OE	Overrun error. Set automatically if data is over-written before being read. Cleared automatically.
0	DR	Data ready. Set automatically when COMRX is full. Cleared by reading COMRX.

Table 108. COMSTA1 Register

Name	Address	Default Value	Access
COMSTA1	0xFFFF0718	0x00	R

COMSTA1 is a modem status register.

Table 109. COMSTA1 MMR Bit Descriptions

Bit	Name	Description
7	DCD	Data carrier detect.
6	RI	Ring indicator.
5	DSR	Data set ready.
4	CTS	Clear to send.
3	DDCD	Delta DCD. Set automatically if DCD changed state since last COMSTA1 read. Cleared automatically by reading COMSTA1.
2	TERI	Trailing edge RI. Set if RI changed from 0 to 1 since COMSTA1 was last read. Cleared automatically by reading COMSTA1.
1	DDSR	Delta DSR. Set automatically if DSR changed state since COMSTA1 was last read. Cleared automatically by reading COMSTA1.
0	DCTS	Delta CTS. Set automatically if CTS changed state since COMSTA1 was last read. Cleared automatically by reading COMSTA1.

Table 110. COMSCR Register

Name	Address	Default Value	Access
COMSCR	0xFFFF071C	0x00	R/W

COMSCR is an 8-bit scratch register used for temporary storage. It is also used in network addressable UART mode.

Table 111. COMDIV2 Register

Name	Address	Default Value	Access
COMDIV2	0xFFFF072C	0x0000	R/W

COMDIV2 is a 16-bit fractional baud divide register.

Table 112. COMDIV2 MMR Bit Descriptions

Bit	Name	Description
15	FBEN	Fractional baud rate generator enable bit. Set by user to enable the fractional baud rate generator. Cleared by user to generate baud rate using the standard 450 UART baud rate generator.
14:13		Reserved.
12:11	FBM[1:0]	M if FBM = 0, M = 4 (see the Fractional Divider section).
10:0	FBN[10:0]	N (see the Fractional Divider section).

Network Addressable UART Mode

This mode connects the MicroConverter to a 256-node serial network, either as a hardware single master or via software in a multimaster network. Bit 7 (ENAM) of the COMIEN1 register must be set to enable UART in network addressable mode (see Table 114). Note that there is no parity check in this mode.

Network Addressable UART Register Definitions

Four additional registers, COMIEN0, COMIEN1, COMIID1, and COMADR are used in network addressable UART mode only.

In network address mode, the least significant bit of the COMIEN1 register is the transmitted network address control bit. If set to 1, the device is transmitting an address. If cleared to 0, the device is transmitting data. For example, the following master-based code transmits the slave's address followed by the data:

```
  COMIEN1  = 0xE7;       //Setting ENAM,
E9BT, E9BR, ETD, NABP
  COMTX = 0xA0;  // Slave address is 0xA0
  while(!(0x020==(COMSTA0 & 0x020))){} //
wait for adr tx to finish.
  COMIEN1  = 0xE6;       //  Clear NAB bit
to indicate Data is coming
   COMTX = 0x55; // Tx data to slave: 0x55
```

Table 113. COMIEN1 Register

Name	Address	Default Value	Access
COMIEN1	0xFFFF0720	0x04	R/W

COMIEN1 is an 8-bit network enable register.

Table 114. COMIEN1 MMR Bit Descriptions

Bit	Name	Description
7	ENAM	Network address mode enable bit. Set by user to enable network address mode. Cleared by user to disable network address mode.
6	E9BT	9-bit transmit enable bit. Set by user to enable 9-bit transmit. ENAM must be set. Cleared by user to disable 9-bit transmit.
5	E9BR	9-bit receive enable bit. Set by user to enable 9-bit receive. ENAM must be set. Cleared by user to disable 9-bit receive.
4	ENI	Network interrupt enable bit.
3	E9BD	Word length. Set for 9-bit data. E9BT has to be cleared. Cleared for 8-bit data.
2	ETD	Transmitter pin driver enable bit. Set by user to enable SOUT pin as an output in slave mode or multimaster mode. Cleared by user; SOUT is three-state.
1	NABP	Network address bit. Interrupt polarity bit.
0	NAB	Network address bit (if NABP = 1). Set by user to transmit the slave address. Cleared by user to transmit data.

Table 115. COMIID1 Register

Name	Address	Default Value	Access
COMIID1	0xFFFF0724	0x01	R

COMIID1 is an 8-bit network interrupt register. Bit 7 to Bit 4 are reserved (see Table 116).

Table 153. PLAADC Register

Name	Address	Default Value	Access
PLAADC	0xFFFF0B48	0x00000000	R/W

PLAADC is the PLA source for the ADC start conversion signal.

Table 154. PLAADC MMR Bit Descriptions

Bit	Value	Description
31:5		Reserved.
4		ADC start conversion enable bit. Set by user to enable ADC start conversion from PLA. Cleared by user to disable ADC start conversion from PLA.
3:0		ADC start conversion source.
	0000	PLA Element 0.
	0001	PLA Element 1.
	1111	PLA Element 15.

Table 155. PLADIN Register

Name	Address	Default Value	Access
PLADIN	0xFFFF0B4C	0x00000000	R/W

PLADIN is a data input MMR for PLA.

Table 156. PLADIN MMR Bit Descriptions

Bit	Description
31:16	Reserved.
15:0	Input bit to Element 15 to Element 0.

Table 157. PLADOUT Register

Name	Address	Default Value	Access
PLADOUT	0xFFFF0B50	0x00000000	R

PLADOUT is a data output MMR for PLA. This register is always updated.

Table 158. PLADOUT MMR Bit Descriptions

Bit	Description
31:16	Reserved.
15:0	Output bit from Element 15 to Element 0.

Table 159. PLALCK Register

Name	Address	Default Value	Access
PLALCK	0xFFFF0B54	0x00	W

PLALCK is a PLA lock option. Bit 0 is written only once. When set, it does not allow modifying any of the PLA MMRs, except PLADIN. A PLA tool is provided in the development system to easily configure the PLA.

Timer1 (General-Purpose Timer)

Timer1 is a general-purpose, 32-bit timer (count down or count up) with a programmable prescaler. The source can be the 32 kHz external crystal, the core clock frequency, or an external GPIO (P1.0 or P0.6). The maximum frequency of the clock input is 44 Mhz). This source can be scaled by a factor of 1, 16, 256, or 32,768.

The counter can be formatted as a standard 32-bit value or as hours: minutes: seconds: hundredths.

Timer1 has a capture register (T1CAP) that can be triggered by a selected IRQ source initial assertion. This feature can be used to determine the assertion of an event more accurately than the precision allowed by the RTOS timer when the IRQ is serviced.

Timer1 can be used to start ADC conversions as shown in the block diagram in Figure 78.

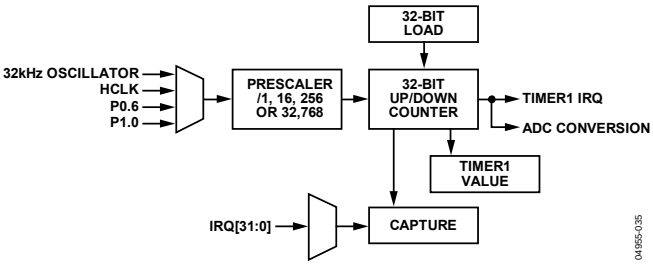


Figure 78. Timer1 Block Diagram

The Timer1 interface consists of five MMRs: T1LD, T1VAL, T1CON, T1CLRI, and T1CAP.

Table 177. T1LD Register

Name	Address	Default Value	Access
T1LD	0xFFFF0320	0x00000000	R/W

T1LD is a 32-bit load register.

Table 178. T1VAL Register

Name	Address	Default Value	Access
T1VAL	0xFFFF0324	0xFFFFFFFF	R

T1VAL is a 32-bit read-only register that represents the current state of the counter.

Table 179. T1CON Register

Name	Address	Default Value	Access
T1CON	0xFFFF0328	0x0000	R/W

T1CON is the configuration MMR described in Table 180.

HARDWARE DESIGN CONSIDERATIONS

POWER SUPPLIES

The ADuC7019/20/21/22/24/25/26/27/28/29 operational power supply voltage range is 2.7 V to 3.6 V. Separate analog and digital power supply pins (AV_{DD} and IOV_{DD}, respectively) allow AV_{DD} to be kept relatively free of noisy digital signals often present on the system IOV_{DD} line. In this mode, the part can also operate with split supplies; that is, it can use different voltage levels for each supply. For example, the system can be designed to operate with an IOV_{DD} voltage level of 3.3 V whereas the AV_{DD} level can be at 3 V or vice versa. A typical split supply configuration is shown in Figure 87.

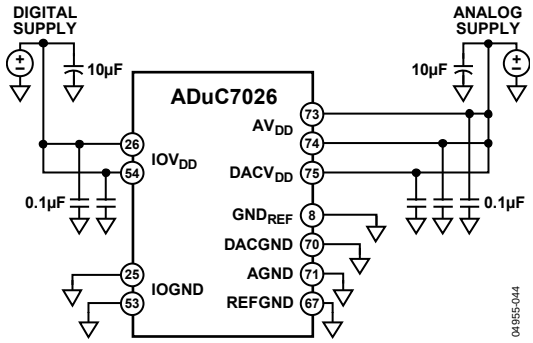


Figure 87. External Dual Supply Connections

As an alternative to providing two separate power supplies, the user can reduce noise on AV_{DD} by placing a small series resistor and/or ferrite bead between AV_{DD} and IOV_{DD} and then decoupling AV_{DD} separately to ground. An example of this configuration is shown in Figure 88. With this configuration, other analog circuitry (such as op amps and voltage reference) can be powered from the AV_{DD} supply line as well.

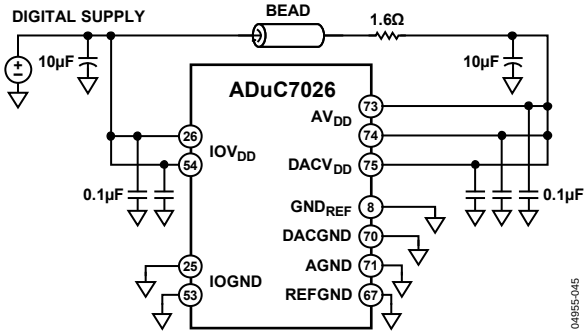


Figure 88. External Single Supply Connections

Note that in both Figure 87 and Figure 88, a large value (10 µF) reservoir capacitor sits on IOV_{DD}, and a separate 10 µF capacitor sits on AV_{DD}. In addition, local small-value (0.1 µF) capacitors are located at each AV_{DD} and IOV_{DD} pin of the chip. As per standard design practice, be sure to include all of these capacitors and ensure that the smaller capacitors are close to each AV_{DD} pin with trace lengths as short as possible. Connect the ground terminal of each of these capacitors directly to the underlying ground plane.

Finally, note that the analog and digital ground pins on the ADuC7019/20/21/22/24/25/26/27/28/29 must be referenced to the same system ground reference point at all times.

IOV_{DD} Supply Sensitivity

The IOV_{DD} supply is sensitive to high frequency noise because it is the supply source for the internal oscillator and PLL circuits. When the internal PLL loses lock, the clock source is removed by a gating circuit from the CPU, and the ARM7TDMI core stops executing code until the PLL regains lock. This feature ensures that no flash interface timings or ARM7TDMI timings are violated.

Typically, frequency noise greater than 50 kHz and 50 mV p-p on top of the supply causes the core to stop working.

If decoupling values recommended in the Power Supplies section do not sufficiently dampen all noise sources below 50 mV on IOV_{DD}, a filter such as the one shown in Figure 89 is recommended.

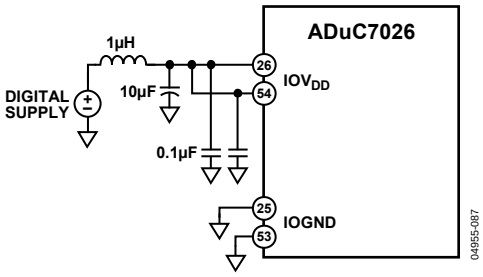


Figure 89. Recommended IOV_{DD} Supply Filter

Linear Voltage Regulator

Each ADuC7019/20/21/22/24/25/26/27/28/29 requires a single 3.3 V supply, but the core logic requires a 2.6 V supply. An on-chip linear regulator generates the 2.6 V from IOV_{DD} for the core logic. The LV_{DD} pin is the 2.6 V supply for the core logic. An external compensation capacitor of 0.47 µF must be connected between LV_{DD} and DGND (as close as possible to these pins) to act as a tank of charge as shown in Figure 90.

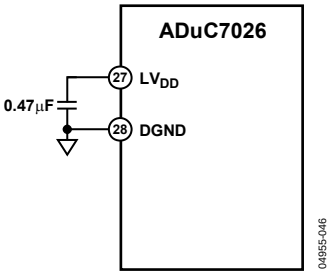


Figure 90. Voltage Regulator Connections

The LV_{DD} pin should not be used for any other chip. It is also recommended to use excellent power supply decoupling on IOV_{DD} to help improve line regulation performance of the on-chip voltage regulator.

POWER-ON RESET OPERATION

An internal power-on reset (POR) is implemented on the ADuC7019/20/21/22/24/25/26/27/28/29. For LV_{DD} below 2.35 V typical, the internal POR holds the part in reset. As LV_{DD} rises above 2.35 V, an internal timer times out for, typically, 128 ms before the part is released from reset. The user must ensure that the power supply IOV_{DD} reaches a stable 2.7 V minimum level by this time. Likewise, on power-down, the internal POR holds the part in reset until LV_{DD} drops below 2.35 V.

Figure 94 illustrates the operation of the internal POR in detail.

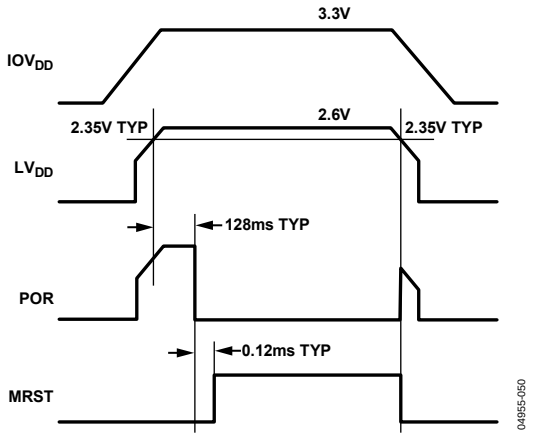


Figure 94. Internal Power-On Reset Operation

TYPICAL SYSTEM CONFIGURATION

A typical ADuC7020 configuration is shown in Figure 95. It summarizes some of the hardware considerations discussed in the previous sections. The bottom of the CSP package has an exposed pad that must be soldered to a metal plate on the board for mechanical reasons. The metal plate of the board can be connected to ground.

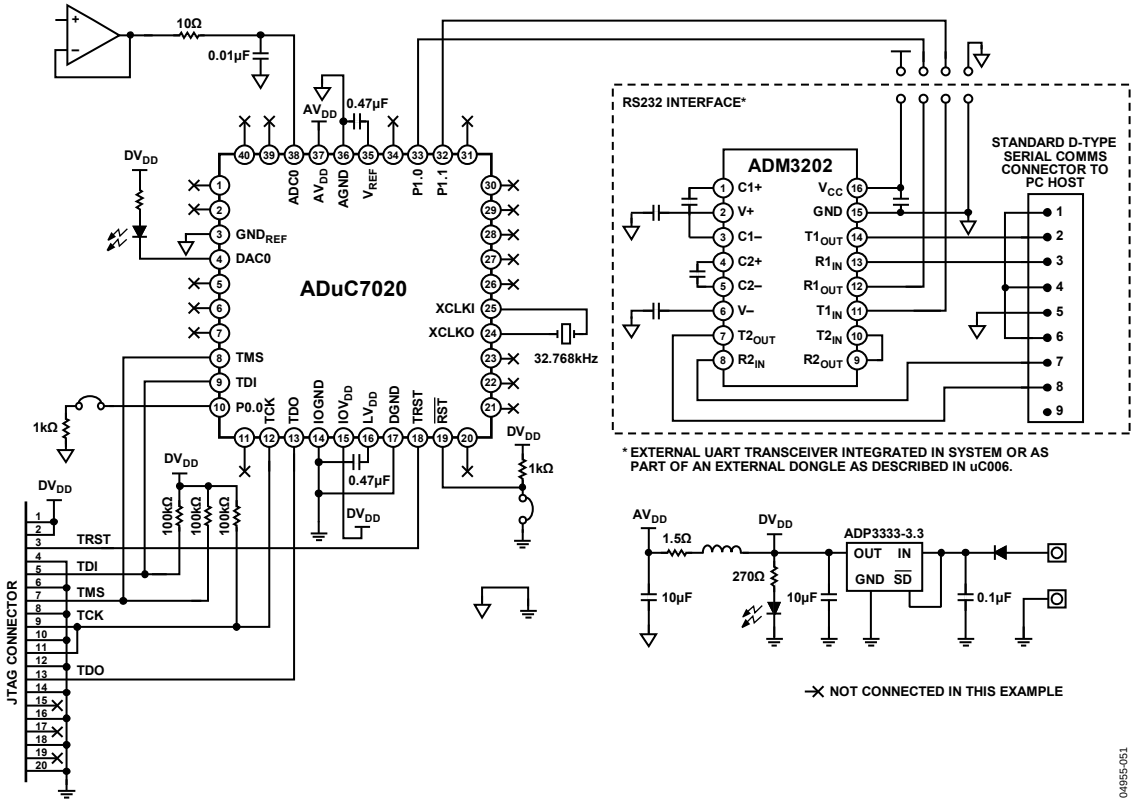


Figure 95. Typical System Configuration