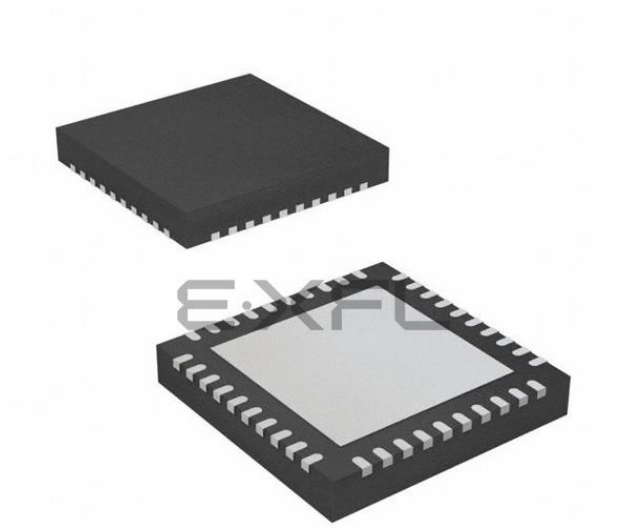

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	44MHz
Connectivity	EBI/EMI, I²C, SPI, UART/USART
Peripherals	PLA, PWM, PSM, Temp Sensor, WDT
Number of I/O	13
Program Memory Size	62KB (31K x16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 32
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	40-VFQFN Exposed Pad, CSP
Supplier Device Package	40-LFCSP-VQ (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/aduc7021bcpz62-rl7

REVISION HISTORY

12/15—Rev. F to Rev. G

Changed CP-40-1 to CP-40-9 ..... Universal
Updated Outline Dimensions 97
Deleted Figure 96 (CP-40-1); Renumbered Sequentially 97
Changes to Ordering Guide 101

5/13—Rev. E to Rev. F

Changes to Figure 1 1
Added Figure 2 to Figure 10; Renumbered Sequentially 4
Changes to Figure 19; Added Figure 20 21
Changes to EPAD Note in Figure 21 and Figure 22 22
Changes to EPAD Note in Table 11 23
Changes to EPAD Note in Figure 23 25
Changes to EPAD Note in Table 12 26
Changes to Table 14 31
Changes to Table 15 33
Changes to Table 82 68
Added Table 83, Figure 73, Figure 74, Following Text, and Table 84; Renumbered Sequentially 69
Changes to Bit 2 Description, Table 98 71
Changes to Table 101 72
Changes to Timer2 (Wake-Up Timer) Section 87
Changes to Figure 94 95
Updated Outline Dimensions 97
Changes to Ordering Guide 101

7/12—Rev. D to Rev. E

Changed SCLOCK to SCLK When Refering to SPI Clock, SPIMISO to MISO when Refering to SPI MISO, SPIMOSI to MOSI when Refering to SPI MOSI, and SPICSL to $\overline{CS}$ when Refering to SPI Chip Select ..... Universal
Changes to Table 4, Table 5, and Figure 5 11
Changes to Endnote 1 in Table 6 and Figure 6 12
Changes to Table 7 and Figure 7 13
Changes to Table 8 and Figure 8 14
Changes to Table 9 and Figure 9 15
Changed EPAD Note in Figure 12 and Table 11 18
Changed EPAD Note in Figure 13 and Table 12 21
Changes to Bit 6 in Table 18 43
Changes to Example Source Code (External Crystal Selection) Section and Example Source Code (External Clock Selection) Section 55
Changes to Serial Peripheral Interface Section 69
Changes to SPICON[10] and SPICON[9] Descriptions in Table 123 70
Changes to Timer Interval Down Equation and Added Timer Interval Up Equation 79
Added Hour:Minute:Second:1/128 Format Section 80
Changes to Table 189 84
Removed CP-40-10 Package 92
Changes to Ordering Guide 96

5/11—Rev. C to Rev. D

Changes to Table 4 11
Changes to Table 105 67
Updated Outline Dimensions 91
Changes to Ordering Guide 94

12/09—Rev. B to Rev. C

Added ADuC7029 Part ..... Universal
Added Table Numbers and Renumbered Tables ..... Universal
Changes to Figure Numbers ..... Universal
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3/07—Rev. A to Rev. B

Added ADuC7028 Part ..... Universal
Updated Format ..... Universal
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Changes to Figure 32 Caption 30
Changes to Table 14 35
Changes to ADC Circuit Overview Section 38
Changes to Programming Section 44
Changes to Flash/EE Control Interface Section 45
Changes to Table 24 47
Changes to RSTCLR Register Section 48
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Changes to Comparator Section 50
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Changes to Digital Peripherals Section 54
Changes to Interrupt System Section 75
Changes to Timers Section 76
Changes to External Memory Interfacing Section 80
Added IOV_{DD} Supply Sensitivity Section 84
Changes to Ordering Guide 90

1/06—Rev. 0 to Rev. A

Changes to Table 1 6
Added the Flash/EE Memory Reliability Section 43
Changes to Table 30 52
Changes to Serial Peripheral Interface 66
Changes to Ordering Guide 90

10/05—Revision 0: Initial Version

SPECIFICATIONS

AV_{DD} = IOV_{DD} = 2.7 V to 3.6 V, V_{REF} = 2.5 V internal reference, f_{CORE} = 41.78 MHz, T_A = −40°C to +125°C, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
ADC CHANNEL SPECIFICATIONS					Eight acquisition clocks and fADC/2
ADC Power-Up Time		5		µs	
DC Accuracy[1, 2]					
Resolution	12			Bits	
Integral Nonlinearity		±0.6	±1.5	LSB	2.5 V internal reference
		±1.0		LSB	1.0 V external reference
Differential Nonlinearity[3, 4]		±0.5	+1/−0.9	LSB	2.5 V internal reference
		+0.7/−0.6		LSB	1.0 V external reference
DC Code Distribution		1		LSB	ADC input is a dc voltage
ENDPOINT ERRORS[5]					
Offset Error		±1	±2	LSB	
Offset Error Match		±1		LSB	
Gain Error		±2	±5	LSB	
Gain Error Match		±1		LSB	
DYNAMIC PERFORMANCE					f_{IN} = 10 kHz sine wave, f_{SAMPLE} = 1 MSPS
Signal-to-Noise Ratio (SNR)		69		dB	Includes distortion and noise components
Total Harmonic Distortion (THD)		−78		dB	
Peak Harmonic or Spurious Noise (PHSN)		−75		dB	
Channel-to-Channel Crosstalk		−80		dB	Measured on adjacent channels
ANALOG INPUT					
Input Voltage Ranges					
Differential Mode			V_{CM}[6] ± V_{REF}/2	V	
Single-Ended Mode			0 to V_{REF}	V	
Leakage Current		±1	±6	µA	
Input Capacitance		20		pF	During ADC acquisition
ON-CHIP VOLTAGE REFERENCE					0.47 µF from V_{REF} to AGND
Output Voltage		2.5		V	
Accuracy			±5	mV	T_A = 25°C
Reference Temperature Coefficient		±40		ppm/°C	
Power Supply Rejection Ratio		75		dB	
Output Impedance		70		Ω	T_A = 25°C
Internal V_{REF} Power-On Time		1		ms	
EXTERNAL REFERENCE INPUT					
Input Voltage Range	0.625		AV_{DD}	V	
DAC CHANNEL SPECIFICATIONS					R_L = 5 kΩ, C_L = 100 pF
DC Accuracy[7]					
Resolution		12		Bits	
Relative Accuracy		±2		LSB	
Differential Nonlinearity			±1	LSB	Guaranteed monotonic
Offset Error			±15	mV	2.5 V internal reference
Gain Error[8]			±1	%	
Gain Error Mismatch		0.1		%	% of full scale on DAC0
ANALOG OUTPUTS					
Output Voltage Range_0		0 to DAC_{REF}		V	DAC_{REF} range: DACGND to $DACV_{DD}$
Output Voltage Range_1		0 to 2.5		V	
Output Voltage Range_2		0 to $DACV_{DD}$		V	
Output Impedance		2		Ω	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
MCU CLOCK RATE					
From 32 kHz Internal Oscillator		326		kHz	CD[12] = 7
From 32 kHz External Crystal		41.78		MHz	CD[12] = 0
Using an External Clock	0.05		44	MHz	T_A = 85°C
	0.05		41.78	MHz	T_A = 125°C
START-UP TIME					Core clock = 41.78 MHz
At Power-On		130		ms	
From Pause/Nap Mode		24		ns	CD[12] = 0
		3.06		µs	CD[12] = 7
From Sleep Mode		1.58		ms	
From Stop Mode		1.7		ms	
PROGRAMMABLE LOGIC ARRAY (PLA)					
Pin Propagation Delay		12		ns	From input pin to output pin
Element Propagation Delay		2.5		ns	
POWER REQUIREMENTS[13, 14]					
Power Supply Voltage Range					
AV_{DD} to AGND and IOV_{DD} to IOGND	2.7		3.6	V	
Analog Power Supply Currents					
AV_{DD} Current		200		µA	ADC in idle mode; all parts except ADuC7019
		400		µA	ADC in idle mode; ADuC7019 only
$DACV_{DD}$ Current[15]		3	25	µA	
Digital Power Supply Current					
IOV_{DD} Current in Normal Mode					Code executing from Flash/EE
		7	10	mA	CD[12] = 7
		11	15	mA	CD[12] = 3
		40	45	mA	CD[12] = 0 (41.78 MHz clock)
IOV_{DD} Current in Pause Mode		25	30	mA	CD[12] = 0 (41.78 MHz clock)
IOV_{DD} Current in Sleep Mode		250	400	µA	T_A = 85°C
		600	1000	µA	T_A = 125°C
Additional Power Supply Currents					
ADC		2		mA	@ 1 MSPS
		0.7		mA	@ 62.5 kSPS
DAC		700		µA	per DAC
ESD TESTS					2.5 V reference, T_A = 25°C
HBM Passed Up To			4	kV	
FCIDM Passed Up To			0.5	kV	

[1] All ADC channel specifications are guaranteed during normal MicroConverter core operation.
[2] Apply to all ADC input channels.
[3] Measured using the factory-set default values in the ADC offset register (ADCOF) and gain coefficient register (ADCGN).
[4] Not production tested but supported by design and/or characterization data on production release.
[5] Measured using the factory-set default values in ADCOF and ADCGN with an external AD845 op amp as an input buffer stage as shown in Figure 59. Based on external ADC system components; the user may need to execute a system calibration to remove external endpoint errors and achieve these specifications (see the Calibration section).
[6] The input signal can be centered on any dc common-mode voltage (V_{CM}) as long as this value is within the ADC voltage input range specified.
[7] DAC linearity is calculated using a reduced code range of 100 to 3995.
[8] DAC gain error is calculated using a reduced code range of 100 to internal 2.5 V V_{REF}.
[9] Endurance is qualified as per JEDEC Standard 22, Method A117 and measured at −40°C, +25°C, +85°C, and +125°C.
[10] Retention lifetime equivalent at junction temperature (T_J) = 85°C as per JEDEC Standard 22m, Method A117. Retention lifetime derates with junction temperature.
[11] Test carried out with a maximum of eight I/Os set to a low output level.
[12] See the POWCON register.
[13] Power supply current consumption is measured in normal, pause, and sleep modes under the following conditions: normal mode with 3.6 V supply, pause mode with 3.6 V supply, and sleep mode with 3.6 V supply.
[14] IOV_{DD} power supply current decreases typically by 2 mA during a Flash/EE erase cycle.
[15] On the ADuC7019/20/21/22, this current must be added to the AV_{DD} current.

Table 3. External Memory Read Cycle

Parameter	Min	Typ	Max	Unit
CLK[1]	1/MD clock	ns typ × (POWCON[2:0] + 1)		
$t_{MS\_AFTER\_CLKH}$	4		8	ns
$t_{ADDR\_AFTER\_CLKH}$	4		16	ns
$t_{AE\_H\_AFTER\_MS}$		½ CLK		
t_{AE}		(XMxPAR[14:12] + 1) × CLK		
$t_{HOLD\_ADDR\_AFTER\_AE\_L}$		½ CLK + (! XMxPAR[10]) × CLK		
$t_{RD\_L\_AFTER\_AE\_L}$		½ CLK + (! XMxPAR[10]+ ! XMxPAR[9]) × CLK		
$t_{RD\_H\_AFTER\_CLKH}$	0		4	
t_{RD}		(XMxPAR[3:0] + 1) × CLK		
$t_{DATA\_BEFORE\_RD\_H}$	16			ns
$t_{DATA\_AFTER\_RD\_H}$	8	+ (! XMxPAR[9]) × CLK		
$t_{RELEASE\_MS\_AFTER\_RD\_H}$		1 × CLK		

[1] See Table 78.

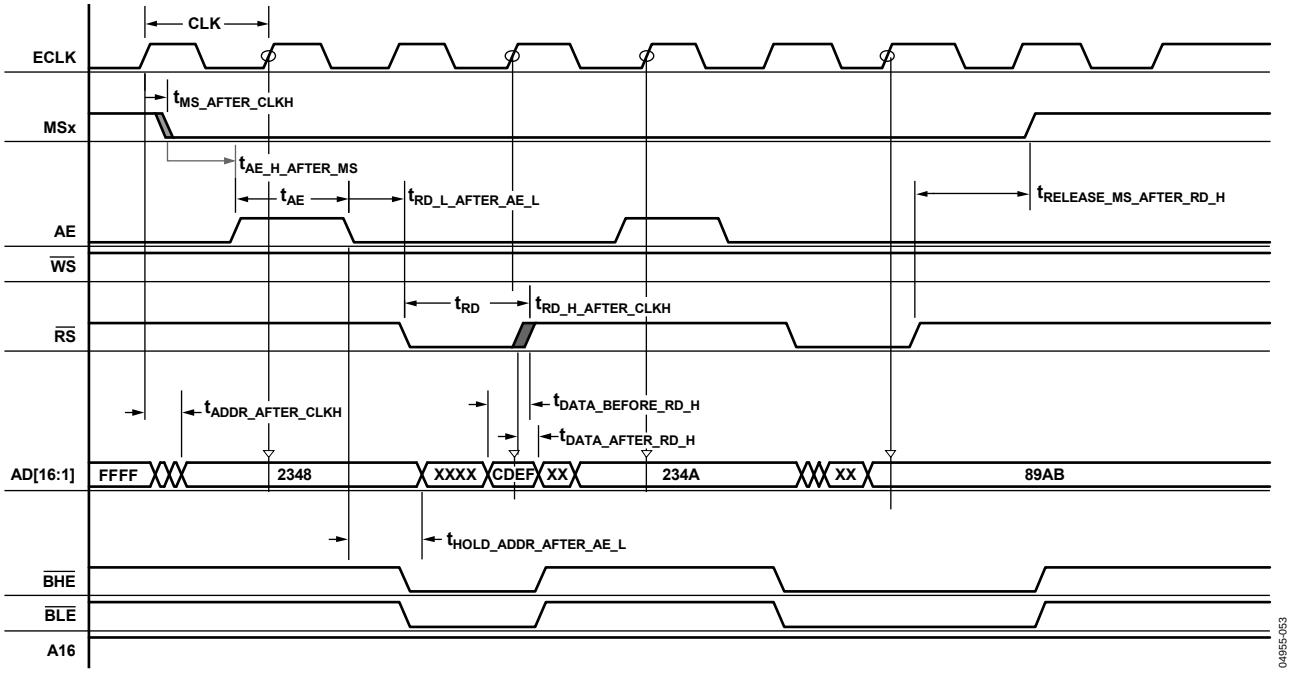
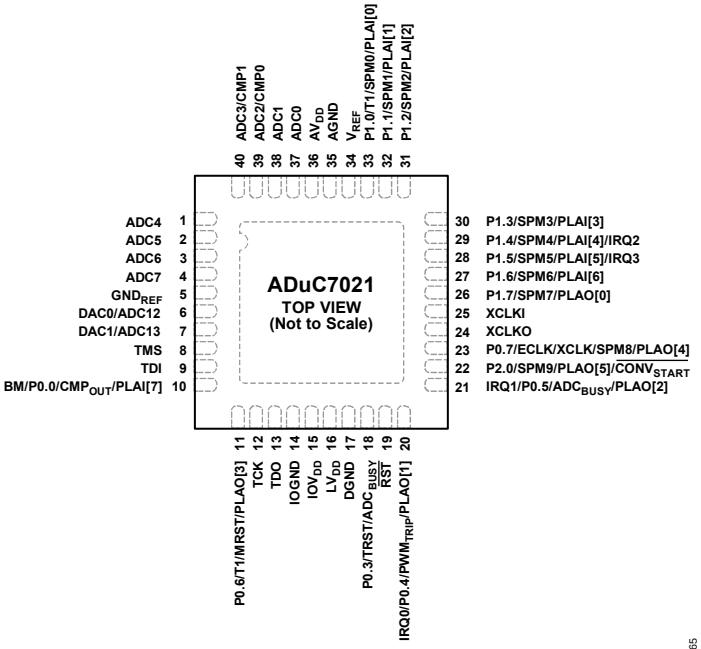


Figure 13. External Memory Read Cycle (See Table 78)



NOTES
1. THE EXPOSED PAD MUST BE SOLDERED FOR MECHANICAL PURPOSES AND LEFT UNCONNECTED.

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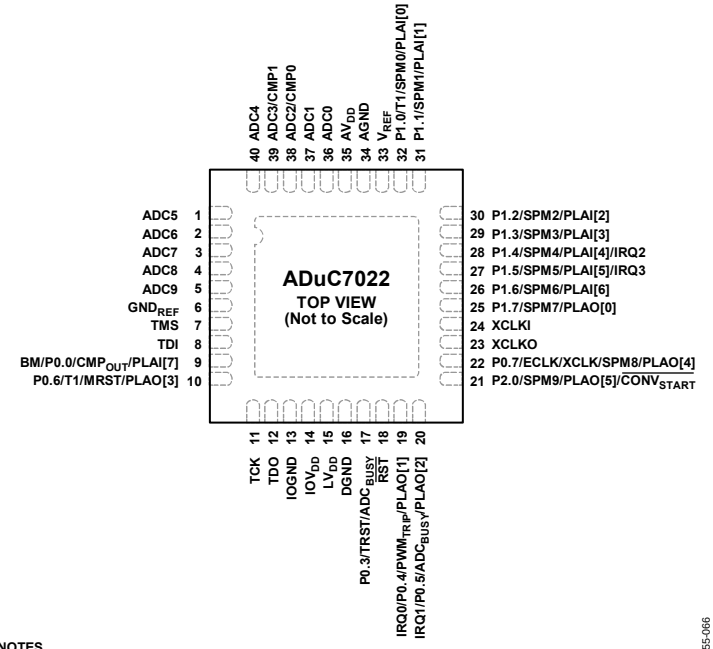
Figure 21. 40-Lead LFCSP_WQ Pin Configuration (ADuC7021)



NOTES
1. THE EXPOSED PAD MUST BE SOLDERED FOR MECHANICAL PURPOSES AND LEFT UNCONNECTED.

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Figure 22. 40-Lead LFCSP_WQ Pin Configuration (ADuC7022)

Pin No.				
7019/7020	7021	7022	Mnemonic	Description
22	22	21	P2.0/SPM9/PLAO[5]/$\overline{CONV_{START}}$	Serial Port Multiplexed. General-Purpose Input and Output Port 2.0/UART/ Programmable Logic Array Output Element 5/Start Conversion Input Signal for ADC.
23	23	22	P0.7/ECLK/XCLK/SPM8/PLAO[4]	Serial Port Multiplexed. General-Purpose Input and Output Port 0.7/ Output for External Clock Signal/Input to the Internal Clock Generator Circuits/UART/ Programmable Logic Array Output Element 4.
24	24	23	XCLKO	Output from the Crystal Oscillator Inverter.
25	25	24	XCLKI	Input to the Crystal Oscillator Inverter and Input to the Internal Clock Generator Circuits.
26	26	25	P1.7/SPM7/PLAO[0]	Serial Port Multiplexed. General-Purpose Input and Output Port 1.7/UART, SPI/Programmable Logic Array Output Element 0.
27	27	26	P1.6/SPM6/PLAI[6]	Serial Port Multiplexed. General-Purpose Input and Output Port 1.6/UART, SPI/Programmable Logic Array Input Element 6.
28	28	27	P1.5/SPM5/PLAI[5]/IRQ3	Serial Port Multiplexed. General-Purpose Input and Output Port 1.5/UART, SPI/Programmable Logic Array Input Element 5/External Interrupt Request 3, Active High.
29	29	28	P1.4/SPM4/PLAI[4]/IRQ2	Serial Port Multiplexed. General-Purpose Input and Output Port 1.4/UART, SPI/Programmable Logic Array Input Element 4/External Interrupt Request 2, Active High.
30	30	29	P1.3/SPM3/PLAI[3]	Serial Port Multiplexed. General-Purpose Input and Output Port 1.3/UART, I2C1/Programmable Logic Array Input Element 3.
31	31	30	P1.2/SPM2/PLAI[2]	Serial Port Multiplexed. General-Purpose Input and Output Port 1.2/UART, I2C1/Programmable Logic Array Input Element 2.
32	32	31	P1.1/SPM1/PLAI[1]	Serial Port Multiplexed. General-Purpose Input and Output Port 1.1/UART, I2C0/Programmable Logic Array Input Element 1.
33	33	32	P1.0/T1/SPM0/PLAI[0]	Serial Port Multiplexed. General-Purpose Input and Output Port 1.0/ Timer1 Input/UART, I2C0/Programmable Logic Array Input Element 0.
34	–	–	P4.2/PLAO[10]	General-Purpose Input and Output Port 4.2/Programmable Logic Array Output Element 10.
35	34	33	V_{REF}	2.5 V Internal Voltage Reference. Must be connected to a 0.47 µF capacitor when using the internal reference.
36	35	34	AGND	Analog Ground. Ground reference point for the analog circuitry.
37	36	35	AV_{DD}	3.3 V Analog Power.
0	0	0	EP	Exposed Pad. The pin configuration for the ADuC7019/ADuC7020/ ADuC7021/ADuC7022 has an exposed pad that must be soldered for mechanical purposes and left unconnected.

Pin No.	Mnemonic	Description
D7	P1.6/SPM6/PLAI[6]	Serial Port Multiplexed. General-Purpose Input and Output Port 1.6/UART, SPI/Programmable Logic Array Input Element 6.
D8	IOV_{DD}	3.3 V Supply for GPIO (see Table 78) and Input of the On-Chip Voltage Regulator.
E1	DAC3/ADC15	DAC3 Voltage Output/ADC Input 15.
E2	DAC2/ADC14	DAC2 Voltage Output/ADC Input 14.
E3	DAC1/ADC13	DAC1 Voltage Output/ADC Input 13.
E4	P3.0/$PWM0_H$/PLAI[8]	General-Purpose Input and Output Port 3.0/PWM Phase 0 High-Side Output/Programmable Logic Array Input Element 8.
E5	P3.2/$PWM1_H$/PLAI[10]	General-Purpose Input and Output Port 3.2/PWM Phase 1 High-Side Output/Programmable Logic Array Input Element 10.
E6	P1.5/SPM5/PLAI[5]/IRQ3	Serial Port Multiplexed. General-Purpose Input and Output Port 1.5/UART, SPI/Programmable Logic Array Input Element 5/External Interrupt Request 3, Active High.
E7	P3.7/PWM_{SYNC}/PLAI[15]	General-Purpose Input and Output Port 3.7/PWM Synchronization/Programmable Logic Array Input Element 15.
E8	XCLKI	Input to the Crystal Oscillator Inverter and Input to the Internal Clock Generator Circuits.
F1	P4.6/PLAO[14]	General-Purpose Input and Output Port 4.6/Programmable Logic Array Output Element 14.
F2	TDI	JTAG Test Port Input, Test Data In. Debug and download access.
F3	DAC0/ADC12	DAC0 Voltage Output/ADC Input 12.
F4	P3.1/$PWM0_L$/PLAI[9]	General-Purpose Input and Output Port 3.1/PWM Phase 0 Low-Side Output/Programmable Logic Array Input Element 9.
F5	P3.3/$PWM1_L$/PLAI[11]	General-Purpose Input and Output Port 3.3/PWM Phase 1 Low-Side Output/Programmable Logic Array Input Element 11.
F6	$\overline{RST}$	Reset Input, Active Low.
F7	P0.7/ECLK/XCLK/SPM8/PLAO[4]	Serial Port Multiplexed. General-Purpose Input and Output Port 0.7/Output for External Clock Signal/Input to the Internal Clock Generator Circuits/UART/Programmable Logic Array Output Element 4.
F8	XCLKO	Output from the Crystal Oscillator Inverter.
G1	BM/P0.0/CMP_{OUT}/PLAI[7]	Multifunction I/O Pin. Boot mode. The ADuC7028 enters UART download mode if BM is low at reset and executes code if BM is pulled high at reset through a 1 kΩ resistor/General-Purpose Input and Output Port 0.0/Voltage Comparator Output/Programmable Logic Array Input Element 7.
G2	P4.7/PLAO[15]	General-Purpose Input and Output Port 4.7/Programmable Logic Array Output Element 15.
G3	TMS	JTAG Test Port Input, Test Mode Select. Debug and download access.
G4	TDO	JTAG Test Port Output, Test Data Out. Debug and download access.
G5	P0.3/TRST/ADC_{BUSY}	General-Purpose Input and Output Port 0.3/JTAG Test Port Input, Test Reset/ADC_{BUSY} Signal Output.
G6	P3.4/$PWM2_H$/PLAI[12]	General-Purpose Input and Output Port 3.4/PWM Phase 2 High-Side Output/Programmable Logic Array Input 12.
G7	P3.5/$PWM2_L$/PLAI[13]	General-Purpose Input and Output Port 3.5/PWM Phase 2 Low-Side Output/Programmable Logic Array Input Element 13.
G8	P2.0/SPM9/PLAO[5]/$\overline{CONV_{START}}$	Serial Port Multiplexed. General-Purpose Input and Output Port 2.0/UART/Programmable Logic Array Output Element 5/Start Conversion Input Signal for ADC.
H1	P0.6/T1/MRST/PLAO[3]	Multifunction Pin, Driven Low After Reset. General-Purpose Output Port 0.6/Timer1 Input/Power-On Reset Output/Programmable Logic Array Output Element 3.
H2	TCK	JTAG Test Port Input, Test Clock. Debug and download access.
H3	IOGND	Ground for GPIO (see Table 78). Typically connected to DGND.
H4	IOV_{DD}	3.3 V Supply for GPIO (see Table 78) and Input of the On-Chip Voltage Regulator.
H5	LV_{DD}	2.6 V Output of the On-Chip Voltage Regulator. This output must be connected to a 0.47 µF capacitor to DGND only.
H6	DGND	Ground for Core Logic.
H7	IRQ0/P0.4/PWM_{TRIP}/PLAO[1]	Multifunction I/O Pin. External Interrupt Request 0, Active High/General-Purpose Input and Output Port 0.4/PWM Trip External Input/Programmable Logic Array Output Element 1.
H8	IRQ1/P0.5/ADC_{BUSY}/PLAO[2]	Multifunction I/O Pin. External Interrupt Request 1, Active High/General-Purpose Input and Output Port 0.5/ADC_{BUSY} Signal Output/Programmable Logic Array Output Element 2.

ADUC7029

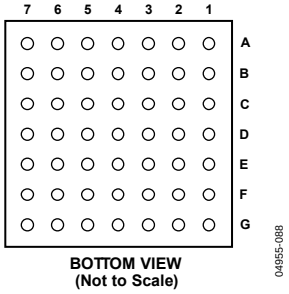


Figure 27. 49-Ball CSP_BGA Pin Configuration (ADuC7029)

Table 15. Pin Function Descriptions (ADuC7029)

Pin No.	Mnemonic	Description
A1	ADC3/CMP1	Single-Ended or Differential Analog Input 3/Comparator Negative Input.
A2	ADC1	Single-Ended or Differential Analog Input 1.
A3	ADC0	Single-Ended or Differential Analog Input 0.
A4	AV_{DD}	3.3 V Analog Power.
A5	V_{REF}	2.5 V Internal Voltage Reference. Must be connected to a 0.47 µF capacitor when using the internal reference.
A6	P1.0/T1/SPM0/PLAI[0]	Serial Port Multiplexed. General-Purpose Input and Output Port 1.0/Timer1 Input/UART, I2C0/ Programmable Logic Array Input Element 0.
A7	P1.1/SPM1/PLAI[1]	Serial Port Multiplexed. General-Purpose Input and Output Port 1.1/UART, I2C0/Programmable Logic Array Input Element 1.
B1	ADC6	Single-Ended or Differential Analog Input 6.
B2	ADC5	Single-Ended or Differential Analog Input 5.
B3	ADC4	Single-Ended or Differential Analog Input 4.
B4	AGND	Analog Ground. Ground reference point for the analog circuitry.
B5	DAC_{REF}	External Voltage Reference for the DACs. Range: DACGND to $DACV_{DD}$.
B6	P1.4/SPM4/PLAI[4]/IRQ2	Serial Port Multiplexed. General-Purpose Input and Output Port 1.4/UART, SPI/Programmable Logic Array Input Element 4/External Interrupt Request 2, Active High.
B7	P1.3/SPM3/PLAI[3]	Serial Port Multiplexed. General-Purpose Input and Output Port 1.3/UART, I2C1/Programmable Logic Array Input Element 3.
C1	GND_{REF}	Ground Voltage Reference for the ADC. For optimal performance, the analog power supply should be separated from IOGND and DGND.
C2	AGND	Analog Ground. Ground reference point for the analog circuitry.
C3	ADC2/CMP0	Single-Ended or Differential Analog Input 2/Comparator Positive Input.
C4	IOGND	Ground for GPIO (see Table 78). Typically connected to DGND.
C5	P1.2/SPM2/PLAI[2]	Serial Port Multiplexed. General-Purpose Input and Output Port 1.2/UART, I2C1/Programmable Logic Array Input Element 2.
C6	P1.6/SPM6/PLAI[6]	Serial Port Multiplexed. General-Purpose Input and Output Port 1.6/UART, SPI/Programmable Logic Array Input Element 6.
C7	P1.5/SPM5/PLAI[5]/IRQ3	Serial Port Multiplexed. General-Purpose Input and Output Port 1.5/UART, SPI/Programmable Logic Array Input Element 5/External Interrupt Request 3, Active High.
D1	DAC0/ADC12	DAC0 Voltage Output/ADC Input 12.
D2	DAC3/ADC15	DAC3 Voltage Output/ADC Input 15.
D3	DAC1/ADC13	DAC1 Voltage Output/ADC Input 13.
D4	$P3.3/PWM1_L$/PLAI[11]	General-Purpose Input and Output Port 3.3/PWM Phase 1 Low-Side Output/Programmable Logic Array Input Element 11.
D5	$P3.4/PWM2_H$/PLAI[12]	General-Purpose Input and Output Port 3.4/PWM Phase 2 High-Side Output/Programmable Logic Array Input 12.
D6	$P3.6/PWM_{TRIP}$/PLAI[14]	General-Purpose Input and Output Port 3.6/PWM Safety Cutoff/Programmable Logic Array Input Element 14.
D7	P1.7/SPM7/PLAO[0]	Serial Port Multiplexed. General-Purpose Input and Output Port 1.7/UART, SPI/Programmable Logic Array Output Element 0.

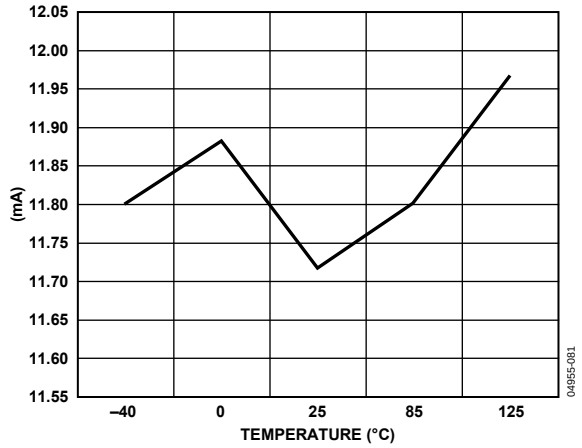


Figure 40. Current Consumption vs. Temperature @ CD = 3

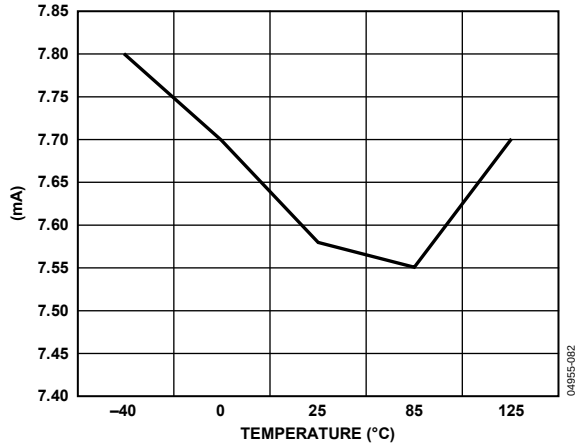


Figure 41. Current Consumption vs. Temperature @ CD = 7

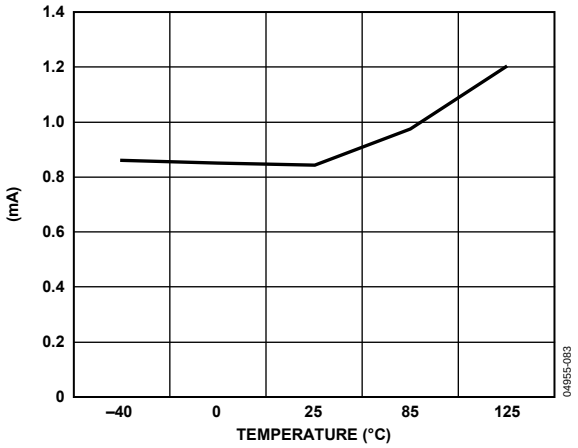


Figure 42. Current Consumption vs. Temperature in Sleep Mode

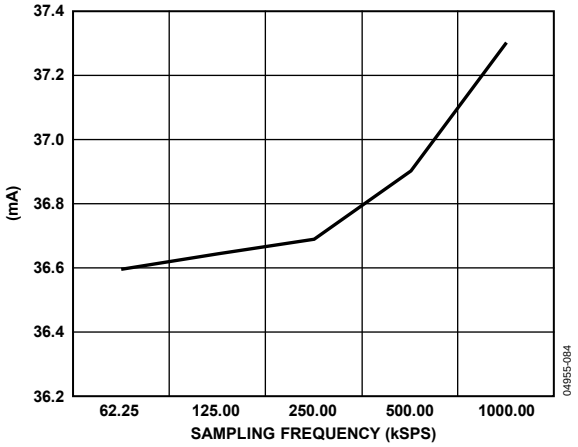


Figure 43. Current Consumption vs. Sampling Frequency

ADC CIRCUIT OVERVIEW

The analog-to-digital converter (ADC) incorporates a fast, multichannel, 12-bit ADC. It can operate from 2.7 V to 3.6 V supplies and is capable of providing a throughput of up to 1 MSPS when the clock source is 41.78 MHz. This block provides the user with a multichannel multiplexer, a differential track-and-hold, an on-chip reference, and an ADC.

The ADC consists of a 12-bit successive approximation converter based around two capacitor DACs. Depending on the input signal configuration, the ADC can operate in one of three modes.

- Fully differential mode, for small and balanced signals
- Single-ended mode, for any single-ended signals
- Pseudo differential mode, for any single-ended signals, taking advantage of the common-mode rejection offered by the pseudo differential input

The converter accepts an analog input range of 0 V to V_{REF} when operating in single-ended or pseudo differential mode. In fully differential mode, the input signal must be balanced around a common-mode voltage (V_{CM}) in the 0 V to AV_{DD} range with a maximum amplitude of 2 V_{REF} (see Figure 48).

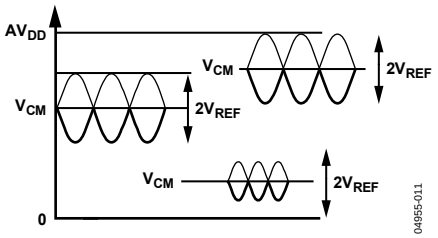


Figure 48. Examples of Balanced Signals in Fully Differential Mode

A high precision, low drift, factory calibrated, 2.5 V reference is provided on-chip. An external reference can also be connected as described in the Band Gap Reference section.

Single or continuous conversion modes can be initiated in the software. An external $\overline{CONV_{START}}$ pin, an output generated from the on-chip PLA, or a Timer0 or Timer1 overflow can also be used to generate a repetitive trigger for ADC conversions.

A voltage output from an on-chip band gap reference proportional to absolute temperature can also be routed through the front-end ADC multiplexer, effectively an additional ADC channel input. This facilitates an internal temperature sensor channel that measures die temperature to an accuracy of ±3°C.

TRANSFER FUNCTION

Pseudo Differential and Single-Ended Modes

In pseudo differential or single-ended mode, the input range is 0 V to V_{REF}. The output coding is straight binary in pseudo differential and single-ended modes with

1 LSB = *FS*/4096, or
2.5 V/4096 = 0.61 mV, or
610 µV when V_{REF} = 2.5 V

The ideal code transitions occur midway between successive integer LSB values (that is, 1/2 LSB, 3/2 LSB, 5/2 LSB, … , FS – 3/2 LSB). The ideal input/output transfer characteristic is shown in Figure 49.

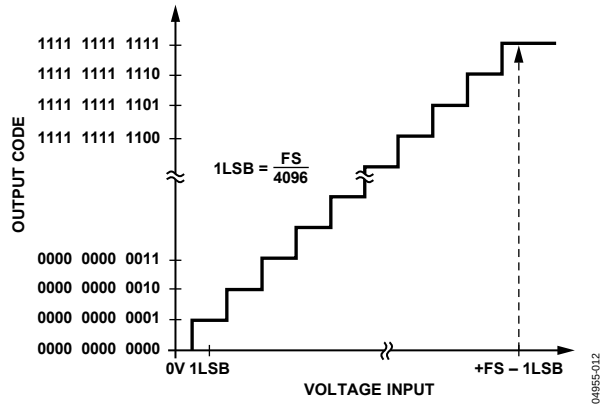


Figure 49. ADC Transfer Function in Pseudo Differential or Single-Ended Mode

Fully Differential Mode

The amplitude of the differential signal is the difference between the signals applied to the V_{IN+} and V_{IN-} input voltage pins (that is, $V_{IN+} - V_{IN-}$). The maximum amplitude of the differential signal is, therefore, $-V_{REF}$ to $+V_{REF}$ p-p (that is, $2 \times V_{REF}$). This is regardless of the common mode (CM). The common mode is the average of the two signals, for example, $(V_{IN+} + V_{IN-})/2$, and is, therefore, the voltage that the two inputs are centered on. This results in the span of each input being CM ± $V_{REF}/2$. This voltage has to be set up externally, and its range varies with V_{REF} (see the Driving the Analog Inputs section).

The output coding is twos complement in fully differential mode with 1 LSB = 2 $V_{REF}/4096$ or 2 × 2.5 V/4096 = 1.22 mV when V_{REF} = 2.5 V. The output result is ±11 bits, but this is shifted by 1 to the right. This allows the result in ADCDAT to be declared as a signed integer when writing C code. The designed code transitions occur midway between successive integer LSB values (that is, 1/2 LSB, 3/2 LSB, 5/2 LSB, … , FS – 3/2 LSB). The ideal input/output transfer characteristic is shown in Figure 50.

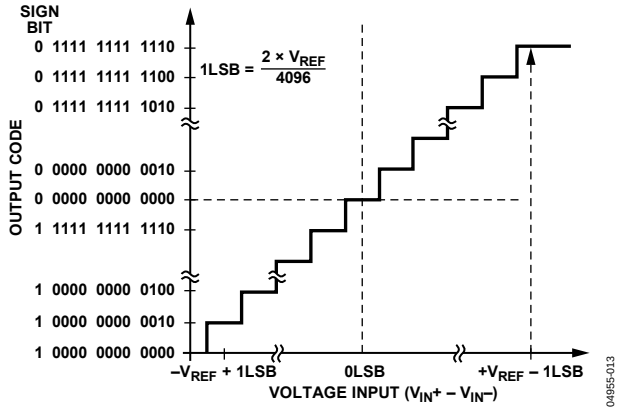


Figure 50. ADC Transfer Function in Differential Mode

Table 28. V_{CM} Ranges

AV_{DD}	V_{REF}	V_{CM} Min	V_{CM} Max	Signal Peak-to-Peak
3.3 V	2.5 V	1.25 V	2.05 V	2.5 V
	2.048 V	1.024 V	2.276 V	2.048 V
	1.25 V	0.75 V	2.55 V	1.25 V
3.0 V	2.5 V	1.25 V	1.75 V	2.5 V
	2.048 V	1.024 V	1.976 V	2.048 V
	1.25 V	0.75 V	2.25 V	1.25 V

CALIBRATION

By default, the factory-set values written to the ADC offset (ADCOF) and gain coefficient registers (ADCGN) yield optimum performance in terms of end-point errors and linearity for standalone operation of the part (see the Specifications section). If system calibration is required, it is possible to modify the default offset and gain coefficients to improve end-point errors, but note that any modification to the factory-set ADCOF and ADCGN values can degrade ADC linearity performance.

For system offset error correction, the ADC channel input stage must be tied to AGND. A continuous software ADC conversion loop must be implemented by modifying the value in ADCOF until the ADC result (ADCDAT) reads Code 0 to Code 1. If the ADCDAT value is greater than 1, ADCOF should be decremented until ADCDAT reads 0 to 1. Offset error correction is done digitally and has a resolution of 0.25 LSB and a range of ±3.125% of V_{REF}.

For system gain error correction, the ADC channel input stage must be tied to V_{REF}. A continuous software ADC conversion loop must be implemented to modify the value in ADCGN until the ADC result (ADCDAT) reads Code 4094 to Code 4095. If the ADCDAT value is less than 4094, ADCGN should be incremented until ADCDAT reads 4094 to 4095. Similar to the offset calibration, the gain calibration resolution is 0.25 LSB with a range of ±3% of V_{REF}.

TEMPERATURE SENSOR

The ADuC7019/20/21/22/24/25/26/27/28/29 provide voltage output from on-chip band gap references proportional to absolute temperature. This voltage output can also be routed through the front-end ADC multiplexer (effectively an additional ADC channel input) facilitating an internal temperature sensor channel, measuring die temperature to an accuracy of ±3°C.

The following is an example routine showing how to use the internal temperature sensor:

```
int main(void)
{
float a = 0;
      short b;
      ADCCON = 0x20;    // power-on the ADC
      delay(2000);
      ADCCP = 0x10;  // Select Temperature
Sensor as an // input to the ADC
      REFCON = 0x01; // connect internal 2.5V
reference // to Vref pin
      ADCCON = 0xE4; // continuous conversion
      while(1)
      {
              while (!ADCSTA){};
      // wait for end of conversion
              b = (ADCDAT >> 16);
      // To calculate temperature in °C, use
the formula:
              a = 0x525 - b;
      // ((Temperature = 0x525 - Sensor
Voltage) / 1.3)
              a /= 1.3;
              b = floor(a);
              printf("Temperature: %d
oC\n",b);
      }
      return 0;
}
```

BAND GAP REFERENCE

Each ADuC7019/20/21/22/24/25/26/27/28/29 provides an on-chip band gap reference of 2.5 V, which can be used for the ADC and DAC. This internal reference also appears on the V_{REF} pin. When using the internal reference, a 0.47 µF capacitor must be connected from the external V_{REF} pin to AGND to ensure stability and fast response during ADC conversions. This reference can also be connected to an external pin (V_{REF}) and used as a reference for other circuits in the system. An external buffer is required because of the low drive capability of the V_{REF} output. A programmable option also allows an external reference input on the V_{REF} pin. Note that it is not possible to disable the internal reference. Therefore, the external reference source must be capable of overdriving the internal reference source.

Table 29. REFCON Register

Name	Address	Default Value	Access
REFCON	0xFFFF048C	0x00	R/W

The band gap reference interface consists of an 8-bit MMR REFCON, described in Table 30.

Table 30. REFCON MMR Bit Designations

Bit	Description
7:1	Reserved.
0	Internal reference output enable. Set by user to connect the internal 2.5 V reference to the V_{REF} pin. The reference can be used for an external component but must be buffered. Cleared by user to disconnect the reference from the V_{REF} pin.

NONVOLATILE FLASH/EE MEMORY

The ADuC7019/20/21/22/24/25/26/27/28/29 incorporate Flash/EE memory technology on-chip to provide the user with nonvolatile, in-circuit reprogrammable memory space.

Like EEPROM, flash memory can be programmed in-system at a byte level, although it must first be erased. The erase is performed in page blocks. As a result, flash memory is often and more correctly referred to as Flash/EE memory.

Overall, Flash/EE memory represents a step closer to the ideal memory device that includes nonvolatility, in-circuit programmability, high density, and low cost. Incorporated in the ADuC7019/20/21/22/24/25/26/27/28/29, Flash/EE memory technology allows the user to update program code space in-circuit, without the need to replace one-time programmable (OTP) devices at remote operating nodes.

Each part contains a 64 kB array of Flash/EE memory. The lower 62 kB is available to the user and the upper 2 kB contain permanently embedded firmware, allowing in-circuit serial download. These 2 kB of embedded firmware also contain a power-on configuration routine that downloads factory-calibrated coefficients to the various calibrated peripherals (such as ADC, temperature sensor, and band gap references). This 2 kB embedded firmware is hidden from user code.

Flash/EE Memory Reliability

The Flash/EE memory arrays on the parts are fully qualified for two key Flash/EE memory characteristics: Flash/EE memory cycling endurance and Flash/EE memory data retention.

Endurance quantifies the ability of the Flash/EE memory to be cycled through many program, read, and erase cycles. A single endurance cycle is composed of four independent, sequential events, defined as

1. Initial page erase sequence
2. Read/verify sequence (single Flash/EE)
3. Byte program sequence memory
4. Second read/verify sequence (endurance cycle)

In reliability qualification, every half word (16-bit wide) location of the three pages (top, middle, and bottom) in the Flash/EE memory is cycled 10,000 times from 0x0000 to 0xFFFF. As indicated in Table 1, the Flash/EE memory endurance qualification is carried out in accordance with JEDEC Retention Lifetime Specification A117 over the industrial temperature range of −40° to +125°C. The results allow the specification of a minimum endurance figure over a supply temperature of 10,000 cycles.

Retention quantifies the ability of the Flash/EE memory to retain its programmed data over time. Again, the parts are qualified in accordance with the formal JEDEC Retention Lifetime Specification (A117) at a specific junction temperature (T_J = 85°C). As part of this qualification procedure, the Flash/EE memory is cycled to its specified endurance limit, described in Table 1, before data retention is characterized. This means that the Flash/EE memory is guaranteed to retain its data for its fully specified retention lifetime every time the Flash/EE memory is reprogrammed. In addition, note that retention lifetime, based on an activation energy of 0.6 eV, derates with T_J as shown in Figure 61.

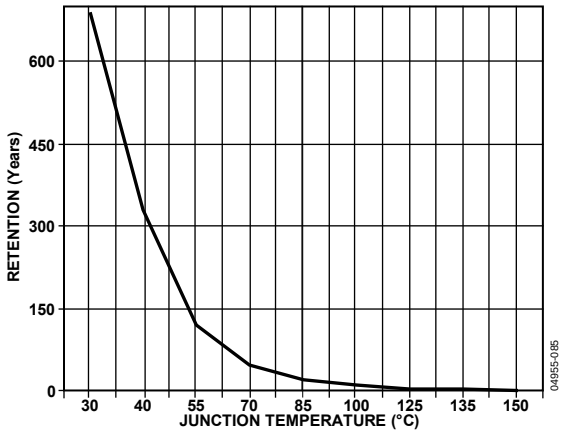


Figure 61. Flash/EE Memory Data Retention

PROGRAMMING

The 62 kB of Flash/EE memory can be programmed in-circuit, using the serial download mode or the provided JTAG mode.

Serial Downloading (In-Circuit Programming)

The ADuC7019/20/21/22/24/25/26/27/28/29 facilitate code download via the standard UART serial port or via the I²C port. The parts enter serial download mode after a reset or power cycle if the BM pin is pulled low through an external 1 kΩ resistor. After a part is in serial download mode, the user can download code to the full 62 kB of Flash/EE memory while the device is in-circuit in its target application hardware. An executable PC serial download is provided as part of the development system for serial downloading via the UART. The AN-806 Application Note describes the protocol for serial downloading via the I²C.

JTAG Access

The JTAG protocol uses the on-chip JTAG interface to facilitate code download and debug.

Table 35. FEECON Register

Name	Address	Default Value	Access
FEECON	0xFFFFF808	0x07	R/W

FEECON is an 8-bit command register. The commands are described in Table 36.

Table 36. Command Codes in FEECON

Code	Command	Description
0x00[1]	Null	Idle state.
0x01[1]	Single read	Load FEEDAT with the 16-bit data. Indexed by FEEADR.
0x02[1]	Single write	Write FEEDAT at the address pointed to by FEEADR. This operation takes 50 μs.
0x03[1]	Erase/write	Erase the page indexed by FEEADR and write FEEDAT at the location pointed by FEEADR. This operation takes approximately 24 ms.
0x04[1]	Single verify	Compare the contents of the location pointed by FEEADR to the data in FEEDAT. The result of the comparison is returned in FEESTA, Bit 1.
0x05[1]	Single erase	Erase the page indexed by FEEADR.
0x06[1]	Mass erase	Erase 62 kB of user space. The 2 kB of kernel are protected. This operation takes 2.48 sec. To prevent accidental execution, a command sequence is required to execute this instruction. See the Command Sequence for Executing a Mass Erase section.
0x07	Reserved	Reserved.
0x08	Reserved	Reserved.
0x09	Reserved	Reserved.
0x0A	Reserved	Reserved.
0x0B	Signature	Give a signature of the 64 kB of Flash/EE in the 24-bit FEESIGN MMR. This operation takes 32,778 clock cycles.
0x0C	Protect	This command can run only once. The value of FEEPRO is saved and removed only with a mass erase (0x06) of the key.
0x0D	Reserved	Reserved.
0x0E	Reserved	Reserved.
0x0F	Ping	No operation; interrupt generated.

[1] The FEECON register always reads 0x07 immediately after execution of any of these commands.

Table 37. FEEDAT Register

Name	Address	Default Value	Access
FEEDAT	0xFFFFF80C	0xXXXX[1]	R/W

[1] X = 0, 1, 2, or 3.

FEEDAT is a 16-bit data register.

Table 38. FEEADR Register

Name	Address	Default Value	Access
FEEADR	0xFFFFF810	0x0000	R/W

FEEADR is another 16-bit address register.

Table 39. FEESIGN Register

Name	Address	Default Value	Access
FEESIGN	0xFFFFF818	0xFFFFFF	R

FEESIGN is a 24-bit code signature.

Table 40. FEEPRO Register

Name	Address	Default Value	Access
FEEPRO	0xFFFFF81C	0x00000000	R/W

FEEPRO MMR provides protection following a subsequent reset of the MMR. It requires a software key (see Table 42).

Table 41. FEEHIDE Register

Name	Address	Default Value	Access
FEEHIDE	0xFFFFF820	0xFFFFFFFF	R/W

FEEHIDE MMR provides immediate protection. It does not require any software key. Note that the protection settings in FEEHIDE are cleared by a reset (see Table 42).

Table 42. FEEPRO and FEEHIDE MMR Bit Designations

Bit	Description
31	Read protection. Cleared by user to protect all code. Set by user to allow reading the code.
30:0	Write protection for Page 123 to Page 120, Page 119 to Page 116, and Page 0 to Page 3. Cleared by user to protect the pages from writing. Set by user to allow writing the pages.

Command Sequence for Executing a Mass Erase

```
FEEDAT=0x3CFF;
FEEADR = 0xFFC3;
FEEMOD= FEEMOD|0x8;    //Erase key enable
FEECON=0x06;           //Mass erase command
```

EXECUTION TIME FROM SRAM AND FLASH/EE

Execution from SRAM

Fetching instructions from SRAM takes one clock cycle; the access time of the SRAM is 2 ns, and a clock cycle is 22 ns minimum. However, if the instruction involves reading or writing data to memory, one extra cycle must be added if the data is in SRAM (or three cycles if the data is in Flash/EE): one cycle to execute the instruction, and two cycles to get the 32-bit data from Flash/EE. A control flow instruction (a branch instruction, for example) takes one cycle to fetch but also takes two cycles to fill the pipeline with the new instructions.

Execution from Flash/EE

Because the Flash/EE width is 16 bits and access time for 16-bit words is 22 ns, execution from Flash/EE cannot be done in one cycle (as can be done from SRAM when the CD Bit = 0). Also, some dead times are needed before accessing data for any value of the CD bit.

In ARM mode, where instructions are 32 bits, two cycles are needed to fetch any instruction when CD = 0. In thumb mode, where instructions are 16 bits, one cycle is needed to fetch any instruction.

Timing is identical in both modes when executing instructions that involve using the Flash/EE for data memory. If the instruction to be executed is a control flow instruction, an extra cycle is needed to decode the new address of the program counter, and then four cycles are needed to fill the pipeline. A data-processing instruction involving only the core register does not require any extra clock cycles. However, if it involves data in Flash/EE, an extra clock cycle is needed to decode the address of the data, and two cycles are needed to get the 32-bit data from Flash/EE. An extra cycle must also be added before fetching another instruction. Data transfer instructions are more complex and are summarized in Table 43.

Table 43. Execution Cycles in ARM/Thumb Mode

Instructions	Fetch Cycles	Dead Time	Data Access	Dead Time
LD[1]	2/1	1	2	1
LDH	2/1	1	1	1
LDM/PUSH	2/1	N[2]	2 × N[2]	N[1]
STR[1]	2/1	1	2 × 20 ns	1
STRH	2/1	1	20 ns	1
STRM/POP	2/1	N[1]	2 × N × 20 ns[1]	N[1]

[1] The SWAP instruction combines an LD and STR instruction with only one fetch, giving a total of eight cycles + 40 ns.
[2] N is the amount of data to load or store in the multiple load/store instruction (1 < N ≤ 16).

RESET AND REMAP

The ARM exception vectors are all situated at the bottom of the memory array, from Address 0x00000000 to Address 0x00000020, as shown in Figure 62.

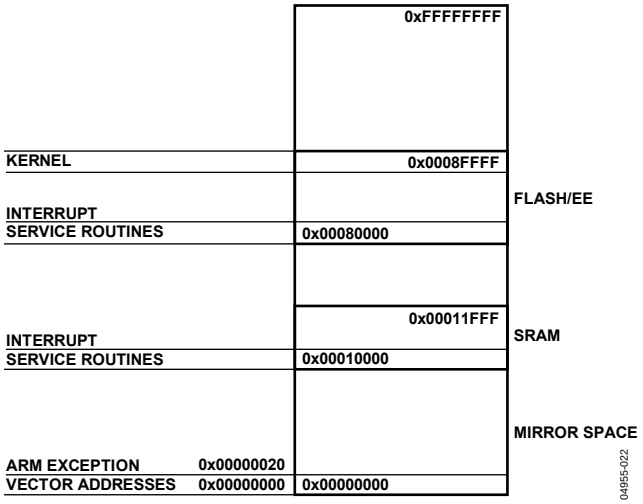


Figure 62. Remap for Exception Execution

By default, and after any reset, the Flash/EE is mirrored at the bottom of the memory array. The remap function allows the programmer to mirror the SRAM at the bottom of the memory array, which facilitates execution of exception routines from SRAM instead of from Flash/EE. This means exceptions are executed twice as fast, being executed in 32-bit ARM mode with 32-bit wide SRAM instead of 16-bit wide Flash/EE memory.

Remap Operation

When a reset occurs on the ADuC7019/20/21/22/24/25/26/27/28/29, execution automatically starts in the factory-programmed, internal configuration code. This kernel is hidden and cannot be accessed by user code. If the part is in normal mode (the BM pin is high), it executes the power-on configuration routine of the kernel and then jumps to the reset vector address, 0x00000000, to execute the user's reset exception routine.

Because the Flash/EE is mirrored at the bottom of the memory array at reset, the reset interrupt routine must always be written in Flash/EE.

The remap is done from Flash/EE by setting Bit 0 of the REMAP register. Caution must be taken to execute this command from Flash/EE, above Address 0x00080020, and not from the bottom of the array because this is replaced by the SRAM.

This operation is reversible. The Flash/EE can be remapped at Address 0x00000000 by clearing Bit 0 of the REMAP MMR. Caution must again be taken to execute the remap function from outside the mirrored area. Any type of reset remaps the Flash/EE memory at the bottom of the array.

Input offset voltage (V_{OS}) is the difference between the center of the hysteresis range and the ground level. This can either be positive or negative. The hysteresis voltage (V_H) is one-half the width of the hysteresis range.

Comparator Interface

The comparator interface consists of a 16-bit MMR, CMPCON, which is described in Table 56.

Table 55. CMPCON Register

Name	Address	Default Value	Access
CMPCON	0xFFFF0444	0x0000	R/W

Table 56. CMPCON MMR Bit Descriptions

Bit	Name	Value	Description
15:11			Reserved.
10	CMPEN		Comparator enable bit. Set by user to enable the comparator. Cleared by user to disable the comparator.
9:8	CMPIN		Comparator negative input select bits.
		00	$AV_{DD}/2$.
		01	ADC3 input.
		10	DAC0 output.
		11	Reserved.
7:6	CMPOC		Comparator output configuration bits.
		00	Reserved.
		01	Reserved.
		10	Output on CMP_{OUT}.
		11	IRQ.
5	CMPOL		Comparator output logic state bit. When low, the comparator output is high if the positive input (CMP0) is above the negative input (CMP1). When high, the comparator output is high if the positive input is below the negative input.
4:3	CMPRES		Response time.
		00	5 µs response time is typical for large signals (2.5 V differential). 17 µs response time is typical for small signals (0.65 mV differential).
		11	3 µs typical.
		01/10	Reserved.
2	CMPHYST		Comparator hysteresis bit. Set by user to have a hysteresis of about 7.5 mV. Cleared by user to have no hysteresis.
1	CMPORI		Comparator output rising edge interrupt. Set automatically when a rising edge occurs on the monitored voltage (CMP0). Cleared by user by writing a 1 to this bit.
0	CMPOFI		Comparator output falling edge interrupt. Set automatically when a falling edge occurs on the monitored voltage (CMP0). Cleared by user.

OSCILLATOR AND PLL—POWER CONTROL

Clocking System

Each ADuC7019/20/21/22/24/25/26/27/28/29 integrates a 32.768 kHz ±3% oscillator, a clock divider, and a PLL. The PLL locks onto a multiple (1275) of the internal oscillator or an external 32.768 kHz crystal to provide a stable 41.78 MHz clock (UCLK) for the system. To allow power saving, the core can operate at this frequency, or at binary submultiples of it. The actual core operating frequency, $UCLK/2^{CD}$, is refered to as HCLK. The default core clock is the PLL clock divided by 8 (CD = 3) or 5.22 MHz. The core clock frequency can also come from an external clock on the ECLK pin as described in Figure 67. The core clock can be outputted on ECLK when using an internal oscillator or external crystal.

Note that when the ECLK pin is used to output the core clock, the output signal is not buffered and is not suitable for use as a clock source to an external device without an external buffer.

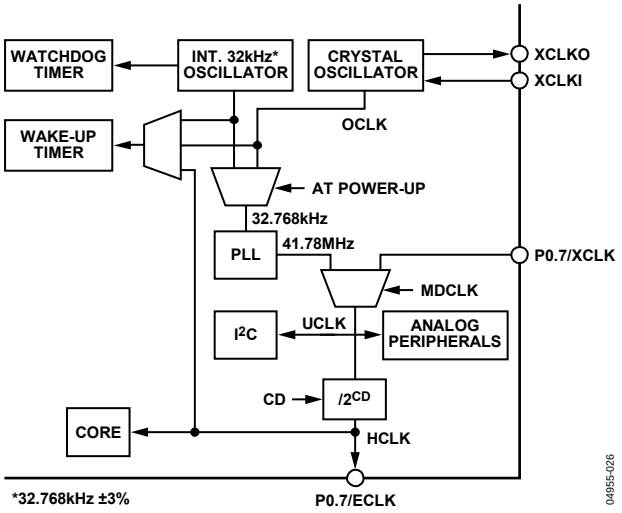


Figure 67. Clocking System

The selection of the clock source is in the PLLCON register. By default, the part uses the internal oscillator feeding the PLL.

External Crystal Selection

To switch to an external crystal, the user must do the following:

1. Enable the Timer2 interrupt and configure it for a timeout period of >120 µs.
2. Follow the write sequence to the PLLCON register, setting the MDCLK bits to 01 and clearing the OSEL bit.
3. Force the part into NAP mode by following the correct write sequence to the POWCON register.

   When the part is interrupted from NAP mode by the Timer2 interrupt source, the clock source has switched to the external clock.

MMRs and Keys

The operating mode, clocking mode, and programmable clock divider are controlled via two MMRs: PLLCON (see Table 61) and POWCON (see Table 64). PLLCON controls the operating mode of the clock system, whereas POWCON controls the core clock frequency and the power-down mode.

To prevent accidental programming, a certain sequence (see Table 65) must be followed to write to the PLLCON and POWCON registers.

Table 59. PLLKEYx Registers

Name	Address	Default Value	Access
PLLKEY1	0xFFFF0410	0x0000	W
PLLKEY2	0xFFFF0418	0x0000	W

Table 60. PLLCON Register

Name	Address	Default Value	Access
PLLCON	0xFFFF0414	0x21	R/W

Table 61. PLLCON MMR Bit Designations

Bit	Name	Value	Description
7:6			Reserved.
5	OSEL		32 kHz PLL input selection. Set by user to select the internal 32 kHz oscillator. Set by default. Cleared by user to select the external 32 kHz crystal.
4:2			Reserved.
1:0	MDCLK		Clocking modes.
		00	Reserved.
		01	PLL. Default configuration.
		10	Reserved.
		11	External clock on the P0.7 pin.

Table 62. POWKEYx Registers

Name	Address	Default Value	Access
POWKEY1	0xFFFF0404	0x0000	W
POWKEY2	0xFFFF040C	0x0000	W

Table 63. POWCON Register

Name	Address	Default Value	Access
POWCON	0xFFFF0408	0x0003	R/W

Table 64. POWCON MMR Bit Designations

Bit	Name	Value	Description
7			Reserved.
6:4	PC		Operating modes.
		000	Active mode.
		001	Pause mode.
		010	Nap.
		011	Sleep mode. IRQ0 to IRQ3 and Timer2 can wake up the part.
		100	Stop mode. IRQ0 to IRQ3 can wake up the part.
		Others	Reserved.
3			Reserved.
2:0	CD		CPU clock divider bits.
		000	41.78 MHz.
		001	20.89 MHz.
		010	10.44 MHz.
		011	5.22 MHz.
		100	2.61 MHz.
		101	1.31 MHz.
		110	653 kHz.
		111	326 kHz.

Table 65. PLLCON and POWCON Write Sequence

PLLCON	POWCON
PLLKEY1 = 0xAA	POWKEY1 = 0x01
PLLCON = 0x01	POWCON = user value
PLLKEY2 = 0x55	POWKEY2 = 0xF4

Table 108. COMSTA1 Register

Name	Address	Default Value	Access
COMSTA1	0xFFFF0718	0x00	R

COMSTA1 is a modem status register.

Table 109. COMSTA1 MMR Bit Descriptions

Bit	Name	Description
7	DCD	Data carrier detect.
6	RI	Ring indicator.
5	DSR	Data set ready.
4	CTS	Clear to send.
3	DDCD	Delta DCD. Set automatically if DCD changed state since last COMSTA1 read. Cleared automatically by reading COMSTA1.
2	TERI	Trailing edge RI. Set if RI changed from 0 to 1 since COMSTA1 was last read. Cleared automatically by reading COMSTA1.
1	DDSR	Delta DSR. Set automatically if DSR changed state since COMSTA1 was last read. Cleared automatically by reading COMSTA1.
0	DCTS	Delta CTS. Set automatically if CTS changed state since COMSTA1 was last read. Cleared automatically by reading COMSTA1.

Table 110. COMSCR Register

Name	Address	Default Value	Access
COMSCR	0xFFFF071C	0x00	R/W

COMSCR is an 8-bit scratch register used for temporary storage. It is also used in network addressable UART mode.

Table 111. COMDIV2 Register

Name	Address	Default Value	Access
COMDIV2	0xFFFF072C	0x0000	R/W

COMDIV2 is a 16-bit fractional baud divide register.

Table 112. COMDIV2 MMR Bit Descriptions

Bit	Name	Description
15	FBEN	Fractional baud rate generator enable bit. Set by user to enable the fractional baud rate generator. Cleared by user to generate baud rate using the standard 450 UART baud rate generator.
14:13		Reserved.
12:11	FBM[1:0]	M if FBM = 0, M = 4 (see the Fractional Divider section).
10:0	FBN[10:0]	N (see the Fractional Divider section).

Network Addressable UART Mode

This mode connects the MicroConverter to a 256-node serial network, either as a hardware single master or via software in a multimaster network. Bit 7 (ENAM) of the COMIEN1 register must be set to enable UART in network addressable mode (see Table 114). Note that there is no parity check in this mode.

Network Addressable UART Register Definitions

Four additional registers, COMIEN0, COMIEN1, COMIID1, and COMADR are used in network addressable UART mode only.

In network address mode, the least significant bit of the COMIEN1 register is the transmitted network address control bit. If set to 1, the device is transmitting an address. If cleared to 0, the device is transmitting data. For example, the following master-based code transmits the slave's address followed by the data:

```
  COMIEN1  = 0xE7;       //Setting ENAM,
E9BT, E9BR, ETD, NABP
  COMTX = 0xA0;  // Slave address is 0xA0
  while(!(0x020==(COMSTA0 & 0x020))){} //
wait for adr tx to finish.
  COMIEN1  = 0xE6;       //  Clear NAB bit
to indicate Data is coming
   COMTX = 0x55; // Tx data to slave: 0x55
```

Table 113. COMIEN1 Register

Name	Address	Default Value	Access
COMIEN1	0xFFFF0720	0x04	R/W

COMIEN1 is an 8-bit network enable register.

Table 114. COMIEN1 MMR Bit Descriptions

Bit	Name	Description
7	ENAM	Network address mode enable bit. Set by user to enable network address mode. Cleared by user to disable network address mode.
6	E9BT	9-bit transmit enable bit. Set by user to enable 9-bit transmit. ENAM must be set. Cleared by user to disable 9-bit transmit.
5	E9BR	9-bit receive enable bit. Set by user to enable 9-bit receive. ENAM must be set. Cleared by user to disable 9-bit receive.
4	ENI	Network interrupt enable bit.
3	E9BD	Word length. Set for 9-bit data. E9BT has to be cleared. Cleared for 8-bit data.
2	ETD	Transmitter pin driver enable bit. Set by user to enable SOUT pin as an output in slave mode or multimaster mode. Cleared by user; SOUT is three-state.
1	NABP	Network address bit. Interrupt polarity bit.
0	NAB	Network address bit (if NABP = 1). Set by user to transmit the slave address. Cleared by user to transmit data.

Table 115. COMIID1 Register

Name	Address	Default Value	Access
COMIID1	0xFFFF0724	0x01	R

COMIID1 is an 8-bit network interrupt register. Bit 7 to Bit 4 are reserved (see Table 116).

Table 137. I2CxALT Registers

Name	Address	Default Value	Access
I2C0ALT	0xFFFF0828	0x00	R/W
I2C1ALT	0xFFFF0928	0x00	R/W

I2CxALT are hardware general call ID registers used in slave mode.

Table 138. I2CxCFG Registers

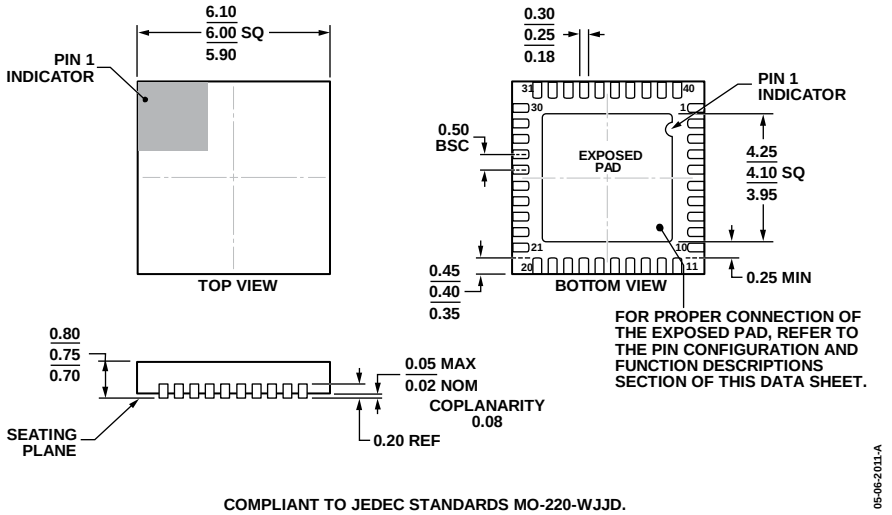
Name	Address	Default Value	Access
I2C0CFG	0xFFFF082C	0x00	R/W
I2C1CFG	0xFFFF092C	0x00	R/W

I2CxCFG are configuration registers.

Table 139. I2C0CFG MMR Bit Descriptions

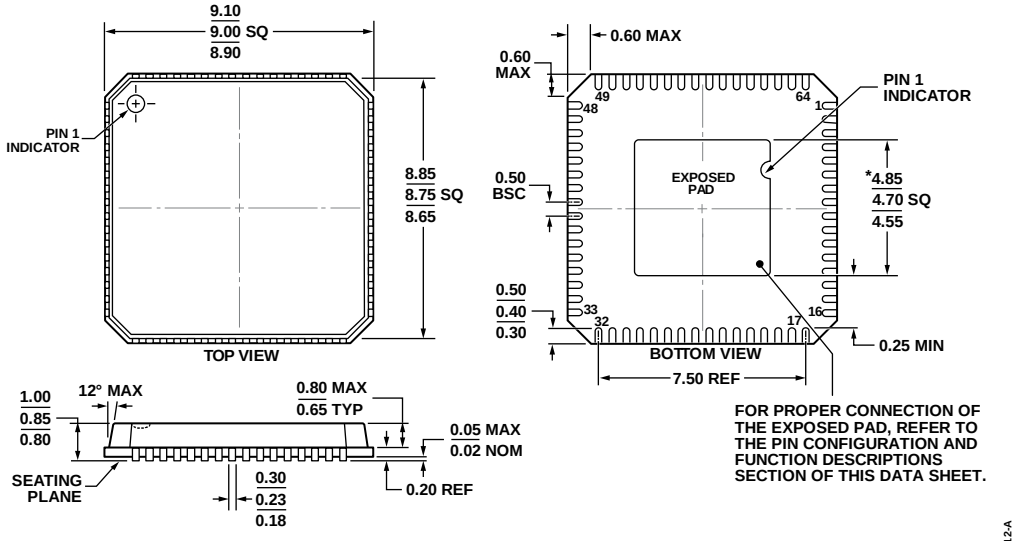
Bit	Description
31:5	Reserved. These bits should be written by the user as 0.
14	Enable stop interrupt. Set by the user to generate an interrupt upon receiving a stop condition and after receiving a valid start condition and matching address. Cleared by the user to disable the generation of an interrupt upon receiving a stop condition.
13	Reserved.
12	Reserved.
11	Enable stretch SCL (holds SCL low). Set by the user to stretch the SCL line. Cleared by the user to disable stretching of the SCL line.
10	Reserved.
9	Slave Tx FIFO request interrupt enable. Set by the user to disable the slave Tx FIFO request interrupt. Cleared by the user to generate an interrupt request just after the negative edge of the clock for the R/W bit. This allows the user to input data into the slave Tx FIFO if it is empty. At 400 ksps and the core clock running at 41.78 MHz, the user has 45 clock cycles to take appropriate action, taking interrupt latency into account.
8	General call status bit clear. Set by the user to clear the general call status bits. Cleared automatically by hardware after the general call status bits are cleared.
7	Master serial clock enable bit. Set by user to enable generation of the serial clock in master mode. Cleared by user to disable serial clock in master mode.
6	Loopback enable bit. Set by user to internally connect the transition to the reception to test user software. Cleared by user to operate in normal mode.
5	Start backoff disable bit. Set by user in multimaster mode. If losing arbitration, the master immediately tries to retransmit. Cleared by user to enable start backoff. After losing arbitration, the master waits before trying to retransmit.
4	Hardware general call enable. When this bit and Bit 3 are set and have received a general call (Address 0x00) and a data byte, the device checks the contents of I2C0ALT against the receive register. If the contents match, the device has received a hardware general call. This is used if a device needs urgent attention from a master device without knowing which master it needs to turn to. This is a "to whom it may concern" call. The ADuC7019/20/21/22/24/25/26/27/28/29 watch for these addresses. The device that requires attention embeds its own address into the message. All masters listen, and the one that can handle the device contacts its slave and acts appropriately. The LSB of the I2C0ALT register should always be written to 1, as indicated in *The I²C-Bus Specification*, January 2000, from NXP.
3	General call enable bit. This bit is set by the user to enable the slave device to acknowledge (ACK) an I²C general call, Address 0x00 (write). The device then recognizes a data bit. If it receives a 0x06 (reset and write programmable part of slave address by hardware) as the data byte, the I²C interface resets as as indicated in *The I²C-Bus Specification,* January 2000, from NXP. This command can be used to reset an entire I²C system. The general call interrupt status bit sets on any general call. The user must take corrective action by setting up the I²C interface after a reset. If it receives a 0x04 (write programmable part of slave address by hardware) as the data byte, the general call interrupt status bit sets on any general call. The user must take corrective action by reprogramming the device address.
2	Reserved.
1	Master enable bit. Set by user to enable the master I²C channel. Cleared by user to disable the master I²C channel.
0	Slave enable bit. Set by user to enable the slave I²C channel. A slave transfer sequence is monitored for the device address in I2C0ID0, I2C0ID1, I2C0ID2, and I2C0ID3. At 400 kSPs, the core clock should run at 41.78 MHz because the interrupt latency could be up to 45 clock cycles alone. After the I²C read bit, the user has 0.5 of an I²C clock cycle to load the Tx FIFO. AT 400 kSPS, this is 1.26 µs, the interrupt latency.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WJJD.

Figure 96. 40-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
6 × 6 mm Body, Very Very Thin Quad
(CP-40-9)
Dimensions shown in millimeters



*COMPLIANT TO JEDEC STANDARDS MO-220-VMMD-4
EXCEPT FOR EXPOSED PAD DIMENSION

Figure 97. 64-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
9 mm × 9 mm Body, Very Thin Quad
(CP-64-1)
Dimensions shown in millimeters

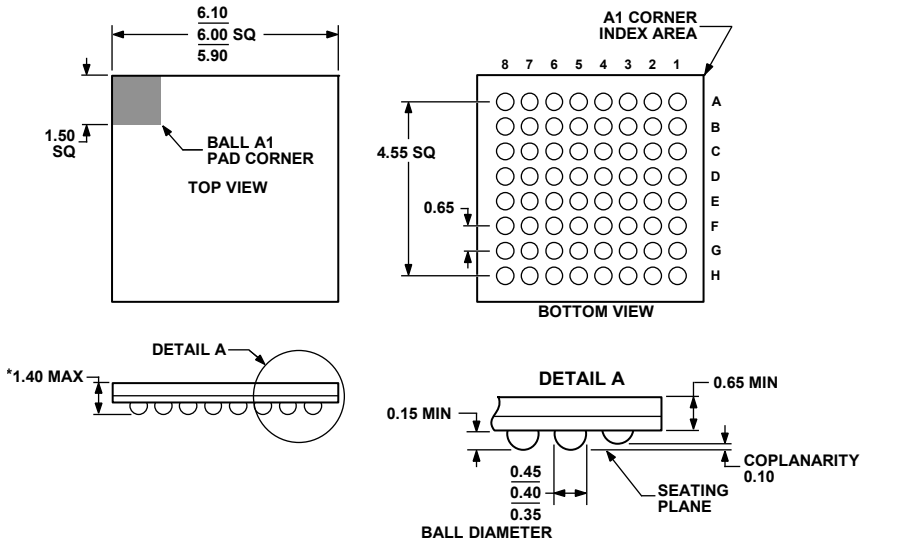


Figure 100. 64-Ball Chip Scale Package Ball Grid Array [CSP_BGA]
(BC-64-4)
Dimensions shown in millimeters

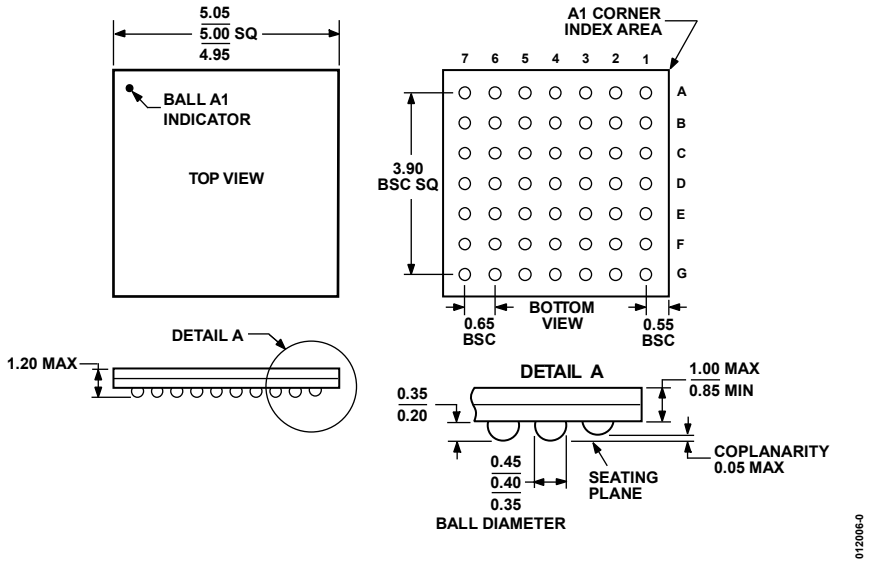


Figure 101. 49-Ball Chip Scale Package Ball Grid Array [CSP_BGA]
(BC-49-1)
Dimensions shown in millimeters