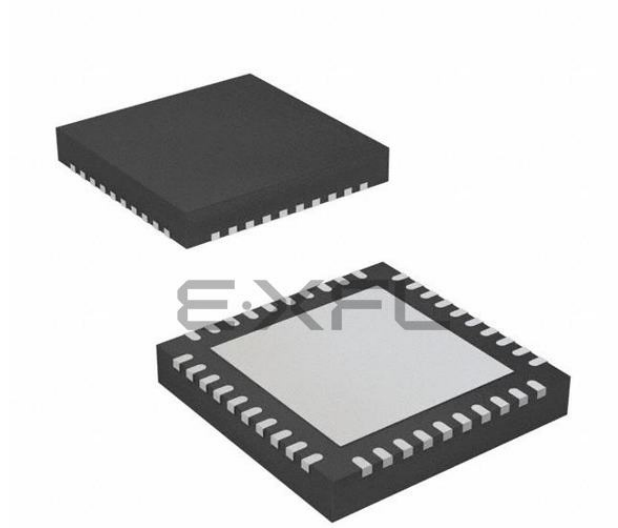

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	44MHz
Connectivity	EBI/EMI, I²C, SPI, UART/USART
Peripherals	PLA, PWM, PSM, Temp Sensor, WDT
Number of I/O	13
Program Memory Size	62KB (31K x16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 32
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	40-VFQFN Exposed Pad, CSP
Supplier Device Package	40-LFCSP-VQ (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/aduc7022bcpz62

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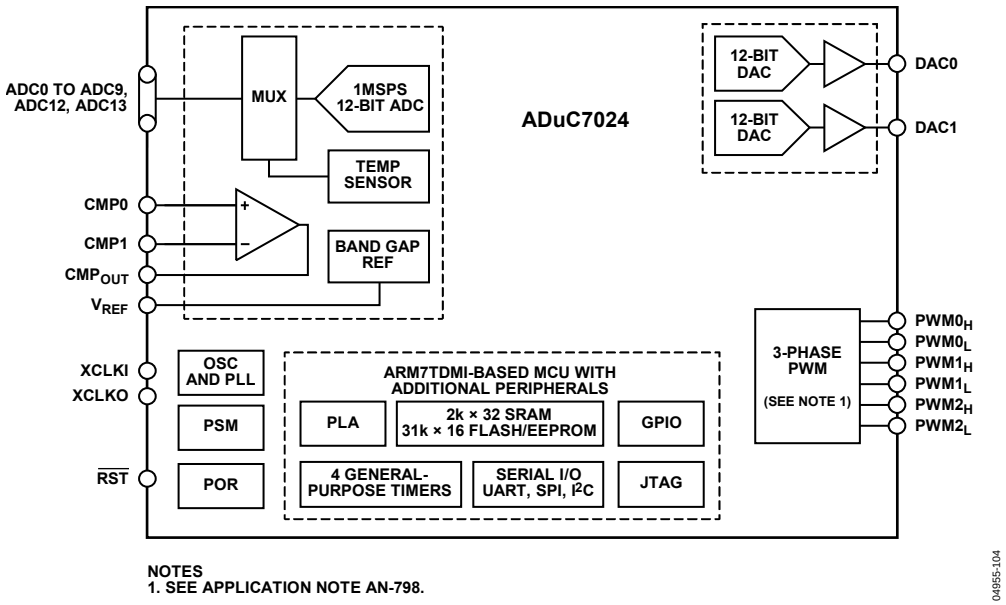

Figure 5.

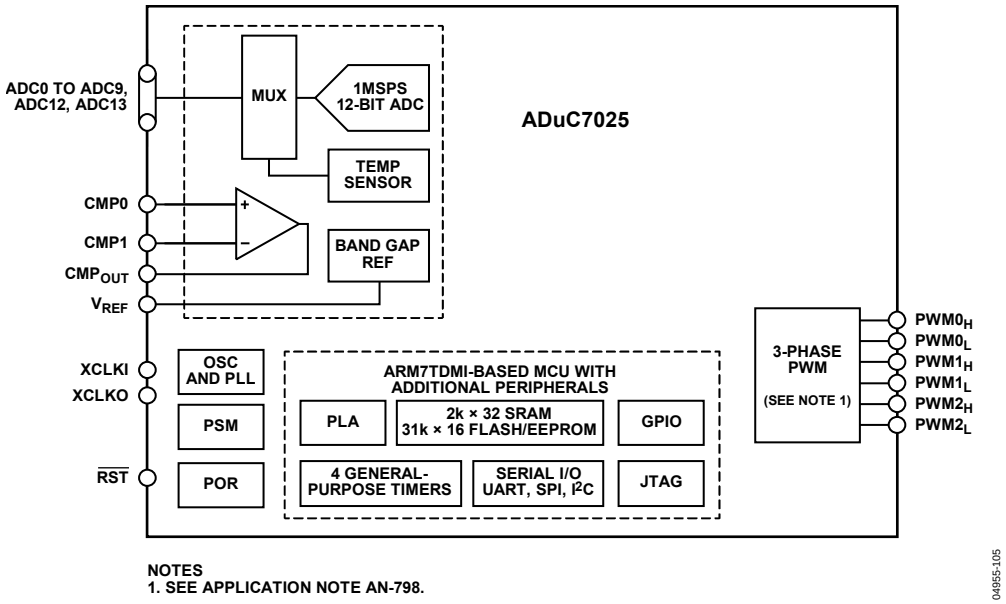

Figure 6.

DETAILED BLOCK DIAGRAM

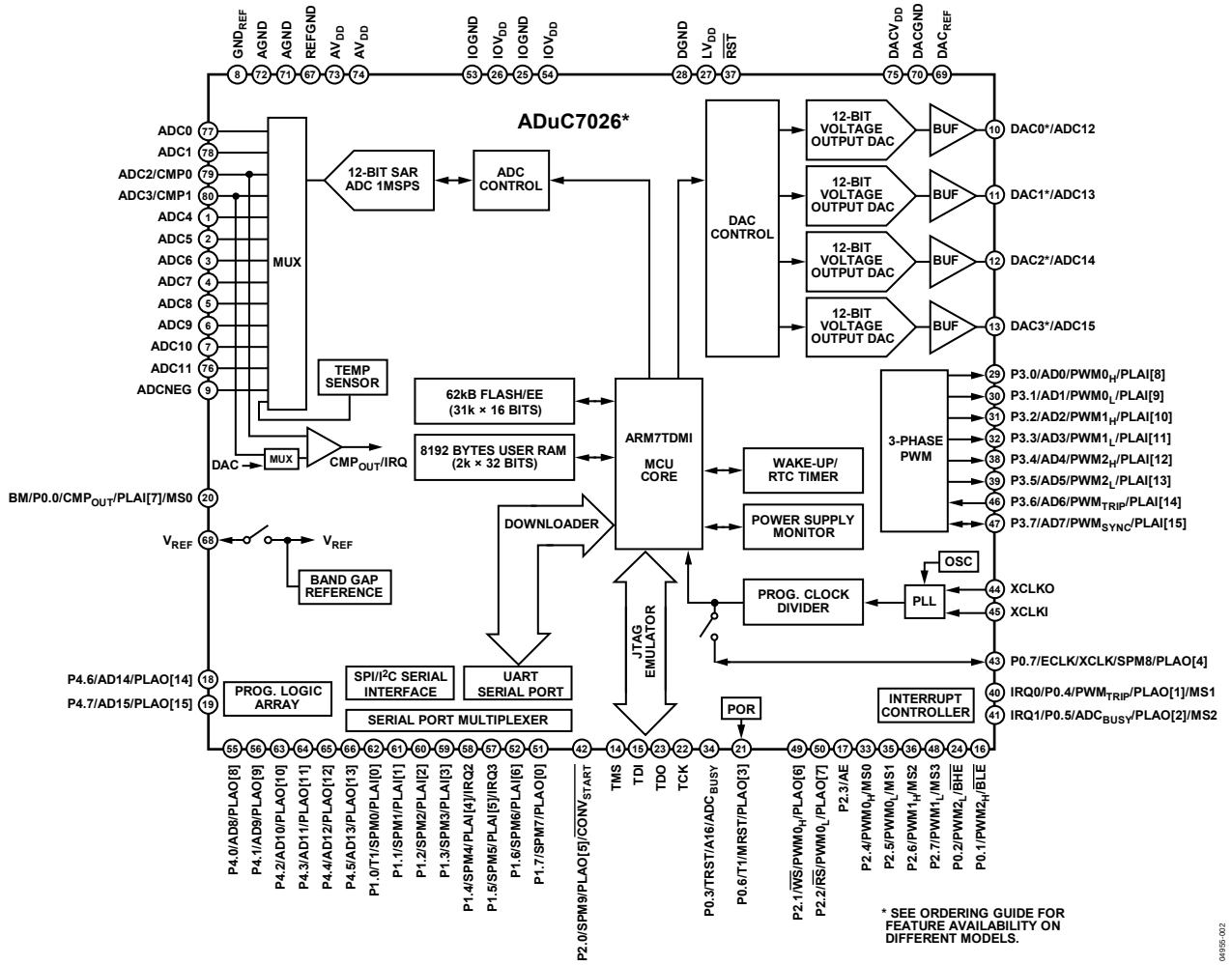

Figure 11.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
MCU CLOCK RATE					
From 32 kHz Internal Oscillator		326		kHz	CD[12] = 7
From 32 kHz External Crystal		41.78		MHz	CD[12] = 0
Using an External Clock	0.05		44	MHz	T_A = 85°C
	0.05		41.78	MHz	T_A = 125°C
START-UP TIME					Core clock = 41.78 MHz
At Power-On		130		ms	
From Pause/Nap Mode		24		ns	CD[12] = 0
		3.06		µs	CD[12] = 7
From Sleep Mode		1.58		ms	
From Stop Mode		1.7		ms	
PROGRAMMABLE LOGIC ARRAY (PLA)					
Pin Propagation Delay		12		ns	From input pin to output pin
Element Propagation Delay		2.5		ns	
POWER REQUIREMENTS[13, 14]					
Power Supply Voltage Range					
AV_{DD} to AGND and IOV_{DD} to IOGND	2.7		3.6	V	
Analog Power Supply Currents					
AV_{DD} Current		200		µA	ADC in idle mode; all parts except ADuC7019
		400		µA	ADC in idle mode; ADuC7019 only
$DACV_{DD}$ Current[15]		3	25	µA	
Digital Power Supply Current					
IOV_{DD} Current in Normal Mode					Code executing from Flash/EE
		7	10	mA	CD[12] = 7
		11	15	mA	CD[12] = 3
		40	45	mA	CD[12] = 0 (41.78 MHz clock)
IOV_{DD} Current in Pause Mode		25	30	mA	CD[12] = 0 (41.78 MHz clock)
IOV_{DD} Current in Sleep Mode		250	400	µA	T_A = 85°C
		600	1000	µA	T_A = 125°C
Additional Power Supply Currents					
ADC		2		mA	@ 1 MSPS
		0.7		mA	@ 62.5 kSPS
DAC		700		µA	per DAC
ESD TESTS					2.5 V reference, T_A = 25°C
HBM Passed Up To			4	kV	
FCIDM Passed Up To			0.5	kV	

[1] All ADC channel specifications are guaranteed during normal MicroConverter core operation.
[2] Apply to all ADC input channels.
[3] Measured using the factory-set default values in the ADC offset register (ADCOF) and gain coefficient register (ADCGN).
[4] Not production tested but supported by design and/or characterization data on production release.
[5] Measured using the factory-set default values in ADCOF and ADCGN with an external AD845 op amp as an input buffer stage as shown in Figure 59. Based on external ADC system components; the user may need to execute a system calibration to remove external endpoint errors and achieve these specifications (see the Calibration section).
[6] The input signal can be centered on any dc common-mode voltage (V_{CM}) as long as this value is within the ADC voltage input range specified.
[7] DAC linearity is calculated using a reduced code range of 100 to 3995.
[8] DAC gain error is calculated using a reduced code range of 100 to internal 2.5 V V_{REF}.
[9] Endurance is qualified as per JEDEC Standard 22, Method A117 and measured at −40°C, +25°C, +85°C, and +125°C.
[10] Retention lifetime equivalent at junction temperature (T_J) = 85°C as per JEDEC Standard 22m, Method A117. Retention lifetime derates with junction temperature.
[11] Test carried out with a maximum of eight I/Os set to a low output level.
[12] See the POWCON register.
[13] Power supply current consumption is measured in normal, pause, and sleep modes under the following conditions: normal mode with 3.6 V supply, pause mode with 3.6 V supply, and sleep mode with 3.6 V supply.
[14] IOV_{DD} power supply current decreases typically by 2 mA during a Flash/EE erase cycle.
[15] On the ADuC7019/20/21/22, this current must be added to the AV_{DD} current.

ABSOLUTE MAXIMUM RATINGS

AGND = REFGND = DACGND = GND_{REF}, T_A = 25°C, unless otherwise noted.

Table 10.

Parameter	Rating
AV_{DD} to IOV_{DD}	−0.3 V to +0.3 V
AGND to DGND	−0.3 V to +0.3 V
IOV_{DD} to IOGND, AV_{DD} to AGND	−0.3 V to +6 V
Digital Input Voltage to IOGND	−0.3 V to +5.3 V
Digital Output Voltage to IOGND	−0.3 V to IOV_{DD} + 0.3 V
V_{REF} to AGND	−0.3 V to AV_{DD} + 0.3 V
Analog Inputs to AGND	−0.3 V to AV_{DD} + 0.3 V
Analog Outputs to AGND	−0.3 V to AV_{DD} + 0.3 V
Operating Temperature Range, Industrial	–40°C to +125°C
Storage Temperature Range	–65°C to +150°C
Junction Temperature	150°C
θ_{JA} Thermal Impedance	
40-Lead LFCSP	26°C/W
49-Ball CSP_BGA	80°C/W
64-Lead LFCSP	24°C/W
64-Ball CSP_BGA	75°C/W
64-Lead LQFP	47°C/W
80-Lead LQFP	38°C/W
Peak Solder Reflow Temperature	
SnPb Assemblies (10 sec to 30 sec)	240°C
RoHS Compliant Assemblies (20 sec to 40 sec)	260°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Only one absolute maximum rating can be applied at any one time.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Address	Name	Byte	Access Type	Default Value	Page
Reference Address Base = 0xFFFF0480					
0x048C	REFCON	1	R/W	0x00	50
ADC Address Base = 0xFFFF0500					
0x0500	ADCCON	2	R/W	0x0600	46
0x0504	ADCCP	1	R/W	0x00	47
0x0508	ADCCN	1	R/W	0x01	47
0x050C	ADCSTA	1	R	0x00	48
0x0510	ADCDAT	4	R	0x00000000	48
0x0514	ADCRST	1	R/W	0x00	48
0x0530	ADCGN	2	R/W	0x0200	48
0x0534	ADCOF	2	R/W	0x0200	48
DAC Address Base = 0xFFFF0600					
0x0600	DAC0CON	1	R/W	0x00	56
0x0604	DAC0DAT	4	R/W	0x00000000	56
0x0608	DAC1CON	1	R/W	0x00	56
0x060C	DAC1DAT	4	R/W	0x00000000	56
0x0610	DAC2CON	1	R/W	0x00	56
0x0614	DAC2DAT	4	R/W	0x00000000	56
0x0618	DAC3CON	1	R/W	0x00	56
0x061C	DAC3DAT	4	R/W	0x00000000	56
UART Base Address = 0xFFFF0700					
0x0700	COMTX	1	R/W	0x00	71
	COMRX	1	R	0x00	71
	COMDIV0	1	R/W	0x00	71
0x0704	COMIEN0	1	R/W	0x00	71
	COMDIV1	1	R/W	0x00	72
0x0708	COMIID0	1	R	0x01	72
0x070C	COMCON0	1	R/W	0x00	72
0x0710	COMCON1	1	R/W	0x00	72
0x0714	COMSTA0	1	R	0x60	72
0x0718	COMSTA1	1	R	0x00	73
0x071C	COMSCR	1	R/W	0x00	73
0x0720	COMIEN1	1	R/W	0x04	73
0x0724	COMIID1	1	R	0x01	73
0x0728	COMADR	1	R/W	0xAA	74
0x072C	COMDIV2	2	R/W	0x0000	73

Address	Name	Byte	Access Type	Default Value	Page
I2C0 Base Address = 0xFFFF0800					
0x0800	I2C0MSTA	1	R/W	0x00	76
0x0804	I2C0SSTA	1	R	0x01	76
0x0808	I2C0SRX	1	R	0x00	77
0x080C	I2C0STX	1	W	0x00	77
0x0810	I2C0MRX	1	R	0x00	77
0x0814	I2C0MTX	1	W	0x00	77
0x0818	I2C0CNT	1	R/W	0x00	77
0x081C	I2C0ADR	1	R/W	0x00	77
0x0824	I2C0BYTE	1	R/W	0x00	77
0x0828	I2C0ALT	1	R/W	0x00	78
0x082C	I2C0CFG	1	R/W	0x00	78
0x0830	I2C0DIV	2	R/W	0x1F1F	79
0x0838	I2C0ID0	1	R/W	0x00	79
0x083C	I2C0ID1	1	R/W	0x00	79
0x0840	I2C0ID2	1	R/W	0x00	79
0x0844	I2C0ID3	1	R/W	0x00	79
0x0848	I2C0CCNT	1	R/W	0x01	79
0x084C	I2C0FSTA	2	R/W	0x0000	79
I2C1 Base Address = 0xFFFF0900					
0x0900	I2C1MSTA	1	R/W	0x00	76
0x0904	I2C1SSTA	1	R	0x01	76
0x0908	I2C1SRX	1	R	0x00	77
0x090C	I2C1STX	1	W	0x00	77
0x0910	I2C1MRX	1	R	0x00	77
0x0914	I2C1MTX	1	W	0x00	77
0x0918	I2C1CNT	1	R/W	0x00	77
0x091C	I2C1ADR	1	R/W	0x00	77
0x0924	I2C1BYTE	1	R/W	0x00	77
0x0928	I2C1ALT	1	R/W	0x00	78
0x092C	I2C1CFG	1	R/W	0x00	78
0x0930	I2C1DIV	2	R/W	0x1F1F	79
0x0938	I2C1ID0	1	R/W	0x00	79
0x093C	I2C1ID1	1	R/W	0x00	79
0x0940	I2C1ID2	1	R/W	0x00	79
0x0944	I2C1ID3	1	R/W	0x00	79
0x0948	I2C1CCNT	1	R/W	0x01	79
0x094C	I2C1FSTA	2	R/W	0x0000	79
SPI Base Address = 0xFFFF0A00					
0x0A00	SPISTA	1	R	0x00	75
0x0A04	SPIRX	1	R	0x00	75
0x0A08	SPITX	1	W	0x00	75
0x0A0C	SPIDIV	1	R/W	0x1B	75
0x0A10	SPICON	2	R/W	0x0000	75

Table 28. V_{CM} Ranges

AV_{DD}	V_{REF}	V_{CM} Min	V_{CM} Max	Signal Peak-to-Peak
3.3 V	2.5 V	1.25 V	2.05 V	2.5 V
	2.048 V	1.024 V	2.276 V	2.048 V
	1.25 V	0.75 V	2.55 V	1.25 V
3.0 V	2.5 V	1.25 V	1.75 V	2.5 V
	2.048 V	1.024 V	1.976 V	2.048 V
	1.25 V	0.75 V	2.25 V	1.25 V

CALIBRATION

By default, the factory-set values written to the ADC offset (ADCOF) and gain coefficient registers (ADCGN) yield optimum performance in terms of end-point errors and linearity for standalone operation of the part (see the Specifications section). If system calibration is required, it is possible to modify the default offset and gain coefficients to improve end-point errors, but note that any modification to the factory-set ADCOF and ADCGN values can degrade ADC linearity performance.

For system offset error correction, the ADC channel input stage must be tied to AGND. A continuous software ADC conversion loop must be implemented by modifying the value in ADCOF until the ADC result (ADCDAT) reads Code 0 to Code 1. If the ADCDAT value is greater than 1, ADCOF should be decremented until ADCDAT reads 0 to 1. Offset error correction is done digitally and has a resolution of 0.25 LSB and a range of ±3.125% of V_{REF}.

For system gain error correction, the ADC channel input stage must be tied to V_{REF}. A continuous software ADC conversion loop must be implemented to modify the value in ADCGN until the ADC result (ADCDAT) reads Code 4094 to Code 4095. If the ADCDAT value is less than 4094, ADCGN should be incremented until ADCDAT reads 4094 to 4095. Similar to the offset calibration, the gain calibration resolution is 0.25 LSB with a range of ±3% of V_{REF}.

TEMPERATURE SENSOR

The ADuC7019/20/21/22/24/25/26/27/28/29 provide voltage output from on-chip band gap references proportional to absolute temperature. This voltage output can also be routed through the front-end ADC multiplexer (effectively an additional ADC channel input) facilitating an internal temperature sensor channel, measuring die temperature to an accuracy of ±3°C.

The following is an example routine showing how to use the internal temperature sensor:

```
int main(void)
{
float a = 0;
      short b;
      ADCCON = 0x20;    // power-on the ADC
      delay(2000);
      ADCCP = 0x10;  // Select Temperature
Sensor as an // input to the ADC
      REFCON = 0x01; // connect internal 2.5V
reference // to Vref pin
      ADCCON = 0xE4; // continuous conversion
      while(1)
      {
              while (!ADCSTA){};
      // wait for end of conversion
              b = (ADCDAT >> 16);
      // To calculate temperature in °C, use
the formula:
              a = 0x525 - b;
      // ((Temperature = 0x525 - Sensor
Voltage) / 1.3)
              a /= 1.3;
              b = floor(a);
              printf("Temperature: %d
oC\n",b);
      }
      return 0;
}
```

BAND GAP REFERENCE

Each ADuC7019/20/21/22/24/25/26/27/28/29 provides an on-chip band gap reference of 2.5 V, which can be used for the ADC and DAC. This internal reference also appears on the V_{REF} pin. When using the internal reference, a 0.47 µF capacitor must be connected from the external V_{REF} pin to AGND to ensure stability and fast response during ADC conversions. This reference can also be connected to an external pin (V_{REF}) and used as a reference for other circuits in the system. An external buffer is required because of the low drive capability of the V_{REF} output. A programmable option also allows an external reference input on the V_{REF} pin. Note that it is not possible to disable the internal reference. Therefore, the external reference source must be capable of overdriving the internal reference source.

Table 29. REFCON Register

Name	Address	Default Value	Access
REFCON	0xFFFF048C	0x00	R/W

The band gap reference interface consists of an 8-bit MMR REFCON, described in Table 30.

Table 30. REFCON MMR Bit Designations

Bit	Description
7:1	Reserved.
0	Internal reference output enable. Set by user to connect the internal 2.5 V reference to the V_{REF} pin. The reference can be used for an external component but must be buffered. Cleared by user to disconnect the reference from the V_{REF} pin.

Table 35. FEECON Register

Name	Address	Default Value	Access
FEECON	0xFFFFF808	0x07	R/W

FEECON is an 8-bit command register. The commands are described in Table 36.

Table 36. Command Codes in FEECON

Code	Command	Description
0x00[1]	Null	Idle state.
0x01[1]	Single read	Load FEEDAT with the 16-bit data. Indexed by FEEADR.
0x02[1]	Single write	Write FEEDAT at the address pointed to by FEEADR. This operation takes 50 μs.
0x03[1]	Erase/write	Erase the page indexed by FEEADR and write FEEDAT at the location pointed by FEEADR. This operation takes approximately 24 ms.
0x04[1]	Single verify	Compare the contents of the location pointed by FEEADR to the data in FEEDAT. The result of the comparison is returned in FEESTA, Bit 1.
0x05[1]	Single erase	Erase the page indexed by FEEADR.
0x06[1]	Mass erase	Erase 62 kB of user space. The 2 kB of kernel are protected. This operation takes 2.48 sec. To prevent accidental execution, a command sequence is required to execute this instruction. See the Command Sequence for Executing a Mass Erase section.
0x07	Reserved	Reserved.
0x08	Reserved	Reserved.
0x09	Reserved	Reserved.
0x0A	Reserved	Reserved.
0x0B	Signature	Give a signature of the 64 kB of Flash/EE in the 24-bit FEESIGN MMR. This operation takes 32,778 clock cycles.
0x0C	Protect	This command can run only once. The value of FEEPRO is saved and removed only with a mass erase (0x06) of the key.
0x0D	Reserved	Reserved.
0x0E	Reserved	Reserved.
0x0F	Ping	No operation; interrupt generated.

[1] The FEECON register always reads 0x07 immediately after execution of any of these commands.

Table 37. FEEDAT Register

Name	Address	Default Value	Access
FEEDAT	0xFFFFF80C	0xXXXX[1]	R/W

[1] X = 0, 1, 2, or 3.

FEEDAT is a 16-bit data register.

Table 38. FEEADR Register

Name	Address	Default Value	Access
FEEADR	0xFFFFF810	0x0000	R/W

FEEADR is another 16-bit address register.

Table 39. FEESIGN Register

Name	Address	Default Value	Access
FEESIGN	0xFFFFF818	0xFFFFFF	R

FEESIGN is a 24-bit code signature.

Table 40. FEEPRO Register

Name	Address	Default Value	Access
FEEPRO	0xFFFFF81C	0x00000000	R/W

FEEPRO MMR provides protection following a subsequent reset of the MMR. It requires a software key (see Table 42).

Table 41. FEEHIDE Register

Name	Address	Default Value	Access
FEEHIDE	0xFFFFF820	0xFFFFFFFF	R/W

FEEHIDE MMR provides immediate protection. It does not require any software key. Note that the protection settings in FEEHIDE are cleared by a reset (see Table 42).

Table 42. FEEPRO and FEEHIDE MMR Bit Designations

Bit	Description
31	Read protection. Cleared by user to protect all code. Set by user to allow reading the code.
30:0	Write protection for Page 123 to Page 120, Page 119 to Page 116, and Page 0 to Page 3. Cleared by user to protect the pages from writing. Set by user to allow writing the pages.

Command Sequence for Executing a Mass Erase

```
FEEDAT=0x3CFF;
FEEADR = 0xFFC3;
FEEMOD= FEEMOD|0x8;    //Erase key enable
FEECON=0x06;           //Mass erase command
```

Input offset voltage (V_{OS}) is the difference between the center of the hysteresis range and the ground level. This can either be positive or negative. The hysteresis voltage (V_H) is one-half the width of the hysteresis range.

Comparator Interface

The comparator interface consists of a 16-bit MMR, CMPCON, which is described in Table 56.

Table 55. CMPCON Register

Name	Address	Default Value	Access
CMPCON	0xFFFF0444	0x0000	R/W

Table 56. CMPCON MMR Bit Descriptions

Bit	Name	Value	Description
15:11			Reserved.
10	CMPEN		Comparator enable bit. Set by user to enable the comparator. Cleared by user to disable the comparator.
9:8	CMPIN		Comparator negative input select bits.
		00	$AV_{DD}/2$.
		01	ADC3 input.
		10	DAC0 output.
		11	Reserved.
7:6	CMPOC		Comparator output configuration bits.
		00	Reserved.
		01	Reserved.
		10	Output on CMP_{OUT}.
		11	IRQ.
5	CMPOL		Comparator output logic state bit. When low, the comparator output is high if the positive input (CMP0) is above the negative input (CMP1). When high, the comparator output is high if the positive input is below the negative input.
4:3	CMPRES		Response time.
		00	5 µs response time is typical for large signals (2.5 V differential). 17 µs response time is typical for small signals (0.65 mV differential).
		11	3 µs typical.
		01/10	Reserved.
2	CMPHYST		Comparator hysteresis bit. Set by user to have a hysteresis of about 7.5 mV. Cleared by user to have no hysteresis.
1	CMPORI		Comparator output rising edge interrupt. Set automatically when a rising edge occurs on the monitored voltage (CMP0). Cleared by user by writing a 1 to this bit.
0	CMPOFI		Comparator output falling edge interrupt. Set automatically when a falling edge occurs on the monitored voltage (CMP0). Cleared by user.

OSCILLATOR AND PLL—POWER CONTROL

Clocking System

Each ADuC7019/20/21/22/24/25/26/27/28/29 integrates a 32.768 kHz ±3% oscillator, a clock divider, and a PLL. The PLL locks onto a multiple (1275) of the internal oscillator or an external 32.768 kHz crystal to provide a stable 41.78 MHz clock (UCLK) for the system. To allow power saving, the core can operate at this frequency, or at binary submultiples of it. The actual core operating frequency, $UCLK/2^{CD}$, is refered to as HCLK. The default core clock is the PLL clock divided by 8 (CD = 3) or 5.22 MHz. The core clock frequency can also come from an external clock on the ECLK pin as described in Figure 67. The core clock can be outputted on ECLK when using an internal oscillator or external crystal.

Note that when the ECLK pin is used to output the core clock, the output signal is not buffered and is not suitable for use as a clock source to an external device without an external buffer.

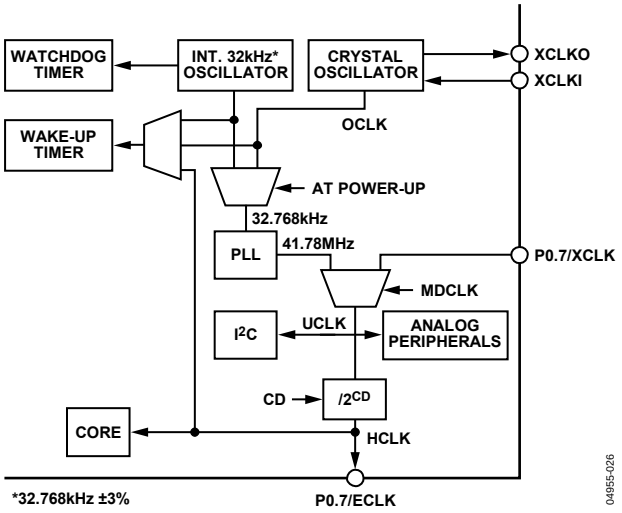

Figure 67. Clocking System

The selection of the clock source is in the PLLCON register. By default, the part uses the internal oscillator feeding the PLL.

External Crystal Selection

To switch to an external crystal, the user must do the following:

1. Enable the Timer2 interrupt and configure it for a timeout period of >120 µs.
2. Follow the write sequence to the PLLCON register, setting the MDCLK bits to 01 and clearing the OSEL bit.
3. Force the part into NAP mode by following the correct write sequence to the POWCON register.

   When the part is interrupted from NAP mode by the Timer2 interrupt source, the clock source has switched to the external clock.

The PWMDAT1 register is a 10-bit register with a maximum value of 0x3FF (= 1023), which corresponds to a maximum programmed dead time of

$$t_{D(max)} = 1023 \times 2 \times t_{CORE} = 1023 \times 2 \times 24 \times 10^{-9} = 48.97\ \mu s$$

for a core clock of 41.78 MHz.

The dead time can be programmed to be zero by writing 0 to the PWMDAT1 register.

PWM Operating Mode (PWMCON and PWMSTA MMRs)

As discussed in the 3-Phase PWM section, the PWM controller of the ADuC7019/20/21/22/24/25/26/27/28/29 can operate in two distinct modes: single update mode and double update mode. The operating mode of the PWM controller is determined by the state of Bit 2 of the PWMCON register. If this bit is cleared, the PWM operates in the single update mode. Setting Bit 2 places the PWM in the double update mode. The default operating mode is single update mode.

In single update mode, a single PWMSYNC pulse is produced in each PWM period. The rising edge of this signal marks the start of a new PWM cycle and is used to latch new values from the PWM configuration registers (PWMDAT0 and PWMDAT1) and the PWM duty cycle registers (PWMCH0, PWMCH1, and PWMCH2) into the 3-phase timing unit. In addition, the PWMEN register is latched into the output control unit on the rising edge of the PWMSYNC pulse. In effect, this means that the characteristics and resulting duty cycles of the PWM signals can be updated only once per PWM period at the start of each cycle. The result is symmetrical PWM patterns about the midpoint of the switching period.

In double update mode, there is an additional PWMSYNC pulse produced at the midpoint of each PWM period. The rising edge of this new PWMSYNC pulse is again used to latch new values of the PWM configuration registers, duty cycle registers, and the PWMEN register. As a result, it is possible to alter both the characteristics (switching frequency and dead time) as well as the output duty cycles at the midpoint of each PWM cycle. Consequently, it is also possible to produce PWM switching patterns that are no longer symmetrical about the midpoint of the period (asymmetrical PWM patterns). In double update mode, it could be necessary to know whether operation at any point in time is in either the first half or the second half of the PWM cycle. This information is provided by Bit 0 of the PWMSTA register, which is cleared during operation in the first half of each PWM period (between the rising edge of the original PWMSYNC pulse and the rising edge of the new PWMSYNC pulse introduced in double update mode). Bit 0 of the PWMSTA register is set during operation in the second half of each PWM period. This status bit allows the user to make a determination of the particular half cycle during implementation of the PWMSYNC interrupt service routine, if required.

The advantage of double update mode is that lower harmonic voltages can be produced by the PWM process, and faster control bandwidths are possible. However, for a given PWM switching frequency, the PWMSYNC pulses occur at twice the rate in the double update mode. Because new duty cycle values must be computed in each PWMSYNC interrupt service routine, there is a larger computational burden on the ARM core in double update mode.

PWM Duty Cycles (PWMCH0, PWMCH1, and PWMCH2 MMRs)

The duty cycles of the six PWM output signals on Pin $PWM0_H$ to Pin $PWM2_L$ are controlled by the three 16-bit read/write duty cycle registers, PWMCH0, PWMCH1, and PWMCH2. The duty cycle registers are programmed in integer counts of the fundamental time unit, t_{CORE}. They define the desired on time of the high-side PWM signal produced by the 3-phase timing unit over half the PWM period. The switching signals produced by the 3-phase timing unit are also adjusted to incorporate the programmed dead time value in the PWMDAT1 register. The 3-phase timing unit produces active high signals so that a high level corresponds to a command to turn on the associated power device.

Figure 69 shows a typical pair of PWM outputs (in this case, 0H and 0L) from the timing unit in single update mode. All illustrated time values indicate the integer value in the associated register and can be converted to time by simply multiplying by the fundamental time increment, t_{CORE}. Note that the switching patterns are perfectly symmetrical about the midpoint of the switching period in this mode because the same values of PWMCH0, PWMDAT0, and PWMDAT1 are used to define the signals in both half cycles of the period.

Figure 69 also demonstrates how the programmed duty cycles are adjusted to incorporate the desired dead time into the resulting pair of PWM signals. The dead time is incorporated by moving the switching instants of both PWM signals (0H and 0L) away from the instant set by the PWMCH0 register.

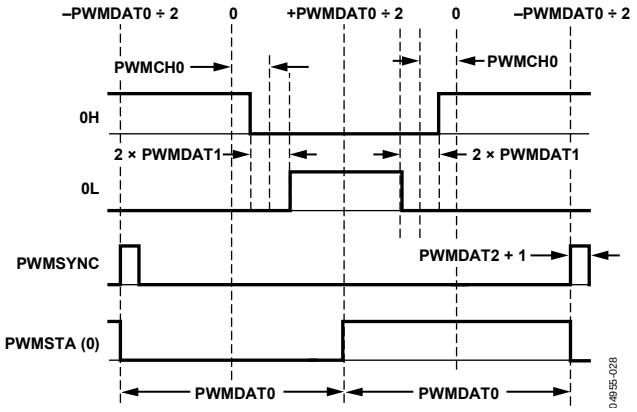

Figure 69. Typical PWM Outputs of the 3-Phase Timing Unit (Single Update Mode)

Both switching edges are moved by an equal amount (PWMDAT1 × t_{CORE}) to preserve the symmetrical output patterns.

Also shown are the PWMSYNC pulse and Bit 0 of the PWMSTA register, which indicates whether operation is in the first or second half cycle of the PWM period.

The resulting on times of the PWM signals over the full PWM period (two half periods) produced by the timing unit can be written as follows:

On the high side

$$t_{0HH} = PWMDAT0 + 2(PWMCH0 - PWMDAT1) \times t_{CORE}$$

$$t_{0HL} = PWMDAT0 - 2(PWMCH0 - PWMDAT1) \times t_{CORE}$$

and the corresponding duty cycles (*d*)

$$d_{0H} = t_{0HH}/t_S = ½ + (PWMCH0 - PWMDAT1)/PWMDAT0$$

and on the low side

$$t_{0LH} = PWMDAT0 - 2(PWMCH0 + PWMDAT1) \times t_{CORE}$$

$$t_{0LL} = PWMDAT0 + 2(PWMCH0 + PWMDAT1) \times t_{CORE}$$

and the corresponding duty cycles (*d*)

$$d_{OL} = t_{0LH}/t_S = ½ - (PWMCH0 + PWMDAT1)/PWMDAT0$$

The minimum permissible t_{0H} and t_{0L} values are zero, corresponding to a 0% duty cycle. In a similar fashion, the maximum value is t_S, corresponding to a 100% duty cycle.

Figure 70 shows the output signals from the timing unit for operation in double update mode. It illustrates a general case where the switching frequency, dead time, and duty cycle are all changed in the second half of the PWM period. The same value for any or all of these quantities can be used in both halves of the PWM cycle. However, there is no guarantee that symmetrical PWM signals are produced by the timing unit in double update mode. Figure 70 also shows that the dead time insertions into the PWM signals are done in the same way as in single update mode.

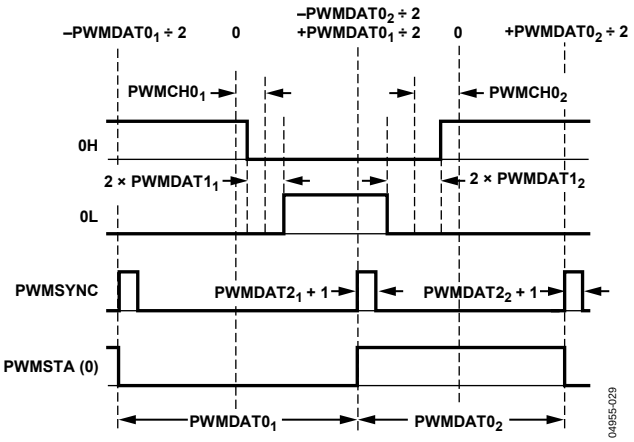

Figure 70. Typical PWM Outputs of the 3-Phase Timing Unit (Double Update Mode)

In general, the on times of the PWM signals in double update mode can be defined as follows:

On the high side

$$t_{0HH} = (PWMDAT0_1/2 + PWMDAT0_2/2 + PWMCH0_1 + PWMCH0_2 - PWMDAT1_1 - PWMDAT1_2) \times t_{CORE}$$

$$t_{0HL} = (PWMDAT0_1/2 + PWMDAT0_2/2 - PWMCH0_1 - PWMCH0_2 + PWMDAT1_1 + PWMDAT1_2) \times t_{CORE}$$

where Subscript *1* refers to the value of that register during the first half cycle, and Subscript *2* refers to the value during the second half cycle.

The corresponding duty cycles (*d*) are

$$d_{0H} = t_{0HH}/t_S = (PWMDAT0_1/2 + PWMDAT0_2/2 + PWMCH0_1 + PWMCH0_2 - PWMDAT1_1 - PWMDAT1_2)/(PWMDAT0_1 + PWMDAT0_2)$$

On the low side

$$t_{0LH} = (PWMDAT0_1/2 + PWMDAT0_2/2 + PWMCH0_1 + PWMCH0_2 + PWMDAT1_1 + PWMDAT1_2) \times t_{CORE}$$

$$t_{0LL} = (PWMDAT0_1/2 + PWMDAT0_2/2 - PWMCH0_1 - PWMCH0_2 - PWMDAT1_1 - PWMDAT1_2) \times t_{CORE}$$

where Subscript *1* refers to the value of that register during the first half cycle, and Subscript *2* refers to the value during the second half cycle.

The corresponding duty cycles (d) are

$$d_{0L} = t_{0LH}/t_S = (\text{PWMDAT0}_1/2 + PWMDAT0_2/2 + PWMCH0_1 + PWMCH0_2 + PWMDAT1_1 + PWMDAT1_2)/(PWMDAT0_1 + PWMDAT0_2)$$

For the completely general case in double update mode (see Figure 70), the switching period is given by

$$t_S = (PWMDAT0_1 + PWMDAT0_2) \times t_{CORE}$$

Again, the values of t_{0H} and t_{0L} are constrained to lie between zero and t_S.

PWM signals similar to those illustrated in Figure 69 and Figure 70 can be produced on the 1H, 1L, 2H, and 2L outputs by programming the PWMCH1 and PWMCH2 registers in a manner identical to that described for PWMCH0. The PWM controller does not produce any PWM outputs until all of the PWMDAT0, PWMCH0, PWMCH1, and PWMCH2 registers have been written to at least once. When these registers are written, internal counting of the timers in the 3-phase timing unit is enabled.

Writing to the PWMDAT0 register starts the internal timing of the main PWM timer. Provided that the PWMDAT0 register is written to prior to the PWMCH0, PWMCH1, and PWMCH2 registers in the initialization, the first PWMSYNC pulse and interrupt (if enabled) appear 1.5 × t_{CORE} × PWMDAT0 seconds after the initial write to the PWMDAT0 register in single update mode. In double update mode, the first PWMSYNC pulse appears after PWMDAT0 × t_{CORE} seconds.

The GDCLK value can range from 0 to 255, corresponding to a programmable chopping frequency rate of 40.8 kHz to 10.44 MHz for a 41.78 MHz core frequency. The gate drive features must be programmed before operation of the PWM controller and are typically not changed during normal operation of the PWM controller. Following a reset, all bits of the PWMCFG register are cleared so that high frequency chopping is disabled, by default.

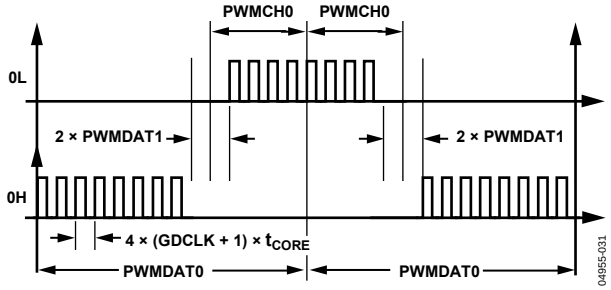

Figure 72. Typical PWM Signals with High Frequency Gate Chopping Enabled on Both High-Side and Low-Side Switches

PWM Shutdown

In the event of external fault conditions, it is essential that the PWM system be instantaneously shut down in a safe fashion. A low level on the PWM_{TRIP} pin provides an instantaneous, asynchronous (independent of the MicroConverter core clock) shutdown of the PWM controller. All six PWM outputs are placed in the off state, that is, in low state. In addition, the PWMSYNC pulse is disabled. The PWM_{TRIP} pin has an internal pull-down resistor to disable the PWM if the pin becomes disconnected. The state of the PWM_{TRIP} pin can be read from Bit 3 of the PWMSTA register.

If a PWM shutdown command occurs, a PWMTRIP interrupt is generated, and internal timing of the 3-phase timing unit of the PWM controller is stopped. Following a PWM shutdown, the PWM can be reenabled (in a PWMTRIP interrupt service routine, for example) only by writing to all of the PWMDAT0, PWMCH0, PWMCH1, and PWMCH2 registers. Provided that the external fault is cleared and the PWMTRIP is returned to a high level, the internal timing of the 3-phase timing unit resumes, and new duty-cycle values are latched on the next PWMSYNC boundary.

Note that the PWMTRIP interrupt is available in IRQ only, and the PWMSYNC interrupt is available in FIQ only. Both interrupts share the same bit in the interrupt controller. Therefore, only one of the interrupts can be used at a time. See the Interrupt System section for further details.

PWM MMRs Interface

The PWM block is controlled via the MMRs described in this section.

Table 66. PWMCON Register

Name	Address	Default Value	Access
PWMCON	0xFFFFFC00	0x0000	R/W

PWMCON is a control register that enables the PWM and chooses the update rate.

Table 67. PWMCON MMR Bit Descriptions

Bit	Name	Description
7:5		Reserved.
4	PWM_SYNCSEL	External sync select. Set to use external sync. Cleared to use internal sync.
3	PWM_EXTSYNC	External sync select. Set to select external synchronous sync signal. Cleared for asynchronous sync signal.
2	PWMDBL	Double update mode. Set to 1 by user to enable double update mode. Cleared to 0 by the user to enable single update mode.
1	PWM_SYNC_EN	PWM synchronization enable. Set by user to enable synchronization. Cleared by user to disable synchronization.
0	PWMEN	PWM enable bit. Set to 1 by user to enable the PWM. Cleared to 0 by user to disable the PWM. Also cleared automatically with PWMTRIP (PWMSTA MMR).

Table 68. PWMSTA Register

Name	Address	Default Value	Access
PWMSTA	0xFFFFFC04	0x0000	R/W

PWMSTA reflects the status of the PWM.

Table 69. PWMSTA MMR Bit Descriptions

Bit	Name	Description
15:10		Reserved.
9	PWMSYNCINT	PWM sync interrupt bit. Writing a 1 to this bit clears this interrupt.
8	PWMTRIPINT	PWM trip interrupt bit. Writing a 1 to this bit clears this interrupt.
3	PWMTRIP	Raw signal from the PWM_{TRIP} pin.
2:1		Reserved.
0	PWMPHASE	PWM phase bit. Set to 1 by the MicroConverter when the timer is counting down (first half). Cleared to 0 by the MicroConverter when the timer is counting up (second half).

Table 116. COMIID1 MMR Bit Descriptions

Bit 3:1 Status Bits	Bit 0 NINT	Priority	Definition	Clearing Operation
000	1		No interrupt	
110	0	2	Matching network address	Read COMRX
101	0	3	Address transmitted, buffer empty	Write data to COMTX or read COMIID0
011	0	1	Receive line status interrupt	Read COMSTA0
010	0	2	Receive buffer full interrupt	Read COMRX
001	0	3	Transmit buffer empty interrupt	Write data to COMTX or read COMIID0
000	0	4	Modem status interrupt	Read COMSTA1

Note that to receive a network address interrupt, the slave must ensure that Bit 0 of COMIEN0 (enable receive buffer full interrupt) is set to 1.

Table 117. COMADR Register

Name	Address	Default Value	Access
COMADR	0xFFFF0728	0xAA	R/W

COMADR is an 8-bit, read/write network address register that holds the address checked for by the network addressable UART. Upon receiving this address, the device interrupts the processor and/or sets the appropriate status bit in COMIID1.

SERIAL PERIPHERAL INTERFACE

The ADuC7019/20/21/22/24/25/26/27/28/29 integrate a complete hardware serial peripheral interface (SPI) on-chip. SPI is an industry standard, synchronous serial interface that allows eight bits of data to be synchronously transmitted and simultaneously received, that is, full duplex up to a maximum bit rate of 3.48 Mb, as shown in Table 118. The SPI interface is not operational with core clock divider (CD) bits. POWCON[2:0] = 6 or 7 in master mode.

The SPI port can be configured for master or slave operation. and typically consists of four pins: MISO (P1.5), MOSI (P1.6), SCLK (P1.4), and $\overline{CS}$ (P1.7).

On the transmit side, the SPITX register (and a TX shift register outside it) loads data onto the transmit pin (in slave mode, MISO; in master mode, MOSI). The transmit status bit, Bit 0, in SPISTA indicates whether there is valid data in the SPITX register.

Similarly, the receive data path consists of the SPIRX register (and an RX shift register). SPISTA, Bit 3 indicates whether there is valid data in the SPIRX register. If valid data in the SPIRX register is overwritten or if valid data in the RX shift register is discarded, SPISTA, Bit 5 (the overflow bit) is set.

MISO (Master In, Slave Out) Pin

The MISO pin is configured as an input line in master mode and an output line in slave mode. The MISO line on the master (data in) should be connected to the MISO line in the slave device (data out). The data is transferred as byte wide (8-bit) serial data, MSB first.

MOSI (Master Out, Slave In) Pin

The MOSI pin is configured as an output line in master mode and an input line in slave mode. The MOSI line on the master (data out) should be connected to the MOSI line in the slave device (data in). The data is transferred as byte wide (8-bit) serial data, MSB first.

SCLK (Serial Clock I/O) Pin

The master serial clock (SCLK) is used to synchronize the data being transmitted and received through the MOSI SCLK period. Therefore, a byte is transmitted/received after eight SCLK periods. The SCLK pin is configured as an output in master mode and as an input in slave mode.

In master mode, the polarity and phase of the clock are controlled by the SPICON register, and the bit rate is defined in the SPIDIV register as follows:

$$f_{SERIAL\,CLOCK} = \frac{f_{UCLK}}{2\times(1+SPIDIV)}$$

The maximum speed of the SPI clock is dependent on the clock divider bits and is summarized in Table 118.

Table 118. SPI Speed vs. Clock Divider Bits in Master Mode

CD Bits	0	1	2	3	4	5
SPIDIV in Hex	0x05	0x0B	0x17	0x2F	0x5F	0xBF
SPI dpeed in MHz	3.482	1.741	0.870	0.435	0.218	0.109

In slave mode, the SPICON register must be configured with the phase and polarity of the expected input clock. The slave accepts data from an external master up to 10.4 Mb at CD = 0. The formula to determine the maximum speed is as follows:

$$f_{SERIAL\,CLOCK} = \frac{f_{HCLK}}{4}$$

In both master and slave modes, data is transmitted on one edge of the SCL signal and sampled on the other. Therefore, it is important that the polarity and phase be configured the same for the master and slave devices.

Chip Select ($\overline{CS}$ Input) Pin

In SPI slave mode, a transfer is initiated by the assertion of $\overline{CS}$, which is an active low input signal. The SPI port then transmits and receives 8-bit data until the transfer is concluded by deassertion of $\overline{CS}$. In slave mode, $\overline{CS}$ is always an input.

I²C-COMPATIBLE INTERFACES

The ADuC7019/20/21/22/24/25/26/27/28/29 support two licensed I²C interfaces. The I²C interfaces are both implemented as a hard-ware master and a full slave interface. Because the two I²C inter-faces are identical, this data sheet describes only I2C0 in detail. Note that the two masters and one of the slaves have individual interrupts (see the Interrupt System section).

Note that when configured as an I²C master device, the ADuC7019/20/21/22/24/25/26/27/28/29 cannot generate a repeated start condition.

The two GPIO pins used for data transfer, SDAx and SCLx, are configured in a wired-AND format that allows arbitration in a multimaster system. These pins require external pull-up resistors. Typical pull-up values are 10 kΩ.

The I²C bus peripheral address in the I²C bus system is programmed by the user. This ID can be modified any time a transfer is not in progress. The user can configure the interface to respond to four slave addresses.

The transfer sequence of an I²C system consists of a master device initiating a transfer by generating a start condition while the bus is idle. The master transmits the slave device address and the direction of the data transfer during the initial address transfer. If the master does not lose arbitration and the slave acknowledges, the data transfer is initiated. This continues until the master issues a stop condition and the bus becomes idle.

The I²C peripheral can be configured only as a master or slave at any given time. The same I²C channel cannot simultaneously support master and slave modes.

Serial Clock Generation

The I²C master in the system generates the serial clock for a transfer. The master channel can be configured to operate in fast mode (400 kHz) or standard mode (100 kHz).

The bit rate is defined in the I2C0DIV MMR as follows:

$$f_{SERIAL\ CLOCK} = \frac{f_{UCLK}}{(2 + DIVH) + (2 + DIVL)}$$

where:
f_{UCLK} = clock before the clock divider.
$DIVH$ = the high period of the clock.
$DIVL$ = the low period of the clock.

Thus, for 100 kHz operation,

$DIVH = DIVL$ = 0xCF

and for 400 kHz,

$DIVH$ = 0x28, $DIVL$ = 0x3C

The I2CxDIV registers correspond to DIVH:DIVL.

Slave Addresses

The registers I2C0ID0, I2C0ID1, I2C0ID2, and I2C0ID3 contain the device IDs. The device compares the four I2C0IDx registers to the address byte. To be correctly addressed, the seven MSBs of either ID register must be identical to that of the seven MSBs of the first received address byte. The LSB of the ID registers (the transfer direction bit) is ignored in the process of address recognition.

I²C Registers

The I²C peripheral interface consists of 18 MMRs, which are discussed in this section.

Table 126. I2CxMSTA Registers

Name	Address	Default Value	Access
I2C0MSTA	0xFFFF0800	0x00	R/W
I2C1MSTA	0xFFFF0900	0x00	R/W

I2CxMSTA are status registers for the master channel.

Table 127. I2C0MSTA MMR Bit Descriptions

Bit	Access Type	Description
7	R/W	Master transmit FIFO flush. Set by user to flush the master Tx FIFO. Cleared automatically after the master Tx FIFO is flushed. This bit also flushes the slave receive FIFO.
6	R	Master busy. Set automatically if the master is busy. Cleared automatically.
5	R	Arbitration loss. Set in multimaster mode if another master has the bus. Cleared when the bus becomes available.
4	R	No ACK. Set automatically if there is no acknowledge of the address by the slave device. Cleared automatically by reading the I2C0MSTA register.
3	R	Master receive IRQ. Set after receiving data. Cleared automatically by reading the I2C0MRX register.
2	R	Master transmit IRQ. Set at the end of a transmission. Cleared automatically by writing to the I2C0MTX register.
1	R	Master transmit FIFO underflow. Set automatically if the master transmit FIFO is underflowing. Cleared automatically by writing to the I2C0MTX register.
0	R	Master TX FIFO not full. Set automatically if the slave transmit FIFO is not full. Cleared automatically by writing twice to the I2C0STX register.

Table 128. I2CxSSTA Registers

Name	Address	Default Value	Access
I2C0SSTA	0xFFFF0804	0x01	R
I2C1SSTA	0xFFFF0904	0x01	R

I2CxSSTA are status registers for the slave channel.

Table 140. I2CxDIV Registers

Name	Address	Default Value	Access
I2C0DIV	0xFFFF0830	0x1F1F	R/W
I2C1DIV	0xFFFF0930	0x1F1F	R/W

I2CxDIV are the clock divider registers.

Table 141. I2CxIDx Registers

Name	Address	Default Value	Access
I2C0ID0	0xFFFF0838	0x00	R/W
I2C0ID1	0xFFFF083C	0x00	R/W
I2C0ID2	0xFFFF0840	0x00	R/W
I2C0ID3	0xFFFF0844	0x00	R/W
I2C1ID0	0xFFFF0938	0x00	R/W
I2C1ID1	0xFFFF093C	0x00	R/W
I2C1ID2	0xFFFF0940	0x00	R/W
I2C1ID3	0xFFFF0944	0x00	R/W

I2CxID0, I2CxID1, I2CxID2, and I2CxID3 are slave address device ID registers of I2Cx.

Table 142. I2CxCCNT Registers

Name	Address	Default Value	Access
I2C0CCNT	0xFFFF0848	0x01	R/W
I2C1CCNT	0xFFFF0948	0x01	R/W

I2CxCCNT are 8-bit start/stop generation counters. They hold off SDA low for start and stop conditions.

Table 143. I2CxFSTA Registers

Name	Address	Default Value	Access
I2C0FSTA	0xFFFF084C	0x0000	R/W
I2C1FSTA	0xFFFF094C	0x0000	R/W

I2CxFSTA are FIFO status registers.

Table 144. I2C0FSTA MMR Bit Descriptions

Bit	Access Type	Value	Description
15:10			Reserved.
9	R/W		Master transmit FIFO flush. Set by the user to flush the master Tx FIFO. Cleared automatically when the master Tx FIFO is flushed. This bit also flushes the slave receive FIFO.
8	R/W		Slave transmit FIFO flush. Set by the user to flush the slave Tx FIFO. Cleared automatically after the slave Tx FIFO is flushed.
7:6	R		Master Rx FIFO status bits.
		00	FIFO empty.
		01	Byte written to FIFO.
		10	One byte in FIFO.
		11	FIFO full.
5:4	R		Master Tx FIFO status bits.
		00	FIFO empty.
		01	Byte written to FIFO.
		10	One byte in FIFO.
		11	FIFO full.
3:2	R		Slave Rx FIFO status bits.
		00	FIFO empty.
		01	Byte written to FIFO.
		10	One byte in FIFO.
		11	FIFO full.
1:0	R		Slave Tx FIFO status bits.
		00	FIFO empty.
		01	Byte written to FIFO.
		10	One byte in FIFO.
		11	FIFO full.

PROCESSOR REFERENCE PERIPHERALS

INTERRUPT SYSTEM

There are 23 interrupt sources on the ADuC7019/20/21/22/24/25/26/27/28/29 that are controlled by the interrupt controller. Most interrupts are generated from the on-chip peripherals, such as ADC and UART. Four additional interrupt sources are generated from external interrupt request pins, IRQ0, IRQ1, IRQ2, and IRQ3. The ARM7TDMI CPU core only recognizes interrupts as one of two types: a normal interrupt request IRQ or a fast interrupt request FIQ. All the interrupts can be masked separately.

The control and configuration of the interrupt system are managed through nine interrupt-related registers, four dedicated to IRQ, and four dedicated to FIQ. An additional MMR is used to select the programmed interrupt source. The bits in each IRQ and FIQ register (except for Bit 23) represent the same interrupt source as described in Table 160.

Table 160. IRQ/FIQ MMRs Bit Description

Bit	Description
0	All interrupts OR'ed (FIQ only)
1	SWI
2	Timer0
3	Timer1
4	Wake-up timer (Timer2)
5	Watchdog timer (Timer3)
6	Flash control
7	ADC channel
8	PLL lock
9	I2C0 slave
10	I2C0 master
11	I2C1 master
12	SPI slave
13	SPI master
14	UART
15	External IRQ0
16	Comparator
17	PSM
18	External IRQ1
19	PLA IRQ0
20	PLA IRQ1
21	External IRQ2
22	External IRQ3
23	PWM trip (IRQ only)/PWM sync (FIQ only)

IRQ

The interrupt request (IRQ) is the exception signal to enter the IRQ mode of the processor. It is used to service general-purpose interrupt handling of internal and external events.

The four 32-bit registers dedicated to IRQ are IRQSTA, IRQSIG, IRQEN, and IRQCLR.

Table 161. IRQSTA Register

Name	Address	Default Value	Access
IRQSTA	0xFFFF0000	0x00000000	R

IRQSTA (read-only register) provides the current-enabled IRQ source status. When set to 1, that source should generate an active IRQ request to the ARM7TDMI core. There is no priority encoder or interrupt vector generation. This function is implemented in software in a common interrupt handler routine. All 32 bits are logically OR'ed to create the IRQ signal to the ARM7TDMI core.

Table 162. IRQSIG Register

Name	Address	Default Value	Access
IRQSIG	0xFFFF0004	0x00XXX000[1]	R

[1] X indicates an undefined value.

IRQSIG reflects the status of the different IRQ sources. If a peripheral generates an IRQ signal, the corresponding bit in the IRQSIG is set; otherwise, it is cleared. The IRQSIG bits are cleared when the interrupt in the particular peripheral is cleared. All IRQ sources can be masked in the IRQEN MMR. IRQSIG is read only.

Table 163. IRQEN Register

Name	Address	Default Value	Access
IRQEN	0xFFFF0008	0x00000000	R/W

IRQEN provides the value of the current enable mask. When each bit is set to 1, the source request is enabled to create an IRQ exception. When each bit is set to 0, the source request is disabled or masked, which does not create an IRQ exception.

Note that to clear an already enabled interrupt source, the user must set the appropriate bit in the IRQCLR register. Clearing an interrupt's IRQEN bit does not disable the interrupt.

Table 164. IRQCLR Register

Name	Address	Default Value	Access
IRQCLR	0xFFFF000C	0x00000000	W

IRQCLR (write-only register) clears the IRQEN register in order to mask an interrupt source. Each bit set to 1 clears the corresponding bit in the IRQEN register without affecting the remaining bits. The pair of registers, IRQEN and IRQCLR, independently manipulates the enable mask without requiring an atomic read-modify-write.

Timer1 (General-Purpose Timer)

Timer1 is a general-purpose, 32-bit timer (count down or count up) with a programmable prescaler. The source can be the 32 kHz external crystal, the core clock frequency, or an external GPIO (P1.0 or P0.6). The maximum frequency of the clock input is 44 Mhz). This source can be scaled by a factor of 1, 16, 256, or 32,768.

The counter can be formatted as a standard 32-bit value or as hours: minutes: seconds: hundredths.

Timer1 has a capture register (T1CAP) that can be triggered by a selected IRQ source initial assertion. This feature can be used to determine the assertion of an event more accurately than the precision allowed by the RTOS timer when the IRQ is serviced.

Timer1 can be used to start ADC conversions as shown in the block diagram in Figure 78.

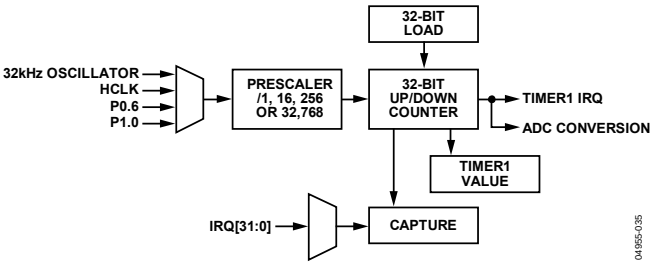

Figure 78. Timer1 Block Diagram

The Timer1 interface consists of five MMRs: T1LD, T1VAL, T1CON, T1CLRI, and T1CAP.

Table 177. T1LD Register

Name	Address	Default Value	Access
T1LD	0xFFFF0320	0x00000000	R/W

T1LD is a 32-bit load register.

Table 178. T1VAL Register

Name	Address	Default Value	Access
T1VAL	0xFFFF0324	0xFFFFFFFF	R

T1VAL is a 32-bit read-only register that represents the current state of the counter.

Table 179. T1CON Register

Name	Address	Default Value	Access
T1CON	0xFFFF0328	0x0000	R/W

T1CON is the configuration MMR described in Table 180.

GROUNDING AND BOARD LAYOUT RECOMMENDATIONS

As with all high resolution data converters, special attention must be paid to grounding and PC board layout of the ADuC7019/20/21/22/24/25/26/27/28/29-based designs to achieve optimum performance from the ADCs and DAC.

Although the parts have separate pins for analog and digital ground (AGND and IOGND), the user must not tie these to two separate ground planes unless the two ground planes are connected very close to the part. This is illustrated in the simplified example shown in Figure 91a. In systems where digital and analog ground planes are connected together somewhere else (at the system power supply, for example), the planes cannot be reconnected near the part because a ground loop results. In these cases, tie all the ADuC7019/20/21/22/24/25/26/27/28/29 AGND and IOGND pins to the analog ground plane, as illustrated in Figure 91b. In systems with only one ground plane, ensure that the digital and analog components are physically separated onto separate halves of the board so that digital return currents do not flow near analog circuitry (and vice versa).

The ADuC7019/20/21/22/24/25/26/27/28/29 can then be placed between the digital and analog sections, as illustrated in Figure 91c.

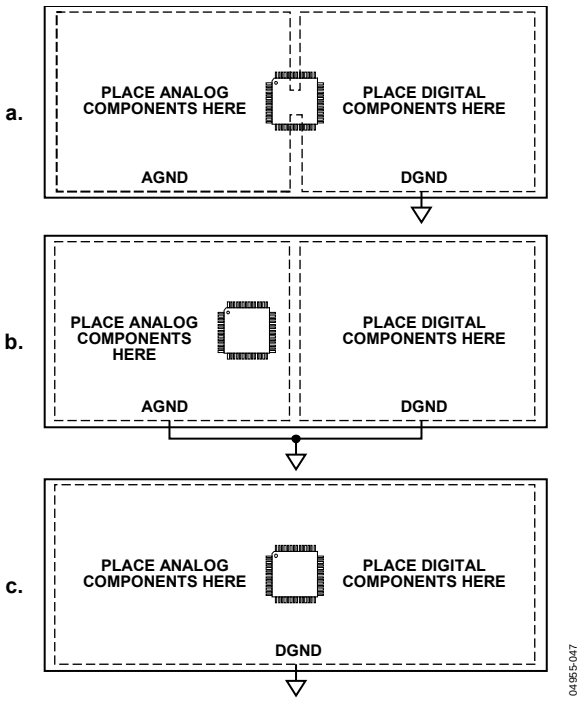

Figure 91. System Grounding Schemes

In all of these scenarios, and in more complicated real-life applications, the user should pay particular attention to the flow of current from the supplies and back to ground. Make sure the return paths for all currents are as close as possible to the paths the currents took to reach their destinations.

For example, do not power components on the analog side (as seen in Figure 91b) with IOV_{DD} because that forces return currents from IOV_{DD} to flow through AGND. Avoid digital currents flowing under analog circuitry, which can occur if a noisy digital chip is placed on the left half of the board (shown in Figure 91c). If possible, avoid large discontinuities in the ground plane(s) such as those formed by a long trace on the same layer because they force return signals to travel a longer path. In addition, make all connections to the ground plane directly, with little or no trace separating the pin from its via to ground.

When connecting fast logic signals (rise/fall time < 5 ns) to any of the ADuC7019/20/21/22/24/25/26/27/28/29 digital inputs, add a series resistor to each relevant line to keep rise and fall times longer than 5 ns at the part's input pins. A value of 100 Ω or 200 Ω is usually sufficient to prevent high speed signals from coupling capacitively into the part and affecting the accuracy of ADC conversions.

CLOCK OSCILLATOR

The clock source for the ADuC7019/20/21/22/24/25/26/27/28/29 can be generated by the internal PLL or by an external clock input. To use the internal PLL, connect a 32.768 kHz parallel resonant crystal between XCLKI and XCLKO, and connect a capacitor from each pin to ground as shown in Figure 92. The crystal allows the PLL to lock correctly to give a frequency of 41.78 MHz. If no external crystal is present, the internal oscillator is used to give a typical frequency of 41.78 MHz ± 3%.

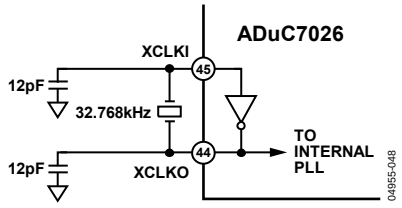

Figure 92. External Parallel Resonant Crystal Connections

To use an external source clock input instead of the PLL (see Figure 93), Bit 1 and Bit 0 of PLLCON must be modified.The external clock uses P0.7 and XCLK.

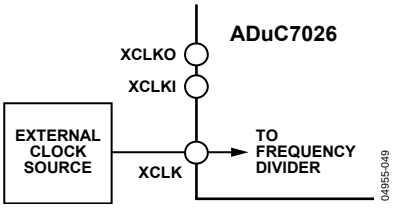

Figure 93. Connecting an External Clock Source

Using an external clock source, the ADuC7019/20/21/22/24/25/26/27/28/29-specified operational clock speed range is 50 kHz to 44 MHz ± 1%, which ensures correct operation of the analog peripherals and Flash/EE.

POWER-ON RESET OPERATION

An internal power-on reset (POR) is implemented on the ADuC7019/20/21/22/24/25/26/27/28/29. For LV_{DD} below 2.35 V typical, the internal POR holds the part in reset. As LV_{DD} rises above 2.35 V, an internal timer times out for, typically, 128 ms before the part is released from reset. The user must ensure that the power supply IOV_{DD} reaches a stable 2.7 V minimum level by this time. Likewise, on power-down, the internal POR holds the part in reset until LV_{DD} drops below 2.35 V.

Figure 94 illustrates the operation of the internal POR in detail.

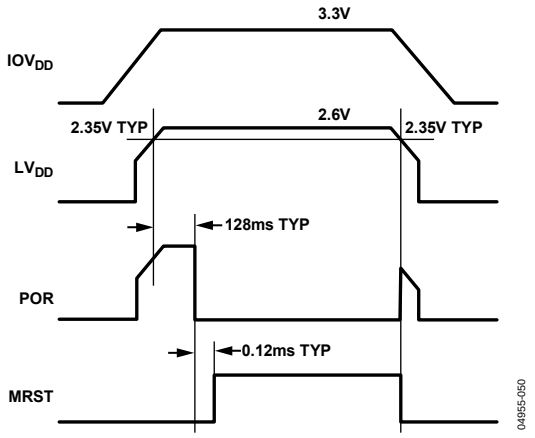

Figure 94. Internal Power-On Reset Operation

TYPICAL SYSTEM CONFIGURATION

A typical ADuC7020 configuration is shown in Figure 95. It summarizes some of the hardware considerations discussed in the previous sections. The bottom of the CSP package has an exposed pad that must be soldered to a metal plate on the board for mechanical reasons. The metal plate of the board can be connected to ground.

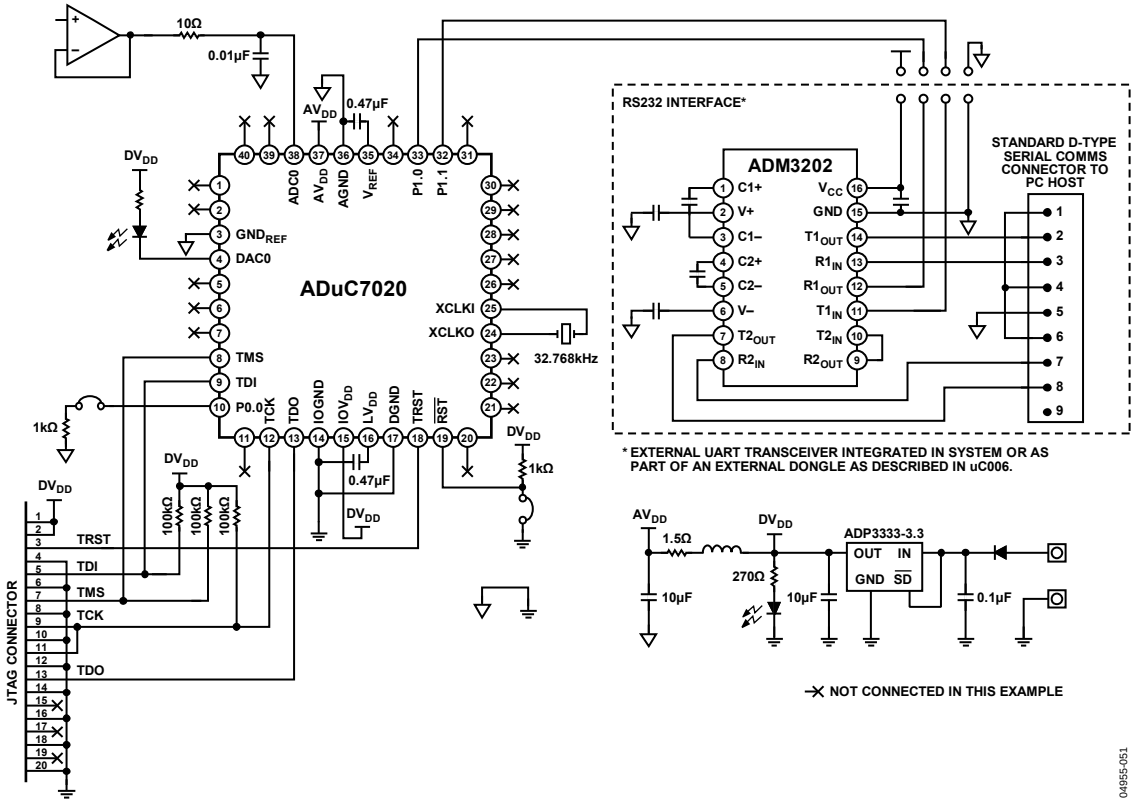

Figure 95. Typical System Configuration

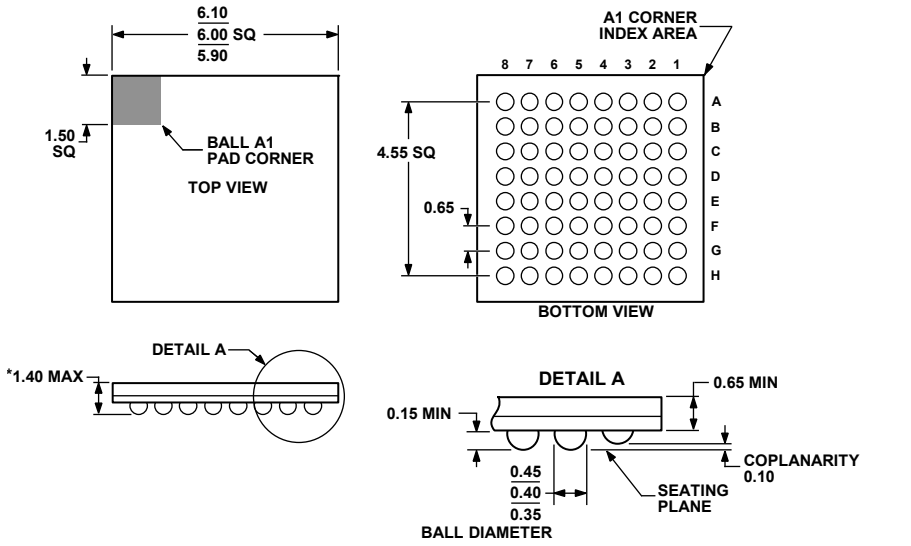

Figure 100. 64-Ball Chip Scale Package Ball Grid Array [CSP_BGA]
(BC-64-4)
Dimensions shown in millimeters

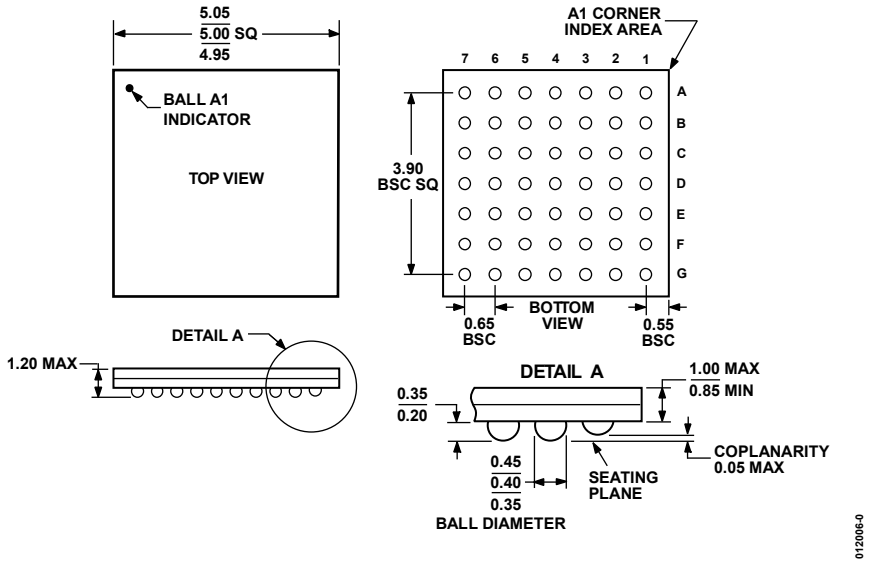

Figure 101. 49-Ball Chip Scale Package Ball Grid Array [CSP_BGA]
(BC-49-1)
Dimensions shown in millimeters