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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Obsolete
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	44MHz
Connectivity	EBI/EMI, I <sup>2</sup> C, SPI, UART/USART
Peripherals	PLA, PWM, PSM, Temp Sensor, WDT
Number of I/O	30
Program Memory Size	62KB (31K x16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 32
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 10x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad, CSP
Supplier Device Package	64-LFCSP-VQ (9x9)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/analog-devices/aduc7024bcpz62i-rl">https://www.e-xfl.com/product-detail/analog-devices/aduc7024bcpz62i-rl</a>

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## SPECIFICATIONS

$AV_{DD} = IOV_{DD} = 2.7\text{ V to }3.6\text{ V}$ ,  $V_{REF} = 2.5\text{ V}$  internal reference,  $f_{CORE} = 41.78\text{ MHz}$ ,  $T_A = -40^\circ\text{C to }+125^\circ\text{C}$ , unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
<b>ADC CHANNEL SPECIFICATIONS</b>					
ADC Power-Up Time		5		$\mu\text{s}$	Eight acquisition clocks and fADC/2  2.5 V internal reference 1.0 V external reference 2.5 V internal reference 1.0 V external reference ADC input is a dc voltage
DC Accuracy <sup>1,2</sup>					
Resolution	12			Bits	
Integral Nonlinearity		$\pm 0.6$	$\pm 1.5$	LSB	
		$\pm 1.0$		LSB	
Differential Nonlinearity <sup>3,4</sup>		$\pm 0.5$	$+1/-0.9$	LSB	
		$+0.7/-0.6$		LSB	
DC Code Distribution		1		LSB	
<b>ENDPOINT ERRORS<sup>5</sup></b>					
Offset Error		$\pm 1$	$\pm 2$	LSB	
Offset Error Match		$\pm 1$		LSB	
Gain Error		$\pm 2$	$\pm 5$	LSB	
Gain Error Match		$\pm 1$		LSB	
<b>DYNAMIC PERFORMANCE</b>					
Signal-to-Noise Ratio (SNR)		69		dB	$f_{IN} = 10\text{ kHz}$ sine wave, $f_{SAMPLE} = 1\text{ MSPS}$ Includes distortion and noise components
Total Harmonic Distortion (THD)		-78		dB	
Peak Harmonic or Spurious Noise (PHSN)		-75		dB	
Channel-to-Channel Crosstalk		-80		dB	Measured on adjacent channels
<b>ANALOG INPUT</b>					
Input Voltage Ranges					During ADC acquisition
Differential Mode			$V_{CM} \pm V_{REF}/2$	V	
Single-Ended Mode			0 to $V_{REF}$	V	
Leakage Current		$\pm 1$	$\pm 6$	$\mu\text{A}$	
Input Capacitance		20		pF	
<b>ON-CHIP VOLTAGE REFERENCE</b>					
Output Voltage		2.5		V	0.47 $\mu\text{F}$ from $V_{REF}$ to AGND
Accuracy			$\pm 5$	mV	
Reference Temperature Coefficient		$\pm 40$		ppm/ $^\circ\text{C}$	$T_A = 25^\circ\text{C}$
Power Supply Rejection Ratio		75		dB	$T_A = 25^\circ\text{C}$
Output Impedance		70		$\Omega$	
Internal $V_{REF}$ Power-On Time		1		ms	
<b>EXTERNAL REFERENCE INPUT</b>					
Input Voltage Range	0.625		$AV_{DD}$	V	
<b>DAC CHANNEL SPECIFICATIONS</b>					
DC Accuracy <sup>7</sup>					$R_L = 5\text{ k}\Omega$ , $C_L = 100\text{ pF}$  Guaranteed monotonic 2.5 V internal reference % of full scale on DAC0
Resolution		12		Bits	
Relative Accuracy		$\pm 2$		LSB	
Differential Nonlinearity			$\pm 1$	LSB	
Offset Error			$\pm 15$	mV	
Gain Error <sup>8</sup>			$\pm 1$	%	
Gain Error Mismatch		0.1		%	
<b>ANALOG OUTPUTS</b>					
Output Voltage Range_0		0 to $DAC_{REF}$		V	$DAC_{REF}$ range: $DAC_{GND}$ to $DAC_{VDD}$
Output Voltage Range_1		0 to 2.5		V	
Output Voltage Range_2		0 to $DAC_{VDD}$		V	
Output Impedance		2		$\Omega$	

TIMING SPECIFICATIONS

Table 2. External Memory Write Cycle

Parameter	Min	Typ	Max	Unit
CLK <sup>1</sup>		UCLK		
t <sub>MS_AFTER_CLKH</sub>	0		4	ns
t <sub>ADDR_AFTER_CLKH</sub>	4		8	ns
t <sub>AE_H_AFTER_MS</sub>		½ CLK		
t <sub>AE</sub>		(XMxPAR[14:12] + 1) × CLK		
t <sub>HOLD_ADDR_AFTER_AE_L</sub>		½ CLK + (!XMxPAR[10]) × CLK		
t <sub>HOLD_ADDR_BEFORE_WR_L</sub>		(!XMxPAR[8]) × CLK		
t <sub>WR_L_AFTER_AE_L</sub>		½ CLK + (!XMxPAR[10] + !XMxPAR[8]) × CLK		
t <sub>DATA_AFTER_WR_L</sub>	8		12	ns
t <sub>WR</sub>		(XMxPAR[7:4] + 1) × CLK		
t <sub>WR_H_AFTER_CLKH</sub>	0		4	ns
t <sub>HOLD_DATA_AFTER_WR_H</sub>		(!XMxPAR[8]) × CLK		
t <sub>BEN_AFTER_AE_L</sub>		½ CLK		
t <sub>RELEASE_MS_AFTER_WR_H</sub>		(!XMxPAR[8] + 1) × CLK		

<sup>1</sup> See Table 78.

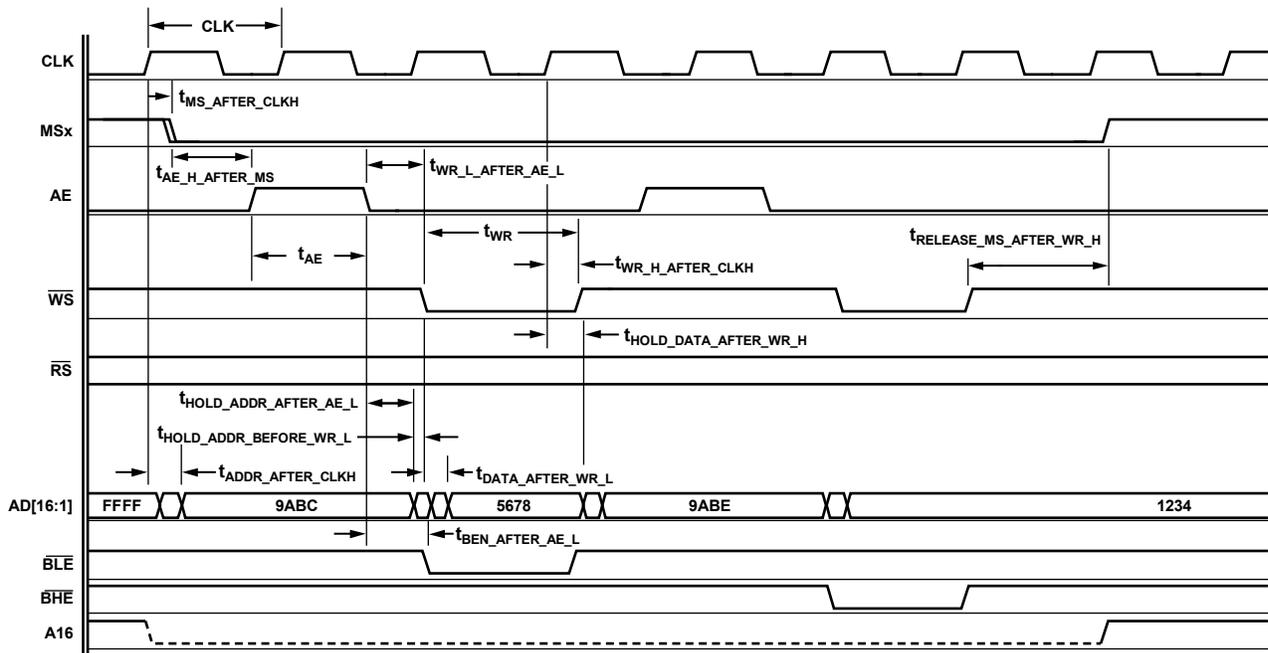


Figure 12. External Memory Write Cycle (See Table 78)



Table 9. SPI Slave Mode Timing (Phase Mode = 0)

Parameter	Description	Min	Typ	Max	Unit
$t_{\overline{CS}}$	$\overline{CS}$ to SCLK edge <sup>1</sup>	$(2 \times t_{HCLK}) + (2 \times t_{UCLK})$			ns
$t_{SL}$	SCLK low pulse width <sup>2</sup>		$(SPIDIV + 1) \times t_{HCLK}$		ns
$t_{SH}$	SCLK high pulse width <sup>2</sup>		$(SPIDIV + 1) \times t_{HCLK}$		ns
$t_{DAV}$	Data output valid after SCLK edge			25	ns
$t_{DSU}$	Data input setup time before SCLK edge <sup>1</sup>	$1 \times t_{UCLK}$			ns
$t_{DHD}$	Data input hold time after SCLK edge <sup>1</sup>	$2 \times t_{UCLK}$			ns
$t_{DF}$	Data output fall time		5	12.5	ns
$t_{DR}$	Data output rise time		5	12.5	ns
$t_{SR}$	SCLK rise time		5	12.5	ns
$t_{SF}$	SCLK fall time		5	12.5	ns
$t_{DOCS}$	Data output valid after $\overline{CS}$ edge			25	ns
$t_{SFS}$	$\overline{CS}$ high after SCLK edge	0			ns

<sup>1</sup>  $t_{UCLK} = 23.9$  ns. It corresponds to the 41.78 MHz internal clock from the PLL before the clock divider; see Figure 67.

<sup>2</sup>  $t_{HCLK}$  depends on the clock divider or CD bits in the POWCONMMR.  $t_{HCLK} = t_{UCLK}/2^{CD}$ ; see Figure 67.

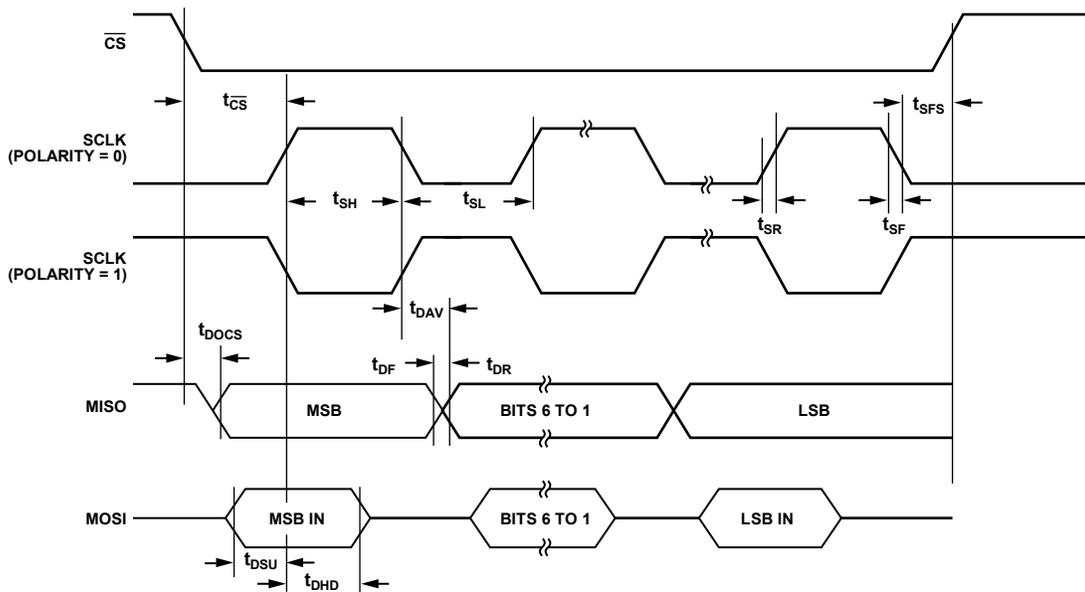
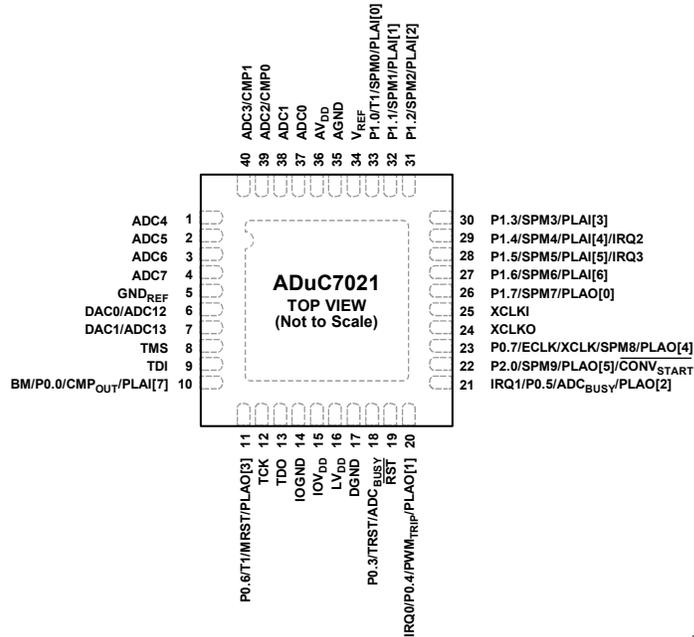


Figure 18. SPI Slave Mode Timing (Phase Mode = 0)

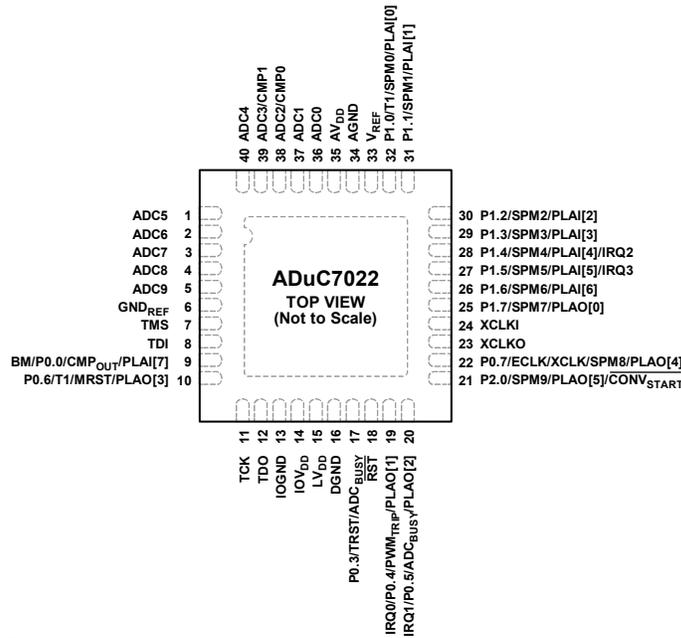
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NOTES  
 1. THE EXPOSED PAD MUST BE SOLDERED FOR MECHANICAL PURPOSES AND LEFT UNCONNECTED.

04985-065

Figure 21. 40-Lead LFCSP\_WQ Pin Configuration (ADuC7021)



NOTES  
 1. THE EXPOSED PAD MUST BE SOLDERED FOR MECHANICAL PURPOSES AND LEFT UNCONNECTED.

04985-066

Figure 22. 40-Lead LFCSP\_WQ Pin Configuration (ADuC7022)

Pin No.	Mnemonic	Description
E1	TMS	JTAG Test Port Input, Test Mode Select. Debug and download access.
E2	BM/P0.0/CMP <sub>OUT</sub> /PLAI[7]	Multifunction I/O Pin. Boot mode. The ADuC7029 enters UART download mode if BM is low at reset and executes code if BM is pulled high at reset through a 1 kΩ resistor/General-Purpose Input and Output Port 0.0/Voltage Comparator Output/Programmable Logic Array Input Element 7.
E3	DAC2/ADC14	DAC2 Voltage Output/ADC Input 14.
E4	IOV <sub>DD</sub>	3.3 V Supply for GPIO (see Table 78) and Input of the On-Chip Voltage Regulator.
E5	P3.2/PWM1 <sub>H</sub> /PLAI[10]	General-Purpose Input and Output Port 3.2/PWM Phase 1 High-Side Output/Programmable Logic Array Input Element 10.
E6	P3.5/PWM2 <sub>L</sub> /PLAI[13]	General-Purpose Input and Output Port 3.5/PWM Phase 2 Low-Side Output/Programmable Logic Array Input Element 13.
E7	P0.7/ECLK/XCLK/SPM8/PLAO[4]	Serial Port Multiplexed. General-Purpose Input and Output Port 0.7/Output for External Clock Signal/Input to the Internal Clock Generator Circuits/UART/Programmable Logic Array Output Element 4.
F1	TDI	JTAG Test Port Input, Test Data In. Debug and download access.
F2	P0.6/T1/MRST/PLAO[3]	Multifunction Pin, Driven Low After Reset. General-Purpose Output Port 0.6/Timer1 Input/Power-On Reset Output/Programmable Logic Array Output Element 3.
F3	IOGND	Ground for GPIO (see Table 78). Typically connected to DGND.
F4	P3.1/PWM0 <sub>L</sub> /PLAI[9]	General-Purpose Input and Output Port 3.1/PWM Phase 0 Low-Side Output/Programmable Logic Array Input Element 9.
F5	P3.0/PWM0 <sub>H</sub> /PLAI[8]	General-Purpose Input and Output Port 3.0/PWM Phase 0 High-Side Output/Programmable Logic Array Input Element 8.
F6	$\overline{\text{RST}}$	Reset Input, Active Low.
F7	P2.0/SPM9/PLAO[5]/CONV <sub>START</sub>	Serial Port Multiplexed. General-Purpose Input and Output Port 2.0/UART/Programmable Logic Array Output Element 5/Start Conversion Input Signal for ADC.
G1	TCK	JTAG Test Port Input, Test Clock. Debug and download access.
G2	TDO	JTAG Test Port Output, Test Data Out. Debug and download access.
G3	LV <sub>DD</sub>	2.6 V Output of the On-Chip Voltage Regulator. This output must be connected to a 0.47 μF capacitor to DGND only.
G4	DGND	Ground for Core Logic.
G5	P0.3/TRST/ADC <sub>BUSY</sub>	General-Purpose Input and Output Port 0.3/JTAG Test Port Input, Test Reset/ADC <sub>BUSY</sub> Signal Output.
G6	IRQ0/P0.4/PWM <sub>TRIP</sub> /PLAO[1]	Multifunction I/O Pin. External Interrupt Request 0, Active High/General-Purpose Input and Output Port 0.4/PWM Trip External Input/Programmable Logic Array Output Element 1.
G7	IRQ1/P0.5/ADC <sub>BUSY</sub> /PLAO[2]	Multifunction I/O Pin. External Interrupt Request 1, Active High/General-Purpose Input and Output Port 0.5/ADC <sub>BUSY</sub> Signal Output/Programmable Logic Array Output Element 2.

**Table 22. ADCCN MMR Bit Designation**

Bit	Value	Description
7:5		Reserved.
4:0		Negative channel selection bits.
	00000	ADC0.
	00001	ADC1.
	00010	ADC2.
	00011	ADC3.
	00100	ADC4.
	00101	ADC5.
	00110	ADC6.
	00111	ADC7.
	01000	ADC8.
	01001	ADC9.
	01010	ADC10.
	01011	ADC11.
	01100	DAC0/ADC12.
	01101	DAC1/ADC13.
	01110	DAC2/ADC14.
	01111	DAC3/ADC15.
	10000	Internal reference (self-diagnostic feature).
	Others	Reserved.

**Table 23. ADCSTA Register**

Name	Address	Default Value	Access
ADCSTA	0xFFFF050C	0x00	R

ADCSTA is an ADC status register that indicates when an ADC conversion result is ready. The ADCSTA register contains only one bit, ADCReady (Bit 0), representing the status of the ADC. This bit is set at the end of an ADC conversion, generating an ADC interrupt. It is cleared automatically by reading the ADCDAT MMR. When the ADC is performing a conversion, the status of the ADC can be read externally via the ADC<sub>BUSY</sub> pin. This pin is high during a conversion. When the conversion is finished, ADC<sub>BUSY</sub> goes back low. This information can be available on P0.5 (see the General-Purpose Input/Output section) if enabled in the ADCCON register.

**Table 24. ADCDAT Register**

Name	Address	Default Value	Access
ADCDAT	0xFFFF0510	0x00000000	R

ADCDAT is an ADC data result register. It holds the 12-bit ADC result as shown in Figure 51.

**Table 25. ADCRST Register**

Name	Address	Default Value	Access
ADCRST	0xFFFF0514	0x00	R/W

ADCRST resets the digital interface of the ADC. Writing any value to this register resets all the ADC registers to their default values.

**Table 26. ADCGN Register**

Name	Address	Default Value	Access
ADCGN	0xFFFF0530	0x0200	R/W

ADCGN is a 10-bit gain calibration register.

**Table 27. ADCOF Register**

Name	Address	Default Value	Access
ADCOF	0xFFFF0534	0x0200	R/W

ADCOF is a 10-bit offset calibration register.

## CONVERTER OPERATION

The ADC incorporates a successive approximation (SAR) architecture involving a charge-sampled input stage. This architecture can operate in three modes: differential, pseudo differential, and single-ended.

### Differential Mode

The ADuC7019/20/21/22/24/25/26/27/28/29 each contain a successive approximation ADC based on two capacitive DACs. Figure 54 and Figure 55 show simplified schematics of the ADC in acquisition and conversion phase, respectively. The ADC comprises control logic, a SAR, and two capacitive DACs. In Figure 54 (the acquisition phase), SW3 is closed and SW1 and SW2 are in Position A. The comparator is held in a balanced condition, and the sampling capacitor arrays acquire the differential signal on the input.

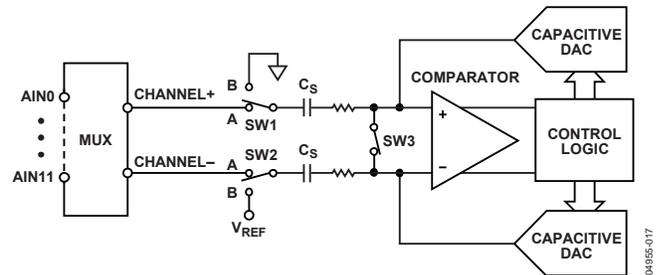


Figure 54. ADC Acquisition Phase

When the ADC starts a conversion, as shown in Figure 55, SW3 opens, and then SW1 and SW2 move to Position B. This causes the comparator to become unbalanced. Both inputs are disconnected once the conversion begins. The control logic and the charge redistribution DACs are used to add and subtract fixed amounts of charge from the sampling capacitor arrays to bring the comparator back into a balanced condition. When the comparator is rebalanced, the conversion is complete. The control logic generates the ADC output code. The output impedances of the sources driving the  $V_{IN+}$  and  $V_{IN-}$  input voltage pins must be matched; otherwise, the two inputs have different settling times, resulting in errors.

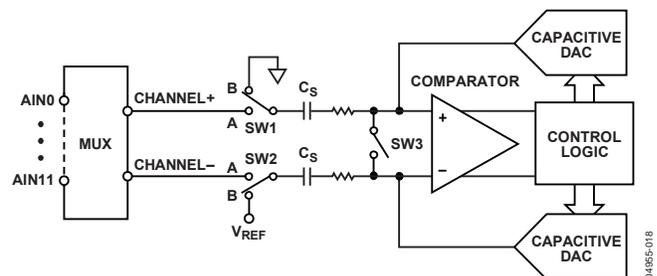


Figure 55. ADC Conversion Phase

## SECURITY

The 62 kB of Flash/EE memory available to the user can be read and write protected.

Bit 31 of the FEEP/EEHIDE MMR (see Table 42) protects the 62 kB from being read through JTAG programming mode. The other 31 bits of this register protect writing to the flash memory. Each bit protects four pages, that is, 2 kB. Write protection is activated for all types of access.

### Three Levels of Protection

- Protection can be set and removed by writing directly into FEEHIDE MMR. This protection does not remain after reset.
- Protection can be set by writing into the FEEP/EE MMR. It takes effect only after a save protection command (0x0C) and a reset. The FEEP/EE MMR is protected by a key to avoid direct access. The key is saved once and must be entered again to modify FEEP/EE. A mass erase sets the key back to 0xFFFF but also erases all the user code.
- Flash can be permanently protected by using the FEEP/EE MMR and a particular value of key: 0xDEADDEAD. Entering the key again to modify the FEEP/EE register is not allowed.

### Sequence to Write the Key

1. Write the bit in FEEP/EE corresponding to the page to be protected.
2. Enable key protection by setting Bit 6 of FEEMOD (Bit 5 must equal 0).
3. Write a 32-bit key in FEEADR and FEEDAT.
4. Run the write key command 0x0C in FEECON; wait for the read to be successful by monitoring FEESTA.
5. Reset the part.

To remove or modify the protection, the same sequence is used with a modified value of FEEP/EE. If the key chosen is the value 0xDEAD, the memory protection cannot be removed. Only a mass erase unprotects the part, but it also erases all user code.

The sequence to write the key is illustrated in the following example (this protects writing Page 4 to Page 7 of the Flash):

```
FEEP/EE=0xFFFFFFFF; //Protect pages 4 to 7
FEEMOD=0x48; //Write key enable
FEEADR=0x1234; //16 bit key value
FEEDAT=0x5678; //16 bit key value
FEECON= 0x0C; // Write key command
```

The same sequence should be followed to protect the part permanently with FEEADR = 0xDEAD and FEEDAT = 0xDEAD.

## FLASH/EE CONTROL INTERFACE

Serial and JTAG programming use the Flash/EE control interface, which includes the eight MMRs outlined in this section.

**Table 31. FEESTA Register**

Name	Address	Default Value	Access
FEESTA	0xFFFFF800	0x20	R

FEESTA is a read-only register that reflects the status of the flash control interface as described in Table 32.

**Table 32. FEESTA MMR Bit Designations**

Bit	Description
15:6	Reserved.
5	Reserved.
4	Reserved.
3	Flash interrupt status bit. Set automatically when an interrupt occurs, that is, when a command is complete and the Flash/EE interrupt enable bit in the FEEMOD register is set. Cleared when reading the FEESTA register.
2	Flash/EE controller busy. Set automatically when the controller is busy. Cleared automatically when the controller is not busy.
1	Command fail. Set automatically when a command completes unsuccessfully. Cleared automatically when reading the FEESTA register.
0	Command pass. Set by the MicroConverter when a command completes successfully. Cleared automatically when reading the FEESTA register.

**Table 33. FEEMOD Register**

Name	Address	Default Value	Access
FEEMOD	0xFFFFF804	0x0000	R/W

FEEMOD sets the operating mode of the flash control interface. Table 34 shows FEEMOD MMR bit designations.

**Table 34. FEEMOD MMR Bit Designations**

Bit	Description
15:9	Reserved.
8	Reserved. This bit should always be set to 0.
7:5	Reserved. These bits should always be set to 0 except when writing keys. See the Sequence to Write the Key section.
4	Flash/EE interrupt enable. Set by user to enable the Flash/EE interrupt. The interrupt occurs when a command is complete. Cleared by user to disable the Flash/EE interrupt.
3	Erase/write command protection. Set by user to enable the erase and write commands. Cleared to protect the Flash against the erase/write command.
2:0	Reserved. These bits should always be set to 0.

**Example source code**

```

t2val_old= T2VAL;
T2LD = 5;
TCON = 0x480;

while ((T2VAL == t2val_old) || (T2VAL >
3)) //ensures timer value loaded
    IRQEN = 0x10;
//enable T2 interrupt
PLLKEY1 = 0xAA;
PLLCON = 0x01;
PLLKEY2 = 0x55;

POWKEY1 = 0x01;
POWCON = 0x27;
// Set Core into Nap mode
POWKEY2 = 0xF4;

```

In noisy environments, noise can couple to the external crystal pins, and PLL may lose lock momentarily. A PLL interrupt is provided in the interrupt controller. The core clock is immediately halted, and this interrupt is only serviced when the lock is restored.

In case of crystal loss, the watchdog timer should be used. During initialization, a test on the RSTSTA register can determine if the reset came from the watchdog timer.

**External Clock Selection**

To switch to an external clock on P0.7, configure P0.7 in Mode 1. The external clock can be up to 44 MHz, providing the tolerance is 1%.

**Table 57. Operating Modes<sup>1</sup>**

Mode	Core	Peripherals	PLL	XTAL/T2/T3	IRQ0 to IRQ3	Start-Up/Power-On Time
Active	X	X	X	X	X	130 ms at CD = 0
Pause		X	X	X	X	24 ns at CD = 0; 3 μs at CD = 7
Nap			X	X	X	24 ns at CD = 0; 3 μs at CD = 7
Sleep				X	X	1.58 ms
Stop					X	1.7 ms

<sup>1</sup> X indicates that the part is powered on.

**Table 58. Typical Current Consumption at 25°C in Milliampere**

PC[2:0]	Mode	CD = 0	CD = 1	CD = 2	CD = 3	CD = 4	CD = 5	CD = 6	CD = 7
000	Active	33.1	21.2	13.8	10	8.1	7.2	6.7	6.45
001	Pause	22.7	13.3	8.5	6.1	4.9	4.3	4	3.85
010	Nap	3.8	3.8	3.8	3.8	3.8	3.8	3.8	3.8
011	Sleep	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4
100	Stop	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4

**Example source code**

```

t2val_old= T2VAL;
T2LD = 5;
TCON = 0x480;

while ((T2VAL == t2val_old) || (T2VAL >
3)) //ensures timer value loaded
    IRQEN = 0x10;
//enable T2 interrupt
PLLKEY1 = 0xAA;
PLLCON = 0x03; //Select external clock
PLLKEY2 = 0x55;

POWKEY1 = 0x01;
POWCON = 0x27;
// Set Core into Nap mode
POWKEY2 = 0xF4;

```

**Power Control System**

A choice of operating modes is available on the ADuC7019/20/21/22/24/25/26/27/28/29. Table 57 describes what part is powered on in the different modes and indicates the power-up time.

Table 58 gives some typical values of the total current consumption (analog + digital supply currents) in the different modes, depending on the clock divider bits. The ADC is turned off. Note that these values also include current consumption of the regulator and other parts on the test board where these values are measured.

**MMRs and Keys**

The operating mode, clocking mode, and programmable clock divider are controlled via two MMRs: PLLCON (see Table 61) and POWCON (see Table 64). PLLCON controls the operating mode of the clock system, whereas POWCON controls the core clock frequency and the power-down mode.

To prevent accidental programming, a certain sequence (see Table 65) must be followed to write to the PLLCON and POWCON registers.

**Table 59. PLLKEYx Registers**

Name	Address	Default Value	Access
PLLKEY1	0xFFFF0410	0x0000	W
PLLKEY2	0xFFFF0418	0x0000	W

**Table 60. PLLCON Register**

Name	Address	Default Value	Access
PLLCON	0xFFFF0414	0x21	R/W

**Table 61. PLLCON MMR Bit Designations**

Bit	Name	Value	Description
7:6			Reserved.
5	OSEL		32 kHz PLL input selection. Set by user to select the internal 32 kHz oscillator. Set by default. Cleared by user to select the external 32 kHz crystal.
4:2			Reserved.
1:0	MDCLK	00 01 10 11	Clocking modes. Reserved. PLL. Default configuration. Reserved. External clock on the P0.7 pin.

**Table 62. POWKEYx Registers**

Name	Address	Default Value	Access
POWKEY1	0xFFFF0404	0x0000	W
POWKEY2	0xFFFF040C	0x0000	W

**Table 63. POWCON Register**

Name	Address	Default Value	Access
POWCON	0xFFFF0408	0x0003	R/W

**Table 64. POWCON MMR Bit Designations**

Bit	Name	Value	Description
7			Reserved.
6:4	PC	000 001 010 011  100  Others	Operating modes. Active mode. Pause mode. Nap. Sleep mode. IRQ0 to IRQ3 and Timer2 can wake up the part. Stop mode. IRQ0 to IRQ3 can wake up the part. Reserved.
3			Reserved.
2:0	CD	000 001 010 011 100 101 110 111	CPU clock divider bits. 41.78 MHz. 20.89 MHz. 10.44 MHz. 5.22 MHz. 2.61 MHz. 1.31 MHz. 653 kHz. 326 kHz.

**Table 65. PLLCON and POWCON Write Sequence**

PLLCON	POWCON
PLLKEY1 = 0xAA	POWKEY1 = 0x01
PLLCON = 0x01	POWCON = user value
PLLKEY2 = 0x55	POWKEY2 = 0xF4

## DIGITAL PERIPHERALS

### 3-PHASE PWM

Each ADuC7019/20/21/22/24/25/26/27/28/29 provides a flexible and programmable, 3-phase pulse-width modulation (PWM) waveform generator. It can be programmed to generate the required switching patterns to drive a 3-phase voltage source inverter for ac induction motor control (ACIM). Note that only active high patterns can be produced.

The PWM generator produces three pairs of PWM signals on the six PWM output pins (PWM0<sub>H</sub>, PWM0<sub>L</sub>, PWM1<sub>H</sub>, PWM1<sub>L</sub>, PWM2<sub>H</sub>, and PWM2<sub>L</sub>). The six PWM output signals consist of three high-side drive signals and three low-side drive signals.

The switching frequency and dead time of the generated PWM patterns are programmable using the PWMDAT0 and PWMDAT1 MMRs. In addition, three duty-cycle control registers (PWMCH0, PWMCH1, and PWMCH2) directly control the duty cycles of the three pairs of PWM signals.

Each of the six PWM output signals can be enabled or disabled by separate output enable bits of the PWMEN register. In addition, three control bits of the PWMEN register permit crossover of the two signals of a PWM pair. In crossover mode, the PWM signal destined for the high-side switch is diverted to the complementary low-side output. The signal destined for the low-side switch is diverted to the corresponding high-side output signal.

In many applications, there is a need to provide an isolation barrier in the gate-drive circuits that turn on the inverter power devices. In general, there are two common isolation techniques: optical isolation using optocouplers and transformer isolation using pulse transformers. The PWM controller permits mixing of the output PWM signals with a high frequency chopping signal to permit easy interface to such pulse transformers. The features of this gate-drive chopping mode can be controlled by the PWMCFG register. An 8-bit value within the PWMCFG register directly controls the chopping frequency. High frequency chopping can be independently enabled for the high-side and low-side outputs using separate control bits in the PWMCFG register.

The PWM generator can operate in one of two distinct modes: single update mode or double update mode. In single update mode, the duty cycle values are programmable only once per PWM period so that the resulting PWM patterns are symmetrical about the midpoint of the PWM period. In the double update mode, a second updating of the PWM duty cycle values is implemented at the midpoint of the PWM period.

In double update mode, it is also possible to produce asymmetrical PWM patterns that produce lower harmonic distortion in 3-phase PWM inverters. This technique permits closed-loop controllers to change the average voltage applied to the machine windings at a faster rate. As a result, faster closed-loop bandwidths are achieved. The operating mode of the PWM block is selected by a control bit in the PWMCON register. In single update mode,

an internal synchronization pulse, PWMSYNC, is produced at the start of each PWM period. In double update mode, an additional PWMSYNC pulse is produced at the midpoint of each PWM period.

The PWM block can also provide an internal synchronization pulse on the PWM<sub>SYNC</sub> pin that is synchronized to the PWM switching frequency. In single update mode, a pulse is produced at the start of each PWM period. In double update mode, an additional pulse is produced at the mid-point of each PWM period. The width of the pulse is programmable through the PWMDAT2 register. The PWM block can also accept an external synchronization pulse on the PWM<sub>SYNC</sub> pin. The selection of external synchronization or internal synchronization is in the PWMCON register. The SYNC input timing can be synchronized to the internal peripheral clock, which is selected in the PWMCON register. If the external synchronization pulse from the chip pin is asynchronous to the internal peripheral clock (typical case), the external PWMSYNC is considered asynchronous and should be synchronized. The synchronization logic adds latency and jitter from the external pulse to the actual PWM outputs. The size of the pulse on the PWM<sub>SYNC</sub> pin must be greater than two core clock periods.

The PWM signals produced by the ADuC7019/20/21/22/24/25/26/27/28/29 can be shut off via a dedicated asynchronous PWM shutdown pin, PWM<sub>TRIP</sub>. When brought low, PWM<sub>TRIP</sub> instantaneously places all six PWM outputs in the off state (high). This hardware shutdown mechanism is asynchronous so that the associated PWM disable circuitry does not go through any clocked logic. This ensures correct PWM shutdown even in the event of a core clock loss.

Status information about the PWM system is available to the user in the PWMSTA register. In particular, the state of the PWM<sub>TRIP</sub> pin is available, as well as a status bit that indicates whether operation is in the first half or the second half of the PWM period.

### 40-Pin Package Devices

On the 40-pin package devices, the PWM outputs are not directly accessible, as described in the General-Purpose Input/Output section. One channel can be brought out on a GPIO (see Table 78) via the PLA as shown in the following example:

```
PWMCON = 0x1;           // enables PWM o/p
PWMDAT0 = 0x055F;      // PWM switching freq
// Configure Port Pins
GP4CON = 0x300;        // P4.2 as PLA output
GP3CON = 0x1;          // P3.0 configured as
                       // output of PWM0
                       // (internally)

// PWM0 onto P4.2
PLAELM8 = 0x0035;     // P3.0 (PWM output)
                       // input of element 8
PLAELM10 = 0x0059;    // PWM from element 8
```

Both switching edges are moved by an equal amount ( $PWMDAT1 \times t_{CORE}$ ) to preserve the symmetrical output patterns.

Also shown are the PWMSYNC pulse and Bit 0 of the PWMSTA register, which indicates whether operation is in the first or second half cycle of the PWM period.

The resulting on times of the PWM signals over the full PWM period (two half periods) produced by the timing unit can be written as follows:

On the high side

$$t_{0HH} = PWMDAT0 + 2(PWMCH0 - PWMDAT1) \times t_{CORE}$$

$$t_{0HL} = PWMDAT0 - 2(PWMCH0 - PWMDAT1) \times t_{CORE}$$

and the corresponding duty cycles ( $d$ )

$$d_{0H} = t_{0HH}/t_s = \frac{1}{2} + (PWMCH0 - PWMDAT1)/PWMDAT0$$

and on the low side

$$t_{0LH} = PWMDAT0 - 2(PWMCH0 + PWMDAT1) \times t_{CORE}$$

$$t_{0LL} = PWMDAT0 + 2(PWMCH0 + PWMDAT1) \times t_{CORE}$$

and the corresponding duty cycles ( $d$ )

$$d_{0L} = t_{0LH}/t_s = \frac{1}{2} - (PWMCH0 + PWMDAT1)/PWMDAT0$$

The minimum permissible  $t_{0H}$  and  $t_{0L}$  values are zero, corresponding to a 0% duty cycle. In a similar fashion, the maximum value is  $t_s$ , corresponding to a 100% duty cycle.

Figure 70 shows the output signals from the timing unit for operation in double update mode. It illustrates a general case where the switching frequency, dead time, and duty cycle are all changed in the second half of the PWM period. The same value for any or all of these quantities can be used in both halves of the PWM cycle. However, there is no guarantee that symmetrical PWM signals are produced by the timing unit in double update mode. Figure 70 also shows that the dead time insertions into the PWM signals are done in the same way as in single update mode.

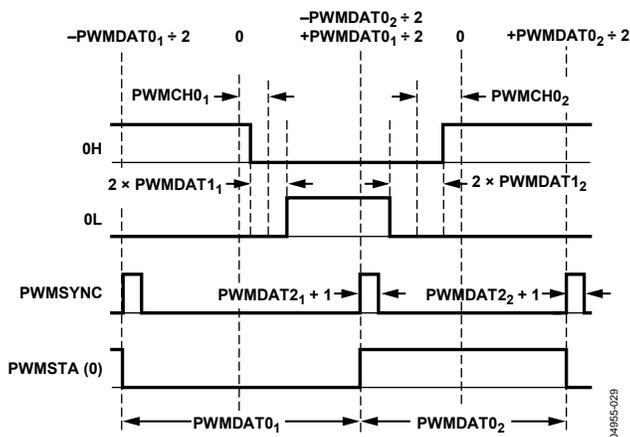


Figure 70. Typical PWM Outputs of the 3-Phase Timing Unit (Double Update Mode)

In general, the on times of the PWM signals in double update mode can be defined as follows:

On the high side

$$t_{0HH} = (PWMDAT0_1/2 + PWMDAT0_2/2 + PWMCH0_1 + PWMCH0_2 - PWMDAT1_1 - PWMDAT1_2) \times t_{CORE}$$

$$t_{0HL} = (PWMDAT0_1/2 + PWMDAT0_2/2 - PWMCH0_1 - PWMCH0_2 + PWMDAT1_1 + PWMDAT1_2) \times t_{CORE}$$

where Subscript 1 refers to the value of that register during the first half cycle, and Subscript 2 refers to the value during the second half cycle.

The corresponding duty cycles ( $d$ ) are

$$d_{0H} = t_{0HH}/t_s = (PWMDAT0_1/2 + PWMDAT0_2/2 + PWMCH0_1 + PWMCH0_2 - PWMDAT1_1 - PWMDAT1_2)/(PWMDAT0_1 + PWMDAT0_2)$$

On the low side

$$t_{0LH} = (PWMDAT0_1/2 + PWMDAT0_2/2 + PWMCH0_1 + PWMCH0_2 + PWMDAT1_1 + PWMDAT1_2) \times t_{CORE}$$

$$t_{0LL} = (PWMDAT0_1/2 + PWMDAT0_2/2 - PWMCH0_1 - PWMCH0_2 - PWMDAT1_1 - PWMDAT1_2) \times t_{CORE}$$

where Subscript 1 refers to the value of that register during the first half cycle, and Subscript 2 refers to the value during the second half cycle.

The corresponding duty cycles ( $d$ ) are

$$d_{0L} = t_{0LH}/t_s = (PWMDAT0_1/2 + PWMDAT0_2/2 + PWMCH0_1 + PWMCH0_2 + PWMDAT1_1 + PWMDAT1_2)/(PWMDAT0_1 + PWMDAT0_2)$$

For the completely general case in double update mode (see Figure 70), the switching period is given by

$$t_s = (PWMDAT0_1 + PWMDAT0_2) \times t_{CORE}$$

Again, the values of  $t_{0H}$  and  $t_{0L}$  are constrained to lie between zero and  $t_s$ .

PWM signals similar to those illustrated in Figure 69 and Figure 70 can be produced on the 1H, 1L, 2H, and 2L outputs by programming the PWMCH1 and PWMCH2 registers in a manner identical to that described for PWMCH0. The PWM controller does not produce any PWM outputs until all of the PWMDAT0, PWMCH0, PWMCH1, and PWMCH2 registers have been written to at least once. When these registers are written, internal counting of the timers in the 3-phase timing unit is enabled.

Writing to the PWMDAT0 register starts the internal timing of the main PWM timer. Provided that the PWMDAT0 register is written to prior to the PWMCH0, PWMCH1, and PWMCH2 registers in the initialization, the first PWMSYNC pulse and interrupt (if enabled) appear  $1.5 \times t_{CORE} \times PWMDAT0$  seconds after the initial write to the PWMDAT0 register in single update mode. In double update mode, the first PWMSYNC pulse appears after  $PWMDAT0 \times t_{CORE}$  seconds.

Table 70. PWMCFG Register

Name	Address	Default Value	Access
PWMCFG	0xFFFFFC10	0x0000	R/W

PWMCFG is a gate chopping register.

Table 71. PWMCFG MMR Bit Descriptions

Bit	Name	Description
15:10		Reserved.
9	CHOPLO	Low-side gate chopping enable bit.
8	CHOPHI	High-side gate chopping enable bit.
7:0	GDCLK	PWM gate chopping period (unsigned).

Table 72. PWMEN Register

Name	Address	Default Value	Access
PWMEN	0xFFFFFC20	0x0000	R/W

PWMEN allows enabling of channel outputs and crossover. See its bit definitions in Table 73.

Table 73. PWMEN MMR Bit Descriptions

Bit	Name	Description
8	0H0L_XOVR	Channel 0 output crossover enable bit. Set to 1 by user to enable Channel 0 output crossover. Cleared to 0 by user to disable Channel 0 output crossover.
7	1H1L_XOVR	Channel 1 output crossover enable bit. Set to 1 by user to enable Channel 1 output crossover. Cleared to 0 by user to disable Channel 1 output crossover.
6	2H2L_XOVR	Channel 2 output crossover enable bit. Set to 1 by user to enable Channel 2 output crossover. Cleared to 0 by user to disable Channel 2 output crossover.
5	0L_EN	0L output enable bit. Set to 1 by user to disable the 0L output of the PWM. Cleared to 0 by user to enable the 0L output of the PWM.
4	0H_EN	0H output enable bit. Set to 1 by user to disable the 0H output of the PWM. Cleared to 0 by user to enable the 0H output of the PWM.
3	1L_EN	1L output enable bit. Set to 1 by user to disable the 1L output of the PWM. Cleared to 0 by user to enable the 1L output of the PWM.
2	1H_EN	1H Output Enable Bit. Set to 1 by user to disable the 1H output of the PWM. Cleared to 0 by user to enable the 1H output of the PWM.
1	2L_EN	2L output enable bit. Set to 1 by user to disable the 2L output of the PWM. Cleared to 0 by user to enable the 2L output of the PWM.
0	2H_EN	2H output enable bit. Set to 1 by user to disable the 2H output of the PWM. Cleared to 0 by user to enable the 2H output of the PWM.

Table 74. PWMDAT0 Register

Name	Address	Default Value	Access
PWMDAT0	0xFFFFFC08	0x0000	R/W

PWMDAT0 is an unsigned 16-bit register for switching period.

Table 75. PWMDAT1 Register

Name	Address	Default Value	Access
PWMDAT1	0xFFFFFC0C	0x0000	R/W

PWMDAT1 is an unsigned 10-bit register for dead time.

Table 76. PWMCHx Registers

Name	Address	Default Value	Access
PWMCH0	0xFFFFFC14	0x0000	R/W
PWMCH1	0xFFFFFC18	0x0000	R/W
PWMCH2	0xFFFFFC1C	0x0000	R/W

PWMCH0, PWMCH1, and PWMCH2 are channel duty cycles for the three phases.

Table 77. PWMDAT2 Register

Name	Address	Default Value	Access
PWMDAT2	0xFFFFFC24	0x0000	R/W

PWMDAT2 is an unsigned 10-bit register for PWM sync pulse width.

## GENERAL-PURPOSE INPUT/OUTPUT

The [ADuC7019/20/21/22/24/25/26/27/28/29](#) provide 40 general-purpose, bidirectional I/O (GPIO) pins. All I/O pins are 5 V tolerant, meaning the GPIOs support an input voltage of 5 V.

In general, many of the GPIO pins have multiple functions (see Table 78 for the pin function definitions). By default, the GPIO pins are configured in GPIO mode.

All GPIO pins have an internal pull-up resistor (of about 100 kΩ), and their drive capability is 1.6 mA. Note that a maximum of 20 GPIOs can drive 1.6 mA at the same time. Using the GPxPAR registers, it is possible to enable/disable the pull-up resistors for the following ports: P0.0, P0.4, P0.5, P0.6, P0.7, and the eight GPIOs of P1.

The 40 GPIOs are grouped in five ports, Port 0 to Port 4 (Port x). Each port is controlled by four or five MMRs.

Note that the kernel changes P0.6 from its default configuration at reset (MRST) to GPIO mode. If MRST is used for external circuitry, an external pull-up resistor should be used to ensure that the level on P0.6 does not drop when the kernel switches mode. Otherwise, P0.6 goes low for the reset period. For example, if MRST is required for power-down, it can be reconfigured in GPOCON MMR.

The input level of any GPIO can be read at any time in the GPxDAT MMR, even when the pin is configured in a mode other than GPIO. The PLA input is always active.

When the [ADuC7019/20/21/22/24/25/26/27/28/29](#) part enters a power-saving mode, the GPIO pins retain their state.

Table 140. I2CxDIV Registers

Name	Address	Default Value	Access
I2C0DIV	0xFFFF0830	0x1F1F	R/W
I2C1DIV	0xFFFF0930	0x1F1F	R/W

I2CxDIV are the clock divider registers.

Table 141. I2CxIDx Registers

Name	Address	Default Value	Access
I2C0ID0	0xFFFF0838	0x00	R/W
I2C0ID1	0xFFFF083C	0x00	R/W
I2C0ID2	0xFFFF0840	0x00	R/W
I2C0ID3	0xFFFF0844	0x00	R/W
I2C1ID0	0xFFFF0938	0x00	R/W
I2C1ID1	0xFFFF093C	0x00	R/W
I2C1ID2	0xFFFF0940	0x00	R/W
I2C1ID3	0xFFFF0944	0x00	R/W

I2CxID0, I2CxID1, I2CxID2, and I2CxID3 are slave address device ID registers of I2Cx.

Table 142. I2CxCCNT Registers

Name	Address	Default Value	Access
I2C0CCNT	0xFFFF0848	0x01	R/W
I2C1CCNT	0xFFFF0948	0x01	R/W

I2CxCCNT are 8-bit start/stop generation counters. They hold off SDA low for start and stop conditions.

Table 143. I2CxFSTA Registers

Name	Address	Default Value	Access
I2C0FSTA	0xFFFF084C	0x0000	R/W
I2C1FSTA	0xFFFF094C	0x0000	R/W

I2CxFSTA are FIFO status registers.

Table 144. I2C0FSTA MMR Bit Descriptions

Bit	Access Type	Value	Description
15:10			Reserved.
9	R/W		Master transmit FIFO flush. Set by the user to flush the master Tx FIFO. Cleared automatically when the master Tx FIFO is flushed. This bit also flushes the slave receive FIFO.
8	R/W		Slave transmit FIFO flush. Set by the user to flush the slave Tx FIFO. Cleared automatically after the slave Tx FIFO is flushed.
7:6	R	00 01 10 11	Master Rx FIFO status bits. FIFO empty. Byte written to FIFO. One byte in FIFO. FIFO full.
5:4	R	00 01 10 11	Master Tx FIFO status bits. FIFO empty. Byte written to FIFO. One byte in FIFO. FIFO full.
3:2	R	00 01 10 11	Slave Rx FIFO status bits. FIFO empty. Byte written to FIFO. One byte in FIFO. FIFO full.
1:0	R	00 01 10 11	Slave Tx FIFO status bits. FIFO empty. Byte written to FIFO. One byte in FIFO. FIFO full.

Table 153. PLAADC Register

Name	Address	Default Value	Access
PLAADC	0xFFFF0B48	0x00000000	R/W

PLAADC is the PLA source for the ADC start conversion signal.

Table 154. PLAADC MMR Bit Descriptions

Bit	Value	Description
31:5		Reserved.
4		ADC start conversion enable bit. Set by user to enable ADC start conversion from PLA. Cleared by user to disable ADC start conversion from PLA.
3:0		ADC start conversion source.
	0000	PLA Element 0.
	0001	PLA Element 1.
	1111	PLA Element 15.

Table 155. PLADIN Register

Name	Address	Default Value	Access
PLADIN	0xFFFF0B4C	0x00000000	R/W

PLADIN is a data input MMR for PLA.

Table 156. PLADIN MMR Bit Descriptions

Bit	Description
31:16	Reserved.
15:0	Input bit to Element 15 to Element 0.

Table 157. PLADOUT Register

Name	Address	Default Value	Access
PLADOUT	0xFFFF0B50	0x00000000	R

PLADOUT is a data output MMR for PLA. This register is always updated.

Table 158. PLADOUT MMR Bit Descriptions

Bit	Description
31:16	Reserved.
15:0	Output bit from Element 15 to Element 0.

Table 159. PLALCK Register

Name	Address	Default Value	Access
PLALCK	0xFFFF0B54	0x00	W

PLALCK is a PLA lock option. Bit 0 is written only once. When set, it does not allow modifying any of the PLA MMRs, except PLADIN. A PLA tool is provided in the development system to easily configure the PLA.

In normal mode, an IRQ is generated each time the value of the counter reaches zero when counting down. It is also generated each time the counter value reaches full scale when counting up. An IRQ can be cleared by writing any value to clear the register of that particular timer (TxCLRI).

When using an asynchronous clock-to-clock timer, the interrupt in the timer block may take more time to clear than the time it takes for the code in the interrupt routine to execute. Ensure that the interrupt signal is cleared before leaving the interrupt service routine. This can be done by checking the IRQSTA MMR.

**Hour:Minute:Second:1/128 Format**

To use the timer in hour:minute:second:hundredths format, select the 32,768 kHz clock and prescaler of 256. The hundredths field does not represent milliseconds but 1/128 of a second (256/32,768). The bits representing the hour, minute, and second are not consecutive in the register. This arrangement applies to TxLD and TxVAL when using the hour:minute:second:hundredths format as set in TxCON[5:4]. See Table 171 for additional details.

**Table 171. Hour:Minnute:Second:Hundredths Format**

Bit	Value	Description
31:24	0 to 23 or 0 to 255	Hours
23:22	0	Reserved
21:16	0 to 59	Minutes
15:14	0	Reserved
13:8	0 to 59	Seconds
7	0	Reserved
6:0	0 to 127	1/128 second

**Timer0 (RTOS Timer)**

Timer0 is a general-purpose, 16-bit timer (count down) with a programmable prescaler (see Figure 77). The prescaler source is the core clock frequency (HCLK) and can be scaled by factors of 1, 16, or 256.

Timer0 can be used to start ADC conversions as shown in the block diagram in Figure 77.

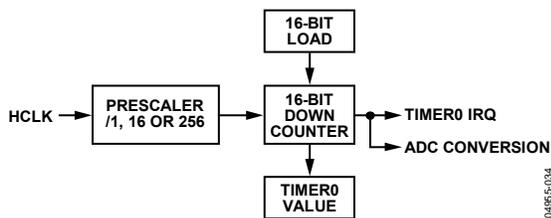


Figure 77. Timer0 Block Diagram

The Timer0 interface consists of four MMRs: T0LD, T0VAL, T0CON, and T0CLRI.

**Table 172. T0LD Register**

Name	Address	Default Value	Access
T0LD	0xFFFF0300	0x0000	R/W

T0LD is a 16-bit load register.

**Table 173. T0VAL Register**

Name	Address	Default Value	Access
T0VAL	0xFFFF0304	0xFFFF	R

T0VAL is a 16-bit read-only register representing the current state of the counter.

**Table 174. T0CON Register**

Name	Address	Default Value	Access
T0CON	0xFFFF0308	0x0000	R/W

T0CON is the configuration MMR described in Table 175.

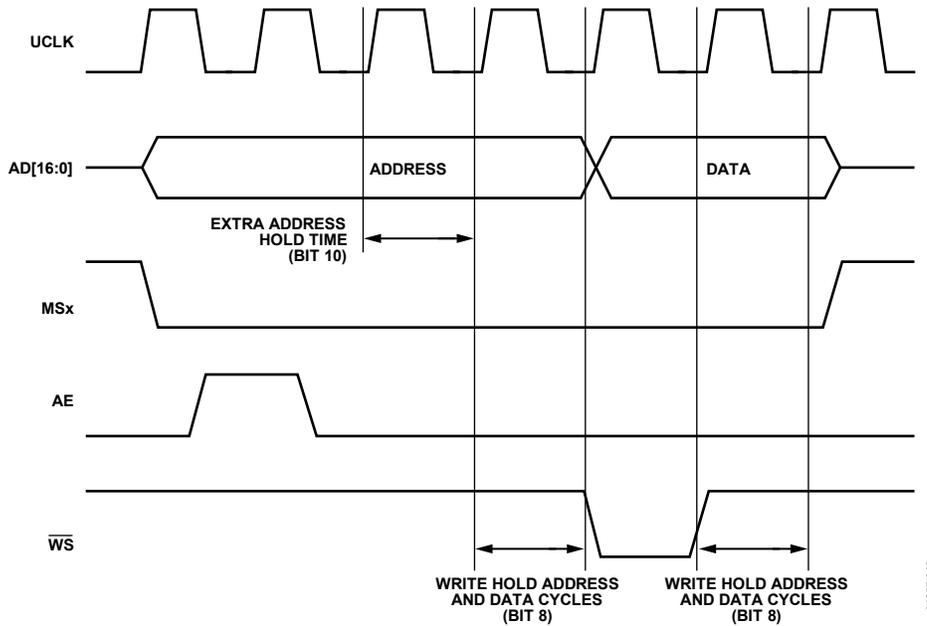
**Table 175. T0CON MMR Bit Descriptions**

Bit	Value	Description
15:8		Reserved.
7		Timer0 enable bit. Set by user to enable Timer0. Cleared by user to disable Timer0 by default.
6		Timer0 mode. Set by user to operate in periodic mode. Cleared by user to operate in free-running mode. Default mode.
5:4		Reserved.
3:2		Prescale.
	00	Core Clock/1. Default value.
	01	Core Clock/16.
	10	Core Clock/256.
	11	Undefined. Equivalent to 00.
1:0		Reserved.

**Table 176. T0CLRI Register**

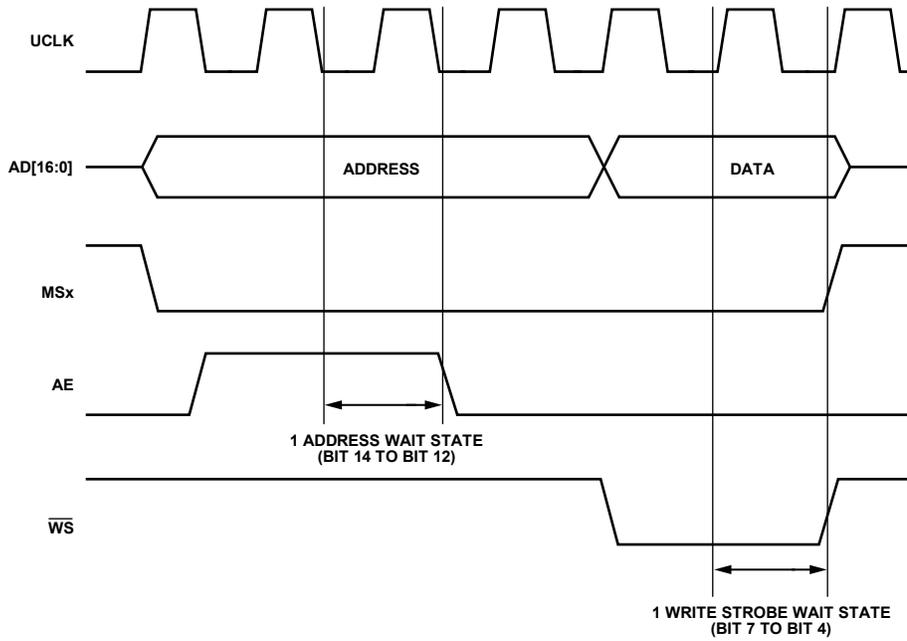
Name	Address	Default Value	Access
T0CLRI	0xFFFF030C	0xFF	W

T0CLRI is an 8-bit register. Writing any value to this register clears the interrupt.



04955-042

Figure 85. External Memory Write Cycle with Address and Write Hold Cycles



04955-043

Figure 86. External Memory Write Cycle with Wait States

**POWER-ON RESET OPERATION**

An internal power-on reset (POR) is implemented on the ADuC7019/20/21/22/24/25/26/27/28/29. For  $LV_{DD}$  below 2.35 V typical, the internal POR holds the part in reset. As  $LV_{DD}$  rises above 2.35 V, an internal timer times out for, typically, 128 ms before the part is released from reset. The user must ensure that the power supply  $IOV_{DD}$  reaches a stable 2.7 V minimum level by this time. Likewise, on power-down, the internal POR holds the part in reset until  $LV_{DD}$  drops below 2.35 V.

Figure 94 illustrates the operation of the internal POR in detail.

**TYPICAL SYSTEM CONFIGURATION**

A typical ADuC7020 configuration is shown in Figure 95. It summarizes some of the hardware considerations discussed in the previous sections. The bottom of the CSP package has an exposed pad that must be soldered to a metal plate on the board for mechanical reasons. The metal plate of the board can be connected to ground.

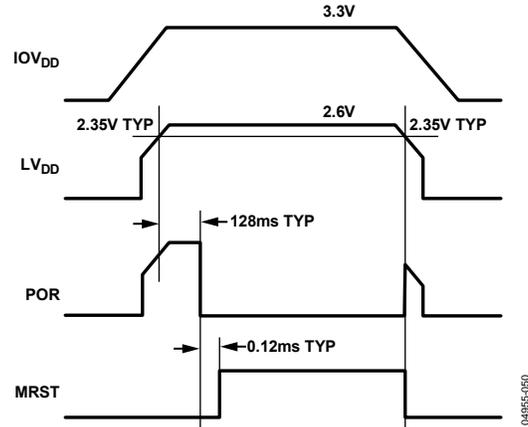


Figure 94. Internal Power-On Reset Operation

04955-050

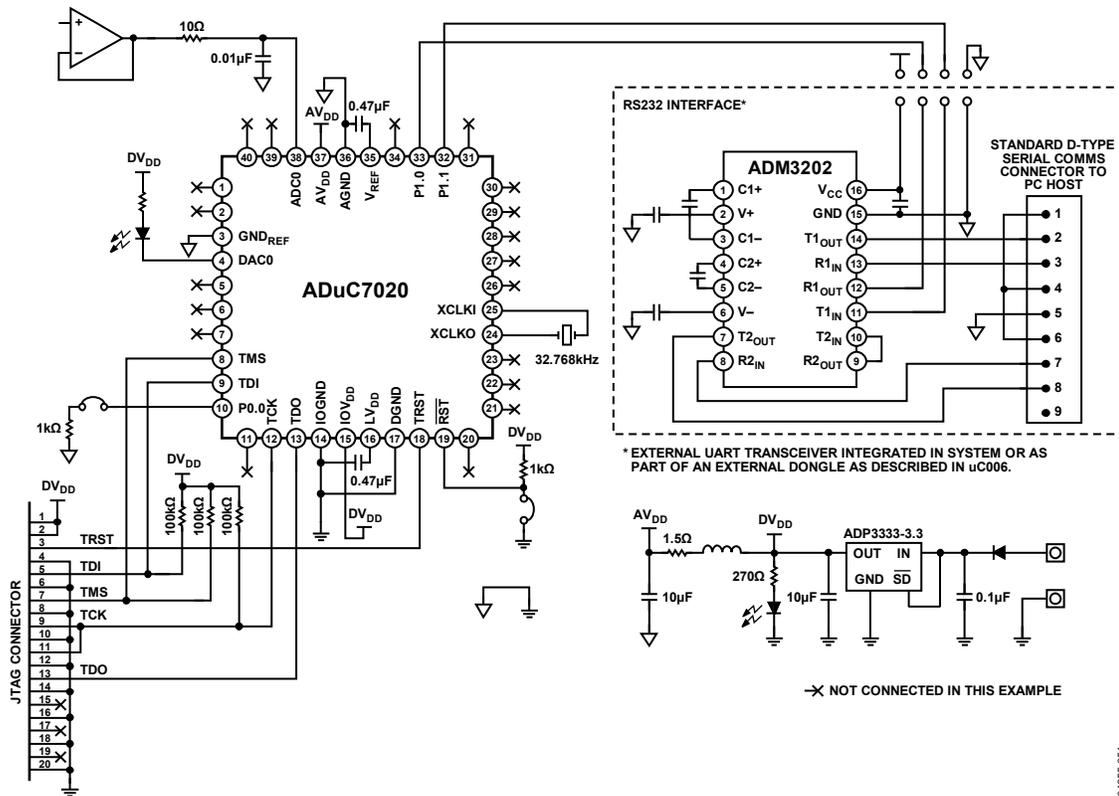


Figure 95. Typical System Configuration

04955-051

## ORDERING GUIDE

Model <sup>1,2</sup>	ADC Channels <sup>3</sup>	DAC Channels	FLASH/ RAM	GPIO	Down- loader	Temperature Range	Package Description	Package Option	Ordering Quantity
ADuC7019BCPZ62I	5	3	62 kB/8 kB	14	I <sup>2</sup> C	-40°C to +125°C	40-Lead LFCSP_WQ	CP-40-9	
ADuC7019BCPZ62I-RL	5	3	62 kB/8 kB	14	I <sup>2</sup> C	-40°C to +125°C	40-Lead LFCSP_WQ	CP-40-9	2,500
ADuC7019BCPZ62I-RL7	5	3	62 kB/8 kB	14	I <sup>2</sup> C	-40°C to +125°C	40-Lead LFCSP_WQ	CP-40-9	750
ADuC7020BCPZ62	5	4	62 kB/8 kB	14	UART	-40°C to +125°C	40-Lead LFCSP_WQ	CP-40-9	
ADuC7020BCPZ62-RL7	5	4	62 kB/8 kB	14	UART	-40°C to +125°C	40-Lead LFCSP_WQ	CP-40-9	750
ADuC7020BCPZ62I	5	4	62 kB/8 kB	14	I <sup>2</sup> C	-40°C to +125°C	40-Lead LFCSP_WQ	CP-40-9	
ADuC7020BCPZ62I-RL	5	4	62 kB/8 kB	14	I <sup>2</sup> C	-40°C to +125°C	40-Lead LFCSP_WQ	CP-40-9	2,500
ADuC7020BCPZ62I-RL7	5	4	62 kB/8 kB	14	I <sup>2</sup> C	-40°C to +125°C	40-Lead LFCSP_WQ	CP-40-9	750
ADuC7021BCPZ62	8	2	62 kB/8 kB	13	UART	-40°C to +125°C	40-Lead LFCSP_WQ	CP-40-9	
ADuC7021BCPZ62-RL	8	2	62 kB/8 kB	13	UART	-40°C to +125°C	40-Lead LFCSP_WQ	CP-40-9	2,500
ADuC7021BCPZ62-RL7	8	2	62 kB/8 kB	13	UART	-40°C to +125°C	40-Lead LFCSP_WQ	CP-40-9	750
ADuC7021BCPZ62I	8	2	62 kB/8 kB	13	I <sup>2</sup> C	-40°C to +125°C	40-Lead LFCSP_WQ	CP-40-9	
ADuC7021BCPZ62I-RL	8	2	62 kB/8 kB	13	I <sup>2</sup> C	-40°C to +125°C	40-Lead LFCSP_WQ	CP-40-9	2,500
ADuC7021BCPZ32	8	2	32 kB/4 kB	13	UART	-40°C to +125°C	40-Lead LFCSP_WQ	CP-40-9	
ADuC7021BCPZ32-RL7	8	2	32 kB/4 kB	13	UART	-40°C to +125°C	40-Lead LFCSP_WQ	CP-40-9	750
ADuC7022BCPZ62	10		62 kB/8 kB	13	UART	-40°C to +125°C	40-Lead LFCSP_WQ	CP-40-9	
ADuC7022BCPZ62-RL7	10		62 kB/8 kB	13	UART	-40°C to +125°C	40-Lead LFCSP_WQ	CP-40-9	750
ADuC7022BCPZ32	10		32 kB/4 kB	13	UART	-40°C to +125°C	40-Lead LFCSP_WQ	CP-40-9	
ADuC7022BCPZ32-RL	10		32 kB/4 kB	13	UART	-40°C to +125°C	40-Lead LFCSP_WQ	CP-40-9	2,500
ADuC7024BCPZ62	10	2	62 kB/8 kB	30	UART	-40°C to +125°C	64-Lead LFCSP_VQ	CP-64-1	
ADuC7024BCPZ62-RL7	10	2	62 kB/8 kB	30	UART	-40°C to +125°C	64-Lead LFCSP_VQ	CP-64-1	750
ADuC7024BCPZ62I	10	2	62 kB/8 kB	30	I <sup>2</sup> C	-40°C to +125°C	64-Lead LFCSP_VQ	CP-64-1	
ADuC7024BCPZ62I-RL	10	2	62 kB/8 kB	30	I <sup>2</sup> C	-40°C to +125°C	64-Lead LFCSP_VQ	CP-64-1	2,500
ADuC7024BSTZ62	10	2	62 kB/8 kB	30	UART	-40°C to +125°C	64-Lead LQFP	ST-64-2	
ADuC7024BSTZ62-RL	10	2	62 kB/8 kB	30	UART	-40°C to +125°C	64-Lead LQFP	ST-64-2	1,000
ADuC7025BCPZ62	12		62 kB/8 kB	30	UART	-40°C to +125°C	64-Lead LFCSP_VQ	CP-64-1	
ADuC7025BCPZ62-RL	12		62 kB/8 kB	30	UART	-40°C to +125°C	64-Lead LFCSP_VQ	CP-64-1	2,500
ADuC7025BCPZ32	12		32 kB/4 kB	30	UART	-40°C to +125°C	64-Lead LFCSP_VQ	CP-64-1	
ADuC7025BCPZ32-RL	12		32 kB/4 kB	30	UART	-40°C to +125°C	64-Lead LFCSP_VQ	CP-64-1	2,500
ADuC7025BSTZ62	12		62 kB/8 kB	30	UART	-40°C to +125°C	64-Lead LQFP	ST-64-2	
ADuC7025BSTZ62-RL	12		62 kB/8 kB	30	UART	-40°C to +125°C	64-Lead LQFP	ST-64-2	1,000
ADuC7026BSTZ62	12	4	62 kB/8 kB	40	UART	-40°C to +125°C	80-Lead LQFP	ST-80-1	
ADuC7026BSTZ62-RL	12	4	62 kB/8 kB	40	UART	-40°C to +125°C	80-Lead LQFP	ST-80-1	1,000
ADuC7026BSTZ62I	12	4	62 kB/8 kB	40	I <sup>2</sup> C	-40°C to +125°C	80-Lead LQFP	ST-80-1	
ADuC7026BSTZ62I-RL	12	4	62 kB/8 kB	40	I <sup>2</sup> C	-40°C to +125°C	80-Lead LQFP	ST-80-1	1,000
ADuC7027BSTZ62	16		62 kB/8 kB	40	UART	-40°C to +125°C	80-Lead LQFP	ST-80-1	
ADuC7027BSTZ62-RL	16		62 kB/8 kB	40	UART	-40°C to +125°C	80-Lead LQFP	ST-80-1	1,000
ADuC7027BSTZ62I	16		62 kB/8 kB	40	I <sup>2</sup> C	-40°C to +125°C	80-Lead LQFP	ST-80-1	
ADuC7027BSTZ62I-RL	16		62 kB/8 kB	40	I <sup>2</sup> C	-40°C to +125°C	80-Lead LQFP	ST-80-1	1,000
ADuC7028BBCZ62	8	4	62 kB/8 kB	30	UART	-40°C to +125°C	64-Ball CSP_BGA	BC-64-4	
ADuC7028BBCZ62-RL	8	4	62 kB/8 kB	30	UART	-40°C to +125°C	64-Ball CSP_BGA	BC-64-4	2,500
ADuC7029BBCZ62	7	4	62 kB/8 kB	22	UART	-40°C to +125°C	49-Ball CSP_BGA	BC-49-1	
ADuC7029BBCZ62-RL	7	4	62 kB/8 kB	22	UART	-40°C to +125°C	49-Ball CSP_BGA	BC-49-1	4,000
ADuC7029BBCZ62I	7	4	62 kB/8 kB	22	I <sup>2</sup> C	-40°C to +125°C	49-Ball CSP_BGA	BC-49-1	
ADuC7029BBCZ62I-RL	7	4	62 kB/8 kB	22	I <sup>2</sup> C	-40°C to +125°C	49-Ball CSP_BGA	BC-49-1	4,000