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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

E·XF

| Product Status | Active |
|----------------------------|---|
| Core Processor | ARM7® |
| Core Size | 16/32-Bit |
| Speed | 44MHz |
| Connectivity | EBI/EMI, I ² C, SPI, UART/USART |
| Peripherals | PLA, PWM, PSM, Temp Sensor, WDT |
| Number of I/O | 30 |
| Program Memory Size | 62KB (31K x16) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 2K x 32 |
| Voltage - Supply (Vcc/Vdd) | 2.7V ~ 3.6V |
| Data Converters | A/D 12x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-VFQFN Exposed Pad, CSP |
| Supplier Device Package | 64-LFCSP-VQ (9x9) |
| Purchase URL | https://www.e-xfl.com/product-detail/analog-devices/aduc7025bcpz62-rl |

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REVISION HISTORY

| 12/15—Rev. F to Rev. G | |
|--|-------|
| Changed CP-40-1 to CP-40-9 Univer- | ersal |
| Updated Outline Dimensions | 97 |
| Deleted Figure 96 (CP-40-1); Renumbered Sequentially | 97 |
| Changes to Ordering Guide | .101 |

5/13-Rev. E to Rev. F

| Changes to Figure 1 | 1 |
|---|-----|
| Added Figure 2 to Figure 10; Renumbered Sequentially | 4 |
| Changes to Figure 19; Added Figure 20 | 21 |
| Changes to EPAD Note in Figure 21 and Figure 22 | 22 |
| Changes to EPAD Note in Table 11 | 23 |
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| Changes to Table 82 | 68 |
| Added Table 83, Figure 73, Figure 74, Following Text, and | |
| Table 84; Renumbered Sequentially | 69 |
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| Changes to Table 101 | 72 |
| Changes to Timer2 (Wake-Up Timer) Section | 87 |
| Changes to Figure 94 | 95 |
| Updated Outline Dimensions | 97 |
| Changes to Ordering Guide | 101 |

7/12-Rev. D to Rev. E

| Changed SCLOCK to SCLK When Refering to SPI Clock, |
|---|
| SPIMISO to MISO when Refering to SPI MISO, SPIMOSI to |
| MOSI when Refering to SPI MOSI, and SPICSL to $\overline{\text{CS}}$ when |
| Refering to SPI Chip Select Universal |
| Changes to Table 4, Table 5, and Figure 511 |
| Changes to Endnote 1 in Table 6 and Figure 612 |
| Changes to Table 7 and Figure 713 |
| Changes to Table 8 and Figure 814 |
| Changes to Table 9 and Figure 915 |
| Changed EPAD Note in Figure 12 and Table 1118 |
| Changed EPAD Note in Figure 13 and Table 1221 |
| Changes to Bit 6 in Table 1843 |
| Changes to Example Source Code (External Crystal Selection) |
| Section and Example Source Code (External Clock Selection) |
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| 5/11—Rev. C to Rev. D |

Changes to Table 411

| Changes to Table 105 | 67 |
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| Updated Outline Dimensions | |
| Changes to Ordering Guide | 94 |
| 12/09—Rev. B to Rev. C | |

-Rev. B to Rev. C

| Added ADuC7029 Part | Universal |
|--|-----------|
| Added Table Numbers and Renumbered Tables | Universal |
| Changes to Figure Numbers | Universal |
| Changes to Table 1 | 6 |
| Changes to Figure 3 | 9 |
| Changes to Table 3 and Figure 4 | 10 |
| Changes to Table 10 | 16 |
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| Updated Outline Dimensions | 91 |
| Changes to Ordering Guide | 94 |
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3/07—Rev. A to Rev. B

| Added ADuC7028 Part | . Universal |
|---|-------------|
| Updated Format | . Universal |
| Changes to Figure 2 | 5 |
| Changes to Table 1 | 6 |
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| Changes to External Memory Interfacing Section | 80 |
| Added IOV _{DD} Supply Sensitivity Section | |
| Changes to Ordering Guide | 90 |

1/06—Rev. 0 to Rev. A

| Changes to Table 1 | 6 |
|---|----|
| Added the Flash/EE Memory Reliability Section | 43 |
| Changes to Table 30 | 52 |
| Changes to Serial Peripheral Interface | 66 |
| Changes to Ordering Guide | 90 |
| | |

10/05—Revision 0: Initial Version



SPECIFICATIONS

 $AV_{DD} = IOV_{DD} = 2.7 V$ to 3.6 V, $V_{REF} = 2.5 V$ internal reference, $f_{CORE} = 41.78 MHz$, $T_A = -40^{\circ}C$ to $+125^{\circ}C$, unless otherwise noted.

| ParameterMinTypMaxUnitTest Conditions/CommentsADC CHANNEL SPECIFICATIONS5 μ sFight acquisition clocks and fADC/2ADC Power-Up Time5 μ sFight acquisition clocks and fADC/2DC Accuracy'*12Bits1.0Resolution11 10 SDifferential Nonlinearity** 20.6 ± 1.5 LSB2.5 V internal referenceDifferential Nonlinearity** ± 0.6 ± 1.5 LSB1.0 V external referenceDC Code Distribution1 ± 2.5 LSB1.0 V external referenceDC Code Distribution ± 1 ± 2.5 LSB1.0 V external referenceD'ffset Eror ± 1 ± 2.5 LSB1.0 V external referenceOffset Eror Match ± 1 ± 2.5 LSBIncludes distortion and noise componentsOffset Eror Match ± 1 LSBfn = 10 MHz sine wave, funnt = 1 MSPSNUMMIC PERPRIMACE -75 dBfn = 10 MHz sine wave, funnt = 1 MSPSOrdan Lokise Ratio (SNR) -75 dBfn = 10 MHz sine wave, funnt = 1 MSPSInput Voltage Ranges -75 dBfpInput Voltage Ranges -75 $4B$ Measured on adjacent channelsOutry Utylege Ranges -75 $4B$ fpInput Voltage Ranges -75 $4B$ 47 MF from V_{RP} to AGNDOutry Utylege Ranges -75 $4B$ 47 MF from V_{RP} to AGNDOutry Utylege Ranges -75 -5 70 Input Voltage Range | Table 1. | | | | - | |
|---|---|-------|-------------------------|--------------------------------|--------|---|
| ADC Characy 1° Eight acquisition clocks and IADC/2 DC Accuracy' ² Bits Resolution 12 Bits Integral Nonlinearity ±0.6 ±1.5 LS8 2.5 Vinternal reference Differential Nonlinearity ±0.5 ±1.4 LS8 2.5 Vinternal reference Differential Nonlinearity ±0.5 ±1.4 LS8 2.5 Vinternal reference DC Code Distribution 1 LS8 2.5 Vinternal reference Offset Error Match ±1 LS8 ADC input is a dc voltage Gain Error Match ±1 LS8 Internal reference Gain Error Match ±1 LS8 Internal reference Signal-to-Noise Ratio (SNR) 69 LS8 Internal reference Signal-to-Noise Ratio (SNR) 69 LS8 Internal reference Total Harmonic Distorion (TND) -78 KB Internal reference Single-to-Match -11 ±6 MA Internal reference Differential Node -75 KB Intududes distortion and noise components | Parameter | Min | Тур | Max | Unit | Test Conditions/Comments |
| ADC Power-Up Time5 μs Besolution12BitsResolution12BitsIntegral Nonlinearity ± 0.6 ± 1.5 LSB2.5 V internal referenceDifferential Nonlinearity ^{1,4} ± 0.5 ± 19 LSB1.0 V external referenceDC Code Distribution1LSB1.0 V external referenceDC Code Distribution1LSBADC input is a dc voltageENDPONT ERRORS ¹ LLSBADC input is a dc voltageCode Distribution ± 1 ± 2 LSBCode Distribution ± 1 ± 2 LSBOffset Error Match ± 1 ± 2 LSBGain Error Match ± 1 LSBIncludes distortion and noise componentsONAMIC ERRORMANCE -75 dBSignal-to-Noise Ratio (SNR)69dBPeak Hamonic Distortion (THD) -78 dBPeak Hamonic Costalk -80 dBMANLOG INPUT -75 dBInput Voltage Ranges $prprDifferential Mode\sqrt{\alpha_1^2} \pm w_2^2VSingle-Ended Mode0 to V_{tar}prOutryut Voltage Ranges2.5NVNC-HIP VOLTAGE REFERENCE2.5NVOutryut Voltage Ranges0.625Nv_{exo}DIFferencial Nonlinearity\pm 1x_3Differencial Nonlinearity\pm 1x_5During ADC Accuracy2.2x_5Reference Seriet Reference2.5NV_{exo}$ | ADC CHANNEL SPECIFICATIONS | | | | | Eight acquisition clocks and fADC/2 |
| DC Accuracy' ^{1,2} Resolution12IIResolution ± 0.6 ± 1.5 LSB2.5 V internal referenceDifferential Nonlinearity ^{1,4} ± 0.5 ± 1.7 LSB1.0 V external referenceDC Code Distribution ± 0.7 LSB1.0 V external referenceDC Code Distribution ± 1.1 ± 2.5 LSBNOC input is a d voltageENDPOINT ERRORS'ILSBNOC input is a d voltageCoffset Error ± 1.1 ± 2.5 LSBOffset Error Match ± 1.1 LSBGain Error Match ± 1.1 LSBDYNAMIC PERFORMANCE ± 1.1 LSBSignal-to-Nose Ratio (SNR)6.9HBTotal Harmonic Distortion (HD) -78 HBPeak Harmonic of Syntous Noise (PHSN) -75 HBMALOG INPUTInput Voltage RangesInput Varge 2.2VDifferential Mode $V_{CR}^2 \pm V_{BR/2}$ VDifferential Mode $0 to V_{ac}$ VLakage Current ± 1.1 ± 6 PFDuring ADC acquisitionInternal Perference $0 to V_{ac}$ ON-CHIP VOUTAGE REFERENCE 2.5 Nu $T_A = 25^{\circ}C$ National Mode 75 40 $12 = 25^{\circ}C$ Output Inpedance 0.625 N_{U0} V_{U1} Power Supple Report Reference 2.0 P_{U1} Differential Nonlinearity ± 1.1 45 Difference Inperature Coefficient 90 N_{U0} Output Inpedance 0.625 | ADC Power-Up Time | | 5 | | μs | |
| Resolution12Bits ± 0.6 ± 1.5 LSB LSB2.5 V internal referenceIntegral Nonlinearity ^{1,4} ± 0.6 ± 1.0 LSB1.0 V external referenceDIfferential Nonlinearity ^{1,4} $\pm 0.7 - 0.5$ LSB2.5 V internal referenceDC Code Distribution1LSB2.5 V internal referenceDC Code Distribution1 ± 2.7 LSBENDPOINT ERRORS'-LSBADC input is a dc voltageCriste Error Match ± 1 ± 2.2 LSBGain Error Match ± 1 LSBfm = 10 kHz sine wave, fsumt = 1 MSPSSignal-to-Noise Ratio (SNR)69KBfm = 10 kHz sine wave, fsumt = 1 MSPSTotal Harmonic Distortion (THD) -75 KBMeasured on adjacent channelsPack Harmonic Cristralik -80 KBMeasured on adjacent channelsANALOG INPUT-75KBKBLincludes distortion and noise componentsInput Voltage Ranges -75 KBVDifferential Mode -75 KBVSingle-Ended Mode 2.5 VVLeakage Current ± 1 ± 6 μA Input Capacitance 2.5 V $7 \pm 25^{\circ}C$ Reference Temperature Coefficient ± 40 $\gamma = 5$ Outy Utolage 2.5 AV_{00} VNutrent Pedence 70 $T \pm 25^{\circ}C$ Internal Valge Range 0.625 AV_{00} VDCACHANKEL SPECIFICATIONS 58 Guaranteed monotonicDifferential Non | DC Accuracy ^{1, 2} | | | | | |
| $ \begin{array}{ c c c c } \mbox{Internal reference} & \pm 1.0 & \pm 1.5 & \pm 1.5 & \pm 2.5 V internal reference \\ \pm 1.0 & \pm 1.0 & \pm 5 & \pm 1.0 & \pm 5 &$ | Resolution | 12 | | | Bits | |
| Life ential Nonlinearity $^{1.4}$ ± 1.0 ± 0.5 LS8 $\pm 1.7 - 0.9$ LS8 LS9 L | Integral Nonlinearity | | ±0.6 | ±1.5 | LSB | 2.5 V internal reference |
| Differential Nonlinearity3-4 ± 0.5 $\pm 1/-0.9$ LSB2.5 V internal reference 1.0 V external reference 1.0 V external reference 1.0 V external referenceDC Code Distribution1LSBADC input is a dx voltageENDPOINT ERNOR5'Offset Error Gain Error ± 1 ± 2 LSBDYNAMIC PERFORMANCE ± 1 LSB-Signal-to-Noise Ratio (SNR)69-dBTotal Harmonic Distortion (THD)-78dBPeak Harmonic or Spurious Noise (PHSN)-75dBMALOG INPUT Input Voltage RangesDifferential Mode $V_{Cin}^4 \pm V_{Kir/2}$ VSingle-Ended Mode0 to V_{inr} VOutput Voltage Reference Ermerature Coefficient ± 40 ppm/*COutput Voltage Ranges2.5VT_a = 25°COutput Voltage Ranges $T_a = 25°C$ Output Voltage Ranges0.625AV _{con} VDAC CHANNEL SPECIFICATIONS $T_a = 25°C$ Output Ingelarea0.625AV _{con} VDAC CHANNEL SPECIFICATIONSR_a = 5 kΩ, CL = 100 pFDAC CHANNEL SPECIFICATIONSDAC CHANNEL SPECIFICATIONSDAC CHANNEL SPECIFICATIONSDAC CHANNEL SPECIFICATIONSDAC CHANNEL SPECIFICATIONSDAC CHANNEL SPECIFICATIONSDIfferential | | | ±1.0 | | LSB | 1.0 V external reference |
| DC Code Distribution $+0.7/-0.6$ LSB1.0 V external reference ADC input is a dc voltageENDPOINT LERRORS'LSBADC input is a dc voltageOffset Error Match ± 1 ± 2 LSBGain Error ± 1 ± 2 ± 5 LSBGain Error Match ± 1 LSB $f_N = 10 \text{ kHz sine wave, fourner = 1 MSPSDYNAMIC PERFORMANCEf_N = 10 \text{ kHz sine wave, fourner = 1 MSPSDYNAMIC PERFORMANCEf_N = 10 \text{ kHz sine wave, fourner = 1 MSPSDYNAMIC PERFORMANCE-75dBPeak Harmonic Distortion (THD)-78dBPeak Harmonic or Spurious Noise(PHSN)-75dBChannel to Channel Crosstalk-80dBMALOG INPUT\mu\muInput Voltage RangesV_{Cx}^{A} \pm V_{W7}/2VDifferential Mode0 \text{ to Verrer}VON-CHIP VOLTAGE REFERENCEV_{Ta} = 25^{\circ}COutput Voltage2.5V_{Ta} = 25^{\circ}CReference Temperature Coefficient\pm 40ppm/^{\circ}CPower Supply Rejection Ratio75dBDTA CHANNEL SPECIFICATIONSTa = 25^{\circ}CDC Accuracy'\pm 1LSBResolution12BitsResolution12SitsResolution12SitsDifferential Nonlinearity\pm 1SitsDAC CHANNEL SPECIFICATIONSF_{T}SitsDC Accuracy'\pm 1SitsResolution12Sits$ | Differential Nonlinearity ^{3, 4} | | ±0.5 | +1/-0.9 | LSB | 2.5 V internal reference |
| DC Code Distribution1LSBADC input is a dc voltageENDPOINT ERRORS'Offset Error Match ± 1 -LSBGain Error Match ± 1 -LSBGain Error Match ± 1 -LSBDYNAMIC PERFORMANCEfn = 10 kHz sine wave, fswerd = 1 MSPSSignal-to-Noise Ratio (SNR)69-dBTotal Harmonic Distortion (THD)-78dB-Peak Harmonic Or Spurious Noise-77dBMeasured on adjacent channelsANALOG INPUTdBMeasured on adjacent channelsInput Voltage Ranges-VV-Differential ModeVoit* ± Ver/2VVLeakage Current ± 1 ± 6 V/4Input Voltage Ranges0.47 µE from Vare to AGNDOntCHIP VOLTAGE REFERENCE-0.47 µE from Vare to AGNDOutput Voltage2.5rVTa = 25°CReference Temperature Coefficient ± 40 Power Supply Rejection Ratio75-MBDIC Accuracy'Differential NonlinearityInternal Vere Power On Time1-ms-DIC Accuracy'Differential NonlinearityDifferential NonlinearityDifferential Nonlinearity-< | | | +0.7/-0.6 | | LSB | 1.0 V external reference |
| ENDPOINT ERRORS* ± 1 ± 2 ± 3 ± 3 ± 2 ± 3 ± 3 Offset Error Match ± 1 ± 2 ± 5 ± 5 ± 5 ± 5 ± 5 Gain Error Match ± 1 ± 2 ± 5 ± 5 ± 5 ± 5 ± 1 ± 5 ± 5 ± 1 ± 6 ± 6 ± 1 ± 1 ± 6 ± 1 ± 6 ± 1 ± 6 ± 1 <td>DC Code Distribution</td> <td></td> <td>1</td> <td></td> <td>LSB</td> <td>ADC input is a dc voltage</td> | DC Code Distribution | | 1 | | LSB | ADC input is a dc voltage |
| Offset Error ± 1 ± 2 LSBOffset Error Match ± 1 LSBGain Error ± 2 ± 5 Gain Error Match ± 1 LSBDTMAMIC PERFORMANCE ± 1 LSBSignal-to-Noise Ratio (SNR)69dBTotal Harmonic Distortion (THD) -78 dBPeak Harmonic or Spurious Noise -75 dB(PHSN) -78 dBChannel-to-Channel Crosstalk -80 dBANALOG INPUT -78 dB Input Voltage Ranges 0 to $V_{ex}^{0} \pm V_{exr/2}$ VSingle-Ended Mode $V_{ex}^{0} \pm V_{exr/2}$ VLeakage Current ± 1 0 to V_{trer} μA Input Voltage Ranges 0 to V_{trer} μA Input Voltage Ranges 0 to V_{trer} μA Input Voltage Ranges 0 to V_{trer} μA Input Capacitance 20 pF During ADC acquisitionON-CHIP VOLTAGE REFERENCE V $T_x = 25^{\circ}C$ Reference Temperature Coefficient ± 40 pg Power Supply Rejection Ratio 75 dB Output Voltage Range 0.625 AV_{co} DAC CHANNEL SPECIFICATIONS $T_x = 15$ DC Acturacy' $E1$ $E3$ Relative Accuracy ± 1 $E3$ Relative Accuracy ± 1 $S6$ Gain Error Mismatch 0.1 $\%$ Michage Range_0 0 to DAC_{axi} V Output Voltage Range_1 0 to DAC_{xir} V | ENDPOINT ERRORS ⁵ | | | | | |
| Offset Error Match ± 1 LLSBGain Error Match ± 2 ± 5 LSBDYNAMIC PERFORMANCE ± 2 ± 5 LSBSignal-to-Noise Ratio (SNR)69dBIncludes distortion and noise componentsTotal Harmonic Distortion (THD) -78 dBPeak Harmonic or Spurious Noise -75 dB(PHSN)Channel-to-Channel Crosstalk -80 dBChannel-to-Channel Crosstalk -80 dBANALOG INPUT -75 dBInput Voltage Ranges $V_{CR}^0 \pm V_{KR}^0 \pm V_{KR}^0/2$ VLeakage Current ± 1 ± 6 Input Capacitance 20 pF Output Voltage 2.5 NV Accuracy ± 5 mV Reference Temperature Coefficient ± 40 ppr/C Power Supply Rejection REFERENCE NV_{CR} NV_{CR} Output Voltage Range 0.625 AV_{DD} V Input Voltage Range 0.625 AV_{DD} V Difference Temperature Coefficient ± 40 ppr/C Reference Temperature Coefficient ± 40 ppr/C Reference Temperature Coefficient ± 2 K_{DD} DAC CHANNEL SPECIPICATIONS K_{DD} K_{DD} DC Accuracy' E K_{DD} Relative Accuracy ± 1 K_{B} Gain Error Mismatch 0.1 $\%$ Michae Andreage 0 0 DAC CHANNEL SPECIPICATIONS K_{DD} DC Accuracy' K_{D} <t< td=""><td>Offset Error</td><td></td><td>±1</td><td>±2</td><td>LSB</td><td></td></t<> | Offset Error | | ±1 | ±2 | LSB | |
| Gain Error 1.2 1.5 LSBGain Error Match ± 1 LSBDYNAMIC PERFORMANCE f_{11} LSBSignal-to-Noise Ratio (SNR) 69 dBPeak Harmonic Of Spurious Noise (PHSN) -75 dBReak Harmonic Of Spurious Noise (PHSN) -75 dBChannel-to-Channel Crosstalk -80 dBMANLOG INPUTInput Voltage Ranges $V_{CN}^6 \pm V_{Rer/Z}$ V Input Voltage Ranges $V_{CN}^6 \pm V_{Rer/Z}$ V Differential Mode $V_{CN}^6 \pm V_{Rer/Z}$ V Leakage Current ± 1 ± 6 μA Input Capacitance 20 pF During ADC acquisitionON-CHIP VOLTAGE REFRENCE $0.47 \mu F$ from Veer to AGND $0.47 \mu F$ from Veer to AGNDOutput Voltage 2.5 V $T_a = 25^{\circ}C$ Output Voltage 2.5 V_{V} $T_a = 25^{\circ}C$ Output Voltage Range 0.625 AV_{oo} V Power Supply Rejection Ratio 75 dB $T_a = 25^{\circ}C$ Output Voltage Range 0.625 AV_{oo} V DAC CHANNEL SPECIFICATIONS DC C_{A} $R_L = 5 k\Omega, C_L = 100 pF$ DC Accuracy' ± 1 LSBGuaranteed monotonicRelative Accuracy ± 1 LSB Guaranteed monotonicDIfferential Nonlinearity ± 1 LSBGuaranteed monotonicDC Accuracy' R_{e} h_{e} h_{e} Resolution 12 ESB $Guaranteed monotonicDI $ | Offset Error Match | | ±1 | | LSB | |
| Call Error Match1LLSBDYNAMIC PERFORMANCE1LSBSignal-to-Noise Ratio (SNR)69dBTotal Harmonic Obstortion (THD)-78dBPeak Harmonic of Spurious Noise (PHSN)-75dBChannel-to-Channel Crosstalk-80dBMALCG INPUT-78dBInput Voltage Ranges $V_{Ce}^{6} \pm V_{Ee/Z}$ VDifferential Mode $V_{Ce}^{6} \pm V_{Ee/Z}$ VSingle-Ended Mode0 to V_{arr} VLeakage Current ± 1 ± 6 μA Input Voltage REFERENCE $V_{Ce}^{6} \pm V_{Ee/Z}$ V_{A} Output Voltage REFERENCE $V_{Ce}^{6} \pm V_{Ee/Z}$ V_{A} Output Voltage2.5 V_{A} V_{A} Reference Temperature Coefficient ± 40 $ppm^{n}CC$ $T_{A} = 25^{\circ}C$ Internal Viez Power-On Time1ms $T_{A} = 5^{\circ}C$ Internal Viez Power-On Time12Bits $R_{a} = 5 kQ, C_{a} = 100 pF$ DCAccuracy' ± 1 LSBGuaranteed monotonicDifferential Nonlinearity ± 1 LSBGuaranteed monotonicDifferential Nonlinearity ± 1 LSBGuaranteed monotonicOutput Hodage Range_00.625 AV_{DO} V DAC CHANNEL SPECIFICATIONS E_{A} E_{A} E_{A} Differential Nonlinearity ± 1 LSBGuaranteed monotonicOffset Error ± 1 E_{A} $2.5 V$ internal referenceGain Error A E_{A} E_{A} <td>Gain Error</td> <td></td> <td>+2</td> <td>+5</td> <td>LSB</td> <td></td> | Gain Error | | +2 | +5 | LSB | |
| DYNAMIC PERFORMANCE $=1$ <th< td=""><td>Gain Error Match</td><td></td><td>+1</td><td></td><td>I SB</td><td></td></th<> | Gain Error Match | | +1 | | I SB | |
| Signal-to-Noise Ratio (SNR)69dBIncludes distortion and noise componentsSignal-to-Noise Ratio (SNR)-78dBPeak Harmonic Distortion (THD)-78dBPeak Harmonic Distortion (THD)-78dBPeak Harmonic Or Spurious Noise (PHSN)-75dBMalboard-75dBANALOG INPUT Input Voltage Ranges-80dBMeasured on adjacent channels-80dBANALOG INPUT Input Voltage Ranges±1±6Differential Mode0 to V _{REF} VLeakage Current±1±6Leakage Current±1±6Accuracy±5WOutput Voltage2.5VAccuracy±40ppm/°CAccuracy±440ppm/°CPower Supply Rejection Ratio750Output Impedance70 Ω Input Voltage Range0.625AV ₀₀ DAC CHANNEL SPECIFICATIONS | | | | | 250 | $f_{\rm IN} = 10 \rm kHz$ sine wave $f_{\rm CAMPLE} = 1 \rm MSPS$ |
| DigrationDigramDigramDigramDigramDigramTotal Harmonic Distortion (THD) -73 dBPeak Harmonic Or Spurious Noise (PHSN) -75 dBChannel-to-Channel Crosstalk -80 dBANLOG INPUT Input Voltage RangesdBDifferential Mode $V_{Cu}^4 \pm V_{igs}/2$ VSingle-Ended Mode 0 to V_{ker} VLeakage Current ± 1 ± 6 μA Input Capacitance20 pF During ADC acquisitionOutput Voltage2.5 V $Accuracy$ Reference Temperature Coefficient ± 40 $pm/°C$ Power Supply Rejection Ratio75dBOutput Voltage Range0.625 AV_{00} Internal Varge Power-On Time1msInput Voltage Range0.625 AV_{00} DC Accuracy' ± 1 ± 1 Relative Accuracy ± 2 LSBDifferential Monlinearity ± 1 $Bits$ Relative Accuracy ± 1 $\%$ Gain Error ⁴ 0.1 $\%$ Matter Accuracy ± 1 $\%$ Gain Error ⁴ 0.1 $\%$ MALOG CUTPUTS V Output Voltage Range_00 to DACserOutput Voltage Range_10 to 2.5VOutput Voltage Range_20 to DACserVOutput Voltage Range_10 to 2.5VOutput Voltage Range_20 to DACserVOutput Voltage Range_10 to 2.5VOutput Voltage Range_2 </td <td>Signal-to-Noise Batio (SNB)</td> <td></td> <td>69</td> <td></td> <td>dB</td> <td>Includes distortion and noise components</td> | Signal-to-Noise Batio (SNB) | | 69 | | dB | Includes distortion and noise components |
| Numeric of Spurious Noise (PHSN)-75dbPeak Harmonic of Spurious Noise (PHSN)-75dBChannel-to-Channel Crosstalk-80dBANLOG INPUT Input Voltage Ranges-80dBDifferential Mode $Vcx^6 \pm Vart/2$ Single-Ended ModeVSingle-Ended Mode0 to V_{RF} VLeakage Current ± 11 ± 6 Input Capacitance20pFDuring ADC acquisitionON-CHIP VOLTAGE REFERENCE0.47 µF from V_{RF} to AGND0.47 µF from V_{RF} to AGNDOutput Voltage2.5w $X_a = 25^\circ C$ Accuracy ± 5 mV $T_a = 25^\circ C$ Reference Temperature Coefficient ± 40 ppm/°CPower Supply Rejection Ratio75GOutput Voltage Range0.625 AV_{00} DAC CHANNEL SPECIFICATIONS $C_{accuracy^7}$ $R_L = 5 k\Omega, C_L = 100 pF$ DAC CHANNEL SPECIFICATIONS L SBDAC CHANNEL SPECIFICATIONS L SBDifferential Nonlinearity ± 11 SB Offset Error ± 15 mVGain Error ⁸ 11 $\%$ Output Voltage Range_00 to DACkerVOutput Voltage Range_00 to DACkerVOutput Voltage Range_00 to DACkerVOutput Voltage Range_10 to 2.5VOutput Voltage Range_20 to DACkerVOutput Voltage Range_20 to DACkerVOutput Voltage Range_20 to DACkerVOutput Voltage Ra | Total Harmonic Distortion (THD) | | -78 | | dB | includes distortion and holse components |
| PreservationChannel-to-Channel Crosstalk-R0dBMeasured on adjacent channelsANALOG INPUTImput Voltage Ranges $V_{CA}^6 \pm V_{RF/2}$ VInput Voltage Ranges $0 \text{ to } V_{ter}$ VLeakage Current ± 1 ± 6 μA Input Voltage Ranges $0 \text{ to } V_{ter}$ VLeakage Current ± 1 ± 6 μA Input Voltage Range 2.5 V $0.47 \ \mu F \text{ from } V_{ser}$ to AGNDON-CHIP VOLTAGE REFERENCE V $1 \times 25^{\circ}\text{C}$ Output Voltage 2.5 V $T_{A} = 25^{\circ}\text{C}$ Reference Temperature Coefficient ± 40 ppm/°CPower Supply Rejection Ratio 75 dB Output Voltage Range 0.625 AV_{00} VTa = 25°CTa = 25°CInternal Varge Power-On TimemsEXTERNAL REFERENCE INPUTmsInput Voltage Range 0.625 DC Accuracy ⁷ ExternalResolution12Relative Accuracy ± 1 Relative Accuracy ± 1 Relative Accuracy ± 1 Gain Error ⁸ 0.1 Gain Error Mismatch 0.1 Output Voltage Range_0 $0 \text{ to } DAC_{SEF}$ Output Voltage Range_1 $0 \text{ to } DAC_{SEF}$ Output Voltage Range_2 $0 \text{ to } DAC_{V_{00}$ Output Voltage Range_2 $0 \text{ to } DAC_{V_{00}$ Output Voltage Range_2 $0 \text{ to } DAC_{V_{00}$ Output Voltage Range_2 $0 \text{ to } DAC_{SEF}$ Output Voltage Range_2 <td>Poak Harmonic or Spurious Noiso</td> <td></td> <td>_76 _75</td> <td></td> <td>dB</td> <td></td> | Poak Harmonic or Spurious Noiso | | _76 _75 | | dB | |
| $\begin{array}{c c c c } Channel-to-Channel Crosstalk & -80 & dB & Measured on adjacent channels \\ \hline ANALOG INPUT & & & & & & & & & & & & & & & & & & &$ | (PHSN) | | -75 | | uв | |
| ANALOG INPUT Input Voltage Ranges Input Voltage Ranges Vcm 4 Vser/2 V Differential Mode $Vcm^4 \pm Vser/2$ V Single-Ended Mode 0 to $Vser/2$ V Leakage Current ± 1 ± 6 μA Input Capacitance 20 pF During ADC acquisition ON-CHIP VOLTAGE REFERENCE V $A^2 \mu F$ from V_{BEF} to AGND Output Voltage 2.5 V $T_a = 25^\circ$ C Accuracy ± 40 pgm/C $T_a = 25^\circ$ C Reference Temperature Coefficient ± 40 pgm/C $T_a = 25^\circ$ C Output Impedance 70 G $T_a = 25^\circ$ C Internal V_{BEF} Power-On Time 1 ms $T_a = 25^\circ$ C Input Voltage Range 0.625 AV_{DD} V $T_a = 25^\circ$ C Input Voltage Range 0.625 AV_{DD} V $T_a = 25^\circ$ C Input Voltage Range 0.625 AV_{DD} V $T_a = 25^\circ$ C Input Voltage Range 0.625 AV_{DD} V $T_a = 25^\circ$ C DAC CHANNEL SPECIFICATIONS $T_a = 16^\circ$ < | Channel-to-Channel Crosstalk | | -80 | | dB | Measured on adjacent channels |
| $\begin{array}{ c c c } \mbox{Input Voltage Ranges} & V_{Cvh}^{6} \pm V_{Cvh}^{6} \pm V_{Err}/2 & V_{Cvh}^{6} \pm V$ | ANALOG INPUT | | | | | |
| Differential Mode $V_{CM}^{4} \pm V_{REF}/2$ VSingle-Ended Mode0 to V_{REF} VLeakage Current ± 1 ± 6 μA Input Capacitance20 pF During ADC acquisitionON-CHIP VOLTAGE REFERENCE V $0.47 \ \mu F \ from V_{REF}$ to AGNDOutput Voltage2.5V $Accuracy$ Accuracy ± 5 mV $T_A = 25^{\circ}C$ Power Supply Rejection Ratio75dBOutput Impedance70 Ω $T_A = 25^{\circ}C$ Input Voltage Range0.625 AV_{DD} V EXTERNAL REFERENCE INPUTms $T_A = 25^{\circ}C$ Input Voltage Range0.625 AV_{DD} V DAC CHANNEL SPECIFICATIONS V $R_L = 5 \ kQ, \ C_L = 100 \ pF$ DC Accuracy' ± 2 LSBGuaranteed monotonicDifferential Nonlinearity ± 11 LSBGuaranteed monotonicOffset Error ± 11 $\%$ $\%$ $\%$ of full scale on DACOANALOG OUTPUTS V M M M Output Voltage Range_0 $0 \ to DAC_{REF}$ V M Output Voltage Range_1 $0 \ to 2.5$ V M Output Voltage Range_1 $0 \ to 2.5$ V M Output Voltage Range_2 $0 \ to DAC_{NEC}$ V M Output Voltage Range_1 $0 \ to 2.5$ V M Output Voltage Range_1 $0 \ to 2.5$ V M Output Voltage Range_1 $0 \ to 2.5$ V M Output Vol | Input Voltage Ranges | | | | | |
| $ \begin{array}{ c c c } Single-Ended Mode & 0 to V_{REF} & V \\ Leakage Current & \pm 1 & \pm 6 & \mu A \\ Input Capacitance & 20 & \mu A \\ On-CHIP VOLTAGE REFERENCE & 2.5 & V \\ Accuracy & \pm 5 & mV & T_A = 25^\circ C \\ Accuracy & \pm 5 & mV & T_A = 25^\circ C \\ Power Supply Rejection Ratio & 75 & dB \\ Output Impedance & 70 & M & T_A = 25^\circ C \\ Internal V_{REF} Power-On Time & 1 & ms \\ EXTERNAL REFERENCE INPUT & T_A = 25^\circ C \\ Internal V_{REF} Power-On Time & 1 & ms \\ EXTERNAL REFERENCE INPUT & T_A = 25^\circ C \\ Input Voltage Range & 0.625 & AV_{DD} & V \\ DAC CHANNEL SPECIFICATIONS & V \\ DC Accuracy^7 & H & H \\ Relative Accuracy & \pm 2 & LSB \\ Differential Nonlinearity & \pm 1 \\ Relative Accuracy & \pm 1 & LSB \\ Differential Nonlinearity & \pm 1 \\ Offset Error & 1 & mV \\ Gain Error Mismatch & 0.1 & W & MV \\ Gain Error Mismatch & 0.1 & W & MV \\ Output Voltage Range_0 & 0 to DAC_{REF} & V \\ Output Voltage Range_1 & 0 to 2.5 & V \\ Output Voltage Range_2 & 0 to DACV_{DD} & V \\ \end{array}$ | Differential Mode | | | $V_{CM}{}^6\pm V_{REF}/2$ | V | |
| Leakage Current ± 1 ± 6 μA Input Capacitance20pFDuring ADC acquisitionON-CHIP VOLTAGE REFERENCE2.5V0.47 μ F from V _{REF} to AGNDOutput Voltage2.5VTA = 25°CAccuracy ± 40 ppm/°CPower Supply Rejection Ratio75dBOutput Impedance70 Ω $T_A = 25°C$ Internal V _{REF} Power-On Time1msEXTERNAL REFERENCE INPUTmsImput Voltage RangeInput Voltage Range0.625AV _{oD} VDAC CHANNEL SPECIFICATIONS $E^{\pm 1}$ LSBDC Accuracy ⁷ 12BitsRelative Accuracy ± 1 LSBOffset Error ± 1 LSBGain Error Mismatch0.1%Output Voltage Range_10 to DACserVDALGG OUTPUTSVDACser range: DACGND to DACV _{DO} Output Voltage Range_20 to DACV _{DO} VOutput Voltage Range_10 to DACV _{DO} VOutput Voltage Range_10 to DACV _{DO} V | Single-Ended Mode | | | $0 \text{ to } V_{\text{REF}}$ | V | |
| Input Capacitance20pFDuring ADC acquisitionON-CHIP VOLTAGE REFERENCE0.47 μF from Vner to AGNDOutput Voltage2.5V $Accuracy ± 5$ NPAccuracy±40ppm/°CReference Temperature Coefficient±40 $ppm/°C$ Power Supply Rejection Ratio75dBOutput Impedance70 Ω $T_A = 25°C$ Internal Vare Power-On Time1msEXTERNAL REFERENCE INPUTmsInput Voltage Range0.625AV _{DD} VDAC CHANNEL SPECIFICATIONS $C_{ACcuracy'}$ RL = 5 kΩ, CL = 100 pFDC Accuracy'±1LSBGaranteed monotonicOffset Error±1KS2.5 V internal referenceGain Error ⁶ ±1%% of full scale on DACOANALOG OUTPUTS C_{ACL} VDAC _{REF} range: DACGND to DACV _{DD} Output Voltage Range_00 to DAC _{REF} VDAC _{REF} range: DACGND to DACV _{DD} Output Voltage Range_10 to 2.5VDAC _{REF} range: DACGND to DACV _{DD} Output Voltage Range_20 to DACV _{DD} VDAC _{REF} range: DACGND to DACV _{DD} | Leakage Current | | ±1 | ±б | μΑ | |
| $\begin{array}{c c c c c c c c c c c c c c c c c c c $ | Input Capacitance | | 20 | | pF | During ADC acquisition |
| Output Voltage2.5VAccuracy ± 5 mVT_A = 25°CReference Temperature Coefficient ± 40 ppm/°CPower Supply Rejection Ratio75dBOutput Impedance70 Ω T_A = 25°CInternal V _{REF} Power-On Time1msEXTERNAL REFERENCE INPUTmsInput Voltage Range0.625AV _{DD} VDAC CHANNEL SPECIFICATIONSVDC Accuracy71BitsResolution12BitsRelative Accuracy ± 1 LSBDifferential Nonlinearity ± 15 mVOffset Error0.1%Gain Error ⁸ 0.1%Output Voltage Range_00 to DAC _{REF} VOutput Voltage Range_10 to DAC _{REF} VOutput Voltage Range_20 to DAC _{REF} VOutput Voltage Range_20 to DAC _{NDO} V | ON-CHIP VOLTAGE REFERENCE | | | | | 0.47 μF from V _{REF} to AGND |
| Accuracy ± 5 mV $T_A = 25^{\circ}$ CReference Temperature Coefficient ± 40 ppm/°CPower Supply Rejection Ratio75dBOutput Impedance70 Ω $T_A = 25^{\circ}$ CInternal V _{REF} Power-On Time1msEXTERNAL REFERENCE INPUTmsInput Voltage Range0.625AV _{DD} VDAC CHANNEL SPECIFICATIONS $K_{EF} = 5 k\Omega, C_L = 100 \text{ pF}$ DC Accuracy ⁷ 12BitsResolution12BitsRelative Accuracy ± 2 LSBDifferential Nonlinearity ± 1 LSBGain Error ⁸ 0.1%Gain Error Mismatch0.1%Output Voltage Range_00 to DAC _{REF} VOutput Voltage Range_10 to DAC _{NEF} VOutput Voltage Range_20 to DACV _{DD} VOutput Voltage Range_20 to DACV _{DD} V | Output Voltage | | 2.5 | | V | |
| Reference Temperature Coefficient ± 40 ppm/°CPower Supply Rejection Ratio75dBOutput Impedance70 Ω $T_A = 25^{\circ}$ CInternal V _{REF} Power-On Time1msEXTERNAL REFERENCE INPUTmsInput Voltage Range0.625AV _{DD} VDAC CHANNEL SPECIFICATIONS $R_L = 5 k\Omega, C_L = 100 pF$ DC Accuracy ⁷ 12BitsResolution12LSBDifferential Nonlinearity ± 1 LSBOffset Error ± 1 LSBGain Error ⁸ 0.1%Output Voltage Range_00 to DAC _{REF} VOutput Voltage Range_10 to DAC _{REF} VOutput Voltage Range_20 to DAC _{ND} V | Accuracy | | | ±5 | mV | $T_A = 25^{\circ}C$ |
| Power Supply Rejection Ratio75dBOutput Impedance70 Ω $T_A = 25^{\circ}C$ Internal VREF Power-On Time1msEXTERNAL REFERENCE INPUTms $T_A = 25^{\circ}C$ Input Voltage Range0.625 AV_{DD} VDAC CHANNEL SPECIFICATIONS V V DAC CHANNEL SPECIFICATIONS $R_L = 5 k\Omega, C_L = 100 pF$ DC Accuracy7 E^2 BitsResolution12BitsDifferential Nonlinearity ± 1 LSBOffset Error ± 1 SB Gain Error ⁸ 0.1%Gain Error Mismatch0.1%Output Voltage Range_00 to DAC_{REF}VOutput Voltage Range_10 to 2.5VOutput Voltage Range_20 to DACVDDVOutput Voltage Range_10 to 2.5VOutput Voltage Range_10 to 2.5VOutput Voltage Range_20 to DACVDDVOutput Impedance2 Ω | Reference Temperature Coefficient | | ±40 | | ppm/°C | |
| Output Impedance70 Ω TA = 25°CInternal VREF Power-On Time1msEXTERNAL REFERENCE INPUTmsInput Voltage Range0.625AV _{DD} VDAC CHANNEL SPECIFICATIONSVVDAC CHANNEL SPECIFICATIONSImput Voltage RangeNDAC CHANNEL SPECIFICATIONSImput Voltage RangeNDAC CHANNEL SPECIFICATIONSImput Voltage RangeNDAC CHANNEL SPECIFICATIONSImput Voltage RangeNDAC CHANNEL SPECIFICATIONSImput Voltage RangeNDifferential Nonlinearity12BitsDifferential Nonlinearity±1LSBDifferential Nonlinearity±1LSBGain Error ⁸ ±1%Gain Error Mismatch0.1%Output Voltage Range_00 to DACREFVOutput Voltage Range_10 to 2.5VOutput Voltage Range_20 to DACREFVOutput Voltage Range_20 to DACVDDVOutput Impedance2 Ω | Power Supply Rejection Ratio | | 75 | | dB | |
| Internal V _{REF} Power-On Time1msEXTERNAL REFERENCE INPUT Input Voltage Range0.625 AV_{DD} VDAC CHANNEL SPECIFICATIONSVVDAC CHANNEL SPECIFICATIONSIRt = 5 k Ω , CL = 100 pFDC Accuracy7IIIResolution12BitsRelative Accuracy ± 2 LSBDifferential Nonlinearity ± 1 LSBOffset Error ± 15 mVGain Error Mismatch0.1%Output Voltage Range_00 to DAC_{REF}VOutput Voltage Range_10 to 2.5VOutput Voltage Range_20 to DACV_DDVOutput Impedance2 Ω | Output Impedance | | 70 | | Ω | $T_A = 25^{\circ}C$ |
| EXTERNAL REFERENCE INPUT Input Voltage Range0.625 AV_{DD} VDAC CHANNEL SPECIFICATIONS DC Accuracy7RL = 5 kQ, CL = 100 pFDC Accuracy712BitsResolution12LSBDifferential Nonlinearity ± 2 LSBDifferential Nonlinearity ± 1 LSBGain Error 6 ± 1 %Gain Error 80.1%MALOG OUTPUTS0 to DAC_REFVOutput Voltage Range_00 to 2.5VOutput Voltage Range_10 to 2.5VOutput Voltage Range_20 to DACV_DDVOutput Impedance2Quitput Impedance | Internal V _{REF} Power-On Time | | 1 | | ms | |
| Input Voltage Range0.625 AV_{DD} VDAC CHANNEL SPECIFICATIONS $R_L = 5 k\Omega, C_L = 100 pF$ DC Accuracy7 $R_L = 5 k\Omega, C_L = 100 pF$ Resolution12BitsRelative Accuracy ± 2 LSBDifferential Nonlinearity ± 1 LSBGain Error8 ± 1 SB Gain Error8 0.1 $\%$ Output Voltage Range_0 $0 \text{ to } DAC_{REF}$ V Output Voltage Range_1 $0 \text{ to } 2.5$ V Output Voltage Range_2 $0 \text{ to } DAC_{ND}$ V Output Voltage Range_2 $0 \text{ to } DAC_{ND}$ V Output Voltage Range_2 $0 \text{ to } DAC_{ND}$ V | EXTERNAL REFERENCE INPUT | | | | | |
| DAC CHANNEL SPECIFICATIONS $R_L = 5 k\Omega, C_L = 100 pF$ DC Accuracy712BitsResolution12LSBRelative Accuracy ± 2 LSBDifferential Nonlinearity ± 1 LSBOffset Error ± 15 mV2.5 V internal referenceGain Error ⁸ ± 1 %Gain Error Mismatch0.1%% of full scale on DAC0ANALOG OUTPUTSVDAC _{REF} range: DACGND to DACV _{DD} VOutput Voltage Range_10 to 2.5VDAC _{REF} range: DACGND to DACV _{DD} Output Voltage Range_20 to DACV _{DD} VOutput Impedance2 Ω Ω | Input Voltage Range | 0.625 | | AV _{DD} | V | |
| DC Accuracy7IIIResolution12BitsRelative Accuracy±2LSBDifferential Nonlinearity±1LSBOffset Error±15mVGain Error ⁸ ±1%Gain Error Mismatch0.1%Output Voltage Range_00 to DAC_REFVOutput Voltage Range_10 to 2.5VOutput Voltage Range_20 to DACV_DDVOutput Impedance2Ω | DAC CHANNEL SPECIFICATIONS | | | | | $R_L = 5 \text{ k}\Omega$, $C_L = 100 \text{ pF}$ |
| Resolution12BitsRelative Accuracy±2LSBDifferential Nonlinearity±1LSBOffset Error±15mVGain Error ⁸ ±1%Gain Error Mismatch0.1%Output Voltage Range_00 to DACREFVOutput Voltage Range_10 to 2.5VOutput Voltage Range_20 to DACVDDOutput Impedance2 | DC Accuracy ⁷ | | | | | |
| Relative Accuracy±2LSBLSBDifferential Nonlinearity±1LSBGuaranteed monotonicOffset Error±15mV2.5 V internal referenceGain Error ⁸ ±1%%Gain Error Mismatch0.1%% of full scale on DAC0ANALOG OUTPUTSVDACREF range: DACGND to DACV_DDOutput Voltage Range_00 to DACREFVOutput Voltage Range_10 to 2.5VOutput Voltage Range_20 to DACV_DDVOutput Impedance2Ω | Resolution | | 12 | | Bits | |
| Differential Nonlinearity±1LSBGuaranteed monotonicOffset Error±15mV2.5 V internal referenceGain Error ⁸ ±1%Gain Error Mismatch0.1%% of full scale on DAC0ANALOG OUTPUTSV%Output Voltage Range_00 to DACREFVOutput Voltage Range_10 to 2.5VOutput Voltage Range_20 to DACVDDVOutput Impedance2Ω | Relative Accuracy | | ±2 | | LSB | |
| Offset Error±15mV2.5 V internal referenceGain Error ⁸ ±1%Gain Error Mismatch0.1%% of full scale on DAC0ANALOG OUTPUTSV%Output Voltage Range_00 to DACREFVOutput Voltage Range_10 to 2.5VOutput Voltage Range_20 to DACVDDOutput Impedance2Ω | Differential Nonlinearity | | | ±1 | LSB | Guaranteed monotonic |
| Gain Error ⁸ ±1%Gain Error Mismatch0.1%% of full scale on DAC0ANALOG OUTPUTSOutput Voltage Range_00 to DACREFVDACREF range: DACGND to DACVDDOutput Voltage Range_10 to 2.5VOutput Voltage Range_20 to DACVDDVOutput Impedance2Ω | Offset Error | | | ±15 | mV | 2.5 V internal reference |
| Gain Error Mismatch0.1%% of full scale on DAC0ANALOG OUTPUTS </td <td>Gain Error⁸</td> <td></td> <td></td> <td>±1</td> <td>%</td> <td></td> | Gain Error ⁸ | | | ±1 | % | |
| ANALOG OUTPUTS V DAC _{REF} range: DACGND to DACV _{DD} Output Voltage Range_0 0 to DAC _{REF} V DAC _{REF} range: DACGND to DACV _{DD} Output Voltage Range_1 0 to 2.5 V Output Voltage Range_2 0 to DACV _{DD} V Output Impedance 2 Ω | Gain Error Mismatch | | 0.1 | | % | % of full scale on DAC0 |
| Output Voltage Range_00 to DACREFVDACREF range: DACGND to DACVDDOutput Voltage Range_10 to 2.5VOutput Voltage Range_20 to DACVDDVOutput Impedance2Ω | ANALOG OUTPUTS | | | | | |
| Output Voltage Range_1 0 to 2.5 V Output Voltage Range_2 0 to DACV _{DD} V Output Impedance 2 Ω | Output Voltage Range_0 | | 0 to DAC _{REF} | | V | DAC _{REF} range: DACGND to DACV _{DD} |
| Output Voltage Range_2 0 to DACV _{DD} V Output Impedance 2 Ω | Output Voltage Range_1 | | 0 to 2.5 | | V | - |
| Output Impedance 2 Ω | Output Voltage Range_2 | | 0 to DACV _{DD} | | V | |
| | Output Impedance | | 2 | | Ω | |

TIMING SPECIFICATIONS

Table 2. External Memory Write Cycle

| Parameter | Min | Тур | Max | Unit |
|-----------------------------------|-----|--|-----|------|
| CLK ¹ | | UCLK | | |
| t _{MS_AFTER_CLKH} | 0 | | 4 | ns |
| t ADDR_AFTER_CLKH | 4 | | 8 | ns |
| t _{AE_H_AFTER_MS} | | ½ CLK | | |
| t _{AE} | | $(XMxPAR[14:12] + 1) \times CLK$ | | |
| t _{HOLD_ADDR_AFTER_AE_L} | | $\frac{1}{2}$ CLK + (!XMxPAR[10]) × CLK | | |
| thold_addr_before_wr_l | | $(!XMxPAR[8]) \times CLK$ | | |
| t _{wr_l_after_ae_l} | | 1/2 CLK + (!XMxPAR[10] + !XMxPAR[8]) × CLK | | |
| tdata_after_wr_l | 8 | | 12 | ns |
| t _{wr} | | $(XMxPAR[7:4] + 1) \times CLK$ | | |
| t wr_h_after_clkh | 0 | | 4 | ns |
| thold_data_after_wr_h | | $(!XMxPAR[8]) \times CLK$ | | |
| tben_after_ae_l | | 1/2 CLK | | |
| trelease_ms_after_wr_h | | $(!XMxPAR[8] + 1) \times CLK$ | | |

¹ See Table 78.



Figure 12. External Memory Write Cycle (See Table 78)

Table 4. I²C Timing in Fast Mode (400 kHz)

| | | | ave | Master | |
|-------------------------|--|-----|-----|--------|------|
| Parameter | Description | Min | Max | Тур | Unit |
| tL | SCL low pulse width ¹ | 200 | | 1360 | ns |
| tн | SCL high pulse width ¹ | 100 | | 1140 | ns |
| t _{shd} | Start condition hold time | 300 | | | ns |
| t dsu | Data setup time | 100 | | 740 | ns |
| t _{DHD} | Data hold time | 0 | | 400 | ns |
| t _{RSU} | Setup time for repeated start | 100 | | | ns |
| t _{PSU} | Stop condition setup time | 100 | | 400 | ns |
| t _{BUF} | Bus-free time between a stop condition and a start condition | 1.3 | | | μs |
| t _R | Rise time for both SCL and SDA | | 300 | 200 | ns |
| tF | Fall time for both SCL and SDA | | 300 | | ns |
| t _{SUP} | Pulse width of spike suppressed | | 50 | | ns |

 1 t_{HCLK} depends on the clock divider or CD bits in the POWCON MMR. t_{HCLK} = t_{UCLK}/2^{CD}; see Figure 67.

Table 5. I²C Timing in Standard Mode (100 kHz)

| | | Slave Ma | | Master | |
|------------------|--|----------|------|--------|------|
| Parameter | Description | Min | Max | Тур | Unit |
| t∟ | SCL low pulse width ¹ | 4.7 | | | μs |
| t _H | SCL high pulse width ¹ | 4.0 | | | ns |
| t _{shd} | Start condition hold time | 4.0 | | | μs |
| t _{DSU} | Data setup time | 250 | | | ns |
| t DHD | Data hold time | 0 | 3.45 | | μs |
| t _{RSU} | Setup time for repeated start | 4.7 | | | μs |
| t PSU | Stop condition setup time | 4.0 | | | μs |
| t _{BUF} | Bus-free time between a stop condition and a start condition | 4.7 | | | μs |
| t _R | Rise time for both SCL and SDA | | 1 | | μs |
| t _F | Fall time for both SCL and SDA | | 300 | | ns |

 1 t_{HCLK} depends on the clock divider or CD bits in the POWCON MMR. t_{HCLK} = t_{UCLK}/2^{CD}; see Figure 67.



Figure 14. I²C Compatible Interface Timing

| Parameter | Description | Min | Тур | Max | Unit |
|------------------|---|----------------------------|--------------------------------|------|------|
| t _{sL} | SCLK low pulse width ¹ | | $(SPIDIV + 1) \times t_{HCLK}$ | | ns |
| t _{sн} | SCLK high pulse width ¹ | | $(SPIDIV + 1) \times t_{HCLK}$ | | ns |
| t _{DAV} | Data output valid after SCLK edge | | | 25 | ns |
| t _{DSU} | Data input setup time before SCLK edge ² | $1 \times t_{\text{UCLK}}$ | | | ns |
| t DHD | Data input hold time after SCLK edge ² | $2 \times t_{\text{UCLK}}$ | | | ns |
| t _{DF} | Data output fall time | | 5 | 12.5 | ns |
| t _{DR} | Data output rise time | | 5 | 12.5 | ns |
| t _{sr} | SCLK rise time | | 5 | 12.5 | ns |
| t _{SF} | SCLK fall time | | 5 | 12.5 | ns |

Table 6. SPI Master Mode Timing (Phase Mode = 1)

¹ t_{HCLK} depends on the clock divider or CD bits in the POWCONMMR. t_{HCLK} = $t_{UCLK}/2^{CD}$; see Figure 67. ² t_{UCLK} = 23.9 ns. It corresponds to the 41.78 MHz internal clock from the PLL before the clock divider; see Figure 67.





| Parameter | Description | Min | Тур | Max | Unit | | |
|------------------|---|----------------------------|--------------------------------|------|------|--|--|
| tsL | SCLK low pulse width ¹ | | $(SPIDIV + 1) \times t_{HCLK}$ | | ns | | |
| tsн | SCLK high pulse width ¹ | | $(SPIDIV + 1) \times t_{HCLK}$ | | ns | | |
| t _{DAV} | Data output valid after SCLK edge | | | 25 | ns | | |
| tdosu | Data output setup before SCLK edge | | | 75 | ns | | |
| t dsu | Data input setup time before SCLK edge ² | $1 \times t_{UCLK}$ | | | ns | | |
| t dhd | Data input hold time after SCLK edge ² | $2 \times t_{\text{UCLK}}$ | | | ns | | |
| t _{DF} | Data output fall time | | 5 | 12.5 | ns | | |
| t _{DR} | Data output rise time | | 5 | 12.5 | ns | | |
| t _{sr} | SCLK rise time | | 5 | 12.5 | ns | | |
| t _{SF} | SCLK fall time | | 5 | 12.5 | ns | | |

Table 7. SPI Master Mode Timing (Phase Mode = 0)

 1 t_{HCLK} depends on the clock divider or CD bits in the POWCONMMR. t_{HCLK} = t_{UCLK}/2^{CD}; see Figure 67.

 2 t_{UCLK} = 23.9 ns. It corresponds to the 41.78 MHz internal clock from the PLL before the clock divider; see Figure 67.



Figure 16. SPI Master Mode Timing (Phase Mode = 0)

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

ADuC7019/ADuC7020/ADuC7021/ADuC7022





| Pin No. | | | | |
|-----------|------|------|---|--|
| 7019/7020 | 7021 | 7022 | Mnemonic | Description |
| 22 | 22 | 21 | P2.0/SPM9/PLAO[5]/CONV _{START} | Serial Port Multiplexed. General-Purpose Input and Output Port 2.0/UART/ Programmable Logic Array Output Element 5/Start Conversion Input Signal for ADC. |
| 23 | 23 | 22 | P0.7/ECLK/XCLK/SPM8/PLAO[4] | Serial Port Multiplexed. General-Purpose Input and Output Port 0.7/ Output for External Clock Signal/Input to the Internal Clock Generator Circuits/UART/ Programmable Logic Array Output Element 4. |
| 24 | 24 | 23 | XCLKO | Output from the Crystal Oscillator Inverter. |
| 25 | 25 | 24 | XCLKI | Input to the Crystal Oscillator Inverter and Input to the Internal Clock Generator Circuits. |
| 26 | 26 | 25 | P1.7/SPM7/PLAO[0] | Serial Port Multiplexed. General-Purpose Input and Output Port 1.7/UART, SPI/Programmable Logic Array Output Element 0. |
| 27 | 27 | 26 | P1.6/SPM6/PLAI[6] | Serial Port Multiplexed. General-Purpose Input and Output Port 1.6/UART, SPI/Programmable Logic Array Input Element 6. |
| 28 | 28 | 27 | P1.5/SPM5/PLAI[5]/IRQ3 | Serial Port Multiplexed. General-Purpose Input and Output Port 1.5/UART, SPI/Programmable Logic Array Input Element 5/External Interrupt Request 3, Active High. |
| 29 | 29 | 28 | P1.4/SPM4/PLAI[4]/IRQ2 | Serial Port Multiplexed. General-Purpose Input and Output Port 1.4/UART, SPI/Programmable Logic Array Input Element 4/External Interrupt Request 2, Active High. |
| 30 | 30 | 29 | P1.3/SPM3/PLAI[3] | Serial Port Multiplexed. General-Purpose Input and Output Port 1.3/UART, I2C1/Programmable Logic Array Input Element 3. |
| 31 | 31 | 30 | P1.2/SPM2/PLAI[2] | Serial Port Multiplexed. General-Purpose Input and Output Port 1.2/UART, I2C1/Programmable Logic Array Input Element 2. |
| 32 | 32 | 31 | P1.1/SPM1/PLAI[1] | Serial Port Multiplexed. General-Purpose Input and Output Port 1.1/UART, I2C0/Programmable Logic Array Input Element 1. |
| 33 | 33 | 32 | P1.0/T1/SPM0/PLAI[0] | Serial Port Multiplexed. General-Purpose Input and Output Port 1.0/ Timer1 Input/UART, I2C0/Programmable Logic Array Input Element 0. |
| 34 | - | - | P4.2/PLAO[10] | General-Purpose Input and Output Port 4.2/Programmable Logic Array Output Element 10. |
| 35 | 34 | 33 | V _{REF} | 2.5 V Internal Voltage Reference. Must be connected to a 0.47 μF capacitor when using the internal reference. |
| 36 | 35 | 34 | AGND | Analog Ground. Ground reference point for the analog circuitry. |
| 37 | 36 | 35 | AV _{DD} | 3.3 V Analog Power. |
| 0 | 0 | 0 | EP | Exposed Pad. The pin configuration for the ADuC7019/ADuC7020/ ADuC7021/ADuC7022 has an exposed pad that must be soldered for mechanical purposes and left unconnected. |

| Pin No. | Mnemonic | Description |
|---------|------------------------------------|--|
| 37 | P3.6/PWM _{TRIP} /PLAI[14] | General-Purpose Input and Output Port 3.6/PWM Safety Cutoff/Programmable Logic Array Input Element 14. |
| 38 | P3.7/PWM _{SYNC} /PLAI[15] | General-Purpose Input and Output Port 3.7/PWM Synchronization Input and Output/ Programmable Logic Array Input Element 15. |
| 39 | P1.7/SPM7/PLAO[0] | Serial Port Multiplexed. General-Purpose Input and Output Port 1.7/UART, SPI/Programmable Logic Array Output Element 0. |
| 40 | P1.6/SPM6/PLAI[6] | Serial Port Multiplexed. General-Purpose Input and Output Port 1.6/UART, SPI/Programmable Logic Array Input Element 6. |
| 41 | IOGND | Ground for GPIO (see Table 78). Typically connected to DGND. |
| 42 | IOV _{DD} | 3.3 V Supply for GPIO (see Table 78) and Input of the On-Chip Voltage Regulator. |
| 43 | P4.0/PLAO[8] | General-Purpose Input and Output Port 4.0/Programmable Logic Array Output Element 8. |
| 44 | P4.1/PLAO[9] | General-Purpose Input and Output Port 4.1/Programmable Logic Array Output Element 9. |
| 45 | P1.5/SPM5/PLAI[5]/IRQ3 | Serial Port Multiplexed. General-Purpose Input and Output Port 1.5/UART, SPI/Programmable Logic Array Input Element 5/External Interrupt Request 3, Active High. |
| 46 | P1.4/SPM4/PLAI[4]/IRQ2 | Serial Port Multiplexed. General-Purpose Input and Output Port 1.4/UART, SPI/Programmable Logic Array Input Element 4/External Interrupt Request 2, Active High. |
| 47 | P1.3/SPM3/PLAI[3] | Serial Port Multiplexed. General-Purpose Input and Output Port 1.3/UART, I2C1/Programmable Logic Array Input Element 3. |
| 48 | P1.2/SPM2/PLAI[2] | Serial Port Multiplexed. General-Purpose Input and Output Port 1.2/UART, I2C1/Programmable Logic Array Input Element 2. |
| 49 | P1.1/SPM1/PLAI[1] | Serial Port Multiplexed. General-Purpose Input and Output Port 1.1/UART, I2CO/Programmable Logic Array Input Element 1. |
| 50 | P1.0/T1/SPM0/PLAI[0] | Serial Port Multiplexed. General-Purpose Input and Output Port 1.0/Timer1 Input/UART, I2C0/ Programmable Logic Array Input Element 0. |
| 51 | P4.2/PLAO[10] | General-Purpose Input and Output Port 4.2/Programmable Logic Array Output Element 10. |
| 52 | P4.3/PLAO[11] | General-Purpose Input and Output Port 4.3/Programmable Logic Array Output Element 11. |
| 53 | P4.4/PLAO[12] | General-Purpose Input and Output Port 4.4/Programmable Logic Array Output Element 12. |
| 54 | P4.5/PLAO[13] | General-Purpose Input and Output Port 4.5/Programmable Logic Array Output Element 13. |
| 55 | V _{REF} | 2.5 V Internal Voltage Reference. Must be connected to a 0.47 μF capacitor when using the internal reference. |
| 56 | DAC _{REF} | External Voltage Reference for the DACs. Range: DACGND to $DACV_{DD}$. |
| 57 | DACGND | Ground for the DAC. Typically connected to AGND. |
| 58 | AGND | Analog Ground. Ground reference point for the analog circuitry. |
| 59 | AV _{DD} | 3.3 V Analog Power. |
| 60 | | 3.3 V Power Supply for the DACs. Must be connected to AV_{DD} . |
| 61 | ADC0 | Single-Ended or Differential Analog Input 0. |
| 62 | ADC1 | Single-Ended or Differential Analog Input 1. |
| 63 | ADC2/CMP0 | Single-Ended or Differential Analog Input 2/Comparator Positive Input. |
| 64 | ADC3/CMP1 | Single-Ended or Differential Analog Input 3/Comparator Negative Input. |
| 0 | EP | Exposed Pad. The pin configuration for the ADuC7024/ADuC7025 LFCSP_VQ has an exposed pad that must be soldered for mechanical purposes and left unconnected. |

TERMINOLOGY ADC SPECIFICATIONS

Integral Nonlinearity (INL)

The maximum deviation of any code from a straight line passing through the endpoints of the ADC transfer function. The endpoints of the transfer function are zero scale, a point ½ LSB below the first code transition, and full scale, a point ½ LSB above the last code transition.

Differential Nonlinearity (DNL)

The difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Offset Error

The deviation of the first code transition (0000 . . . 000) to (0000 . . . 001) from the ideal, that is, $+\frac{1}{2}$ LSB.

Gain Error

The deviation of the last code transition from the ideal AIN voltage (full scale -1.5 LSB) after the offset error has been adjusted out.

Signal to (Noise + Distortion) Ratio (SINAD)

The measured ratio of signal to (noise + distortion) at the output of the ADC. The signal is the rms amplitude of the fundamental. Noise is the rms sum of all nonfundamental signals up to half the sampling frequency ($f_s/2$), excluding dc.

The ratio is dependent upon the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise.

The theoretical signal to (noise + distortion) ratio for an ideal N-bit converter with a sine wave input is given by

Signal to (Noise + Distortion) = (6.02 N + 1.76) dB

Thus, for a 12-bit converter, this is 74 dB.

Total Harmonic Distortion (THD)

The ratio of the rms sum of the harmonics to the fundamental.

DAC SPECIFICATIONS

Relative Accuracy

Otherwise known as endpoint linearity, relative accuracy is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero error and full-scale error.

Voltage Output Settling Time

The amount of time it takes the output to settle to within a 1 LSB level for a full-scale input change.

OVERVIEW OF THE ARM7TDMI CORE

The ARM7° core is a 32-bit reduced instruction set computer (RISC). It uses a single 32-bit bus for instruction and data. The length of the data can be eight bits, 16 bits, or 32 bits. The length of the instruction word is 32 bits.

The ARM7TDMI is an ARM7 core with four additional features.

- T support for the thumb (16-bit) instruction set.
- D support for debug.
- M support for long multiplications.
- I includes the EmbeddedICE module to support embedded system debugging.

THUMB MODE (T)

An ARM instruction is 32 bits long. The ARM7TDMI processor supports a second instruction set that is compressed into 16 bits, called the thumb instruction set. Faster execution from 16-bit memory and greater code density can usually be achieved by using the thumb instruction set instead of the ARM instruction set, which makes the ARM7TDMI core particularly suitable for embedded applications.

However, the thumb mode has two limitations.

- Thumb code typically requires more instructions for the same job. As a result, ARM code is usually best for maximizing the performance of time-critical code.
- The thumb instruction set does not include some of the instructions needed for exception handling, which automatically switches the core to ARM code for exception handling.

See the ARM7TDMI user guide for details on the core architecture, the programming model, and both the ARM and ARM thumb instruction sets.

LONG MULTIPLY (M)

The ARM7TDMI instruction set includes four extra instructions that perform 32-bit by 32-bit multiplication with a 64-bit result, and 32-bit by 32-bit multiplication-accumulation (MAC) with a 64-bit result. These results are achieved in fewer cycles than required on a standard ARM7 core.

EmbeddedICE (I)

EmbeddedICE provides integrated on-chip support for the core. The EmbeddedICE module contains the breakpoint and watchpoint registers that allow code to be halted for debugging purposes. These registers are controlled through the JTAG test port.

When a breakpoint or watchpoint is encountered, the processor halts and enters debug state. Once in a debug state, the processor registers can be inspected as well as the Flash/EE, SRAM, and memory mapped registers.

EXCEPTIONS

ARM supports five types of exceptions and a privileged processing mode for each type. The five types of exceptions are

- Normal interrupt or IRQ, which is provided to service general-purpose interrupt handling of internal and external events.
- Fast interrupt or FIQ, which is provided to service data transfers or communication channels with low latency. FIQ has priority over IRQ.
- Memory abort.
- Attempted execution of an undefined instruction.
- Software interrupt instruction (SWI), which can be used to make a call to an operating system.

Typically, the programmer defines interrupt as IRQ, but for higher priority interrupt, that is, faster response time, the programmer can define interrupt as FIQ.

ARM REGISTERS

ARM7TDMI has a total of 37 registers: 31 general-purpose registers and six status registers. Each operating mode has dedicated banked registers.

When writing user-level programs, 15 general-purpose 32-bit registers (R0 to R14), the program counter (R15), and the current program status register (CPSR) are usable. The remaining registers are used for system-level programming and exception handling only.

When an exception occurs, some of the standard registers are replaced with registers specific to the exception mode. All exception modes have replacement banked registers for the stack pointer (R13) and the link register (R14), as represented in Figure 44. The fast interrupt mode has more registers (R8 to R12) for fast interrupt processing. This means that interrupt processing can begin without the need to save or restore these registers and, thus, save critical time in the interrupt handling process.



More information relative to the programmer's model and the ARM7TDMI core architecture can be found in the following materials from ARM:

- DDI0029G, ARM7TDMI Technical Reference Manual
- DDI-0100, ARM Architecture Reference Manual

INTERRUPT LATENCY

The worst-case latency for a fast interrupt request (FIQ) consists of the following:

- The longest time the request can take to pass through the synchronizer
- The time for the longest instruction to complete (the longest instruction is an LDM) that loads all the registers including the PC
- The time for the data abort entry
- The time for FIQ entry

At the end of this time, the ARM7TDMI executes the instruction at 0x1C (FIQ interrupt vector address). The maximum total time is 50 processor cycles, which is just under 1.2 µs in a system using a continuous 41.78 MHz processor clock.

The maximum interrupt request (IRQ) latency calculation is similar but must allow for the fact that FIQ has higher priority and may delay entry into the IRQ handling routine for an arbitrary length of time. This time can be reduced to 42 cycles if the LDM command is not used. Some compilers have an option to compile without using this command. Another option is to run the part in thumb mode where the time is reduced to 22 cycles.

The minimum latency for FIQ or IRQ interrupts is a total of five cycles, which consist of the shortest time the request can take through the synchronizer plus the time to enter the exception mode.

Note that the ARM7TDMI always runs in ARM (32-bit) mode when in privileged modes, for example, when executing interrupt service routines.

MEMORY ORGANIZATION

The ADuC7019/20/21/22/24/25/26/27/28/29 incorporate two separate blocks of memory: 8 kB of SRAM and 64 kB of on-chip Flash/EE memory. The 62 kB of on-chip Flash/EE memory is available to the user, and the remaining 2 kB are reserved for the factory-configured boot page. These two blocks are mapped as shown in Figure 45.



Figure 45. Physical Memory Map

Note that by default, after a reset, the Flash/EE memory is mirrored at Address 0x00000000. It is possible to remap the SRAM at Address 0x00000000 by clearing Bit 0 of the REMAP MMR. This remap function is described in more detail in the Flash/EE Memory section.

MEMORY ACCESS

The ARM7 core sees memory as a linear array of a 2^{32} byte location where the different blocks of memory are mapped as outlined in Figure 45.

The ADuC7019/20/21/22/24/25/26/27/28/29 memory organizations are configured in little endian format, which means that the least significant byte is located in the lowest byte address, and the most significant byte is in the highest byte address.



FLASH/EE MEMORY

The total 64 kB of Flash/EE memory is organized as $32 \text{ k} \times 16$ bits; 31 k × 16 bits is user space and 1 k × 16 bits is reserved for the on-chip kernel. The page size of this Flash/EE memory is 512 bytes.

Sixty-two kilobytes of Flash/EE memory are available to the user as code and nonvolatile data memory. There is no distinction between data and program because ARM code shares the same space. The real width of the Flash/EE memory is 16 bits, which means that in ARM mode (32-bit instruction), two accesses to the Flash/EE are necessary for each instruction fetch. It is therefore recommended to use thumb mode when executing from Flash/EE memory for optimum access speed. The maximum access speed for the Flash/EE memory is 41.78 MHz in thumb mode and 20.89 MHz in full ARM mode. More details about Flash/EE access time are outlined in the Execution Time from SRAM and Flash/EE section.

SRAM

Eight kilobytes of SRAM are available to the user, organized as $2 \text{ k} \times 32$ bits, that is, two words. ARM code can run directly from SRAM at 41.78 MHz, given that the SRAM array is configured as a 32-bit wide memory array. More details about SRAM access time are outlined in the Execution Time from SRAM and Flash/EE section.

MEMORY MAPPED REGISTERS

The memory mapped register (MMR) space is mapped into the upper two pages of the memory array and accessed by indirect addressing through the ARM7 banked registers.

The MMR space provides an interface between the CPU and all on-chip peripherals. All registers, except the core registers, reside in the MMR area. All shaded locations shown in Figure 47 are unoccupied or reserved locations and should not be accessed by user software. Table 16 shows the full MMR memory map.

The access time for reading from or writing to an MMR depends on the advanced microcontroller bus architecture (AMBA) bus used to access the peripheral. The processor has two AMBA buses: the advanced high performance bus (AHB) used for system modules and the advanced peripheral bus (APB) used for lower performance peripheral. Access to the AHB is one cycle, and access to the APB is two cycles. All peripherals on the ADuC7019/20/21/22/24/25/26/27/28/29 are on the APB except the Flash/EE memory, the GPIOs (see Table 78), and the PWM.

Table 18. ADCCON MMR Bit Designations

| Bit | Value | Description |
|-------|-------|--|
| 15:13 | | Reserved. |
| 12:10 | | ADC clock speed. |
| | 000 | fADC/1. This divider is provided to obtain 1 MSPS ADC with an external clock <41.78 MHz. |
| | 001 | fADC/2 (default value). |
| | 010 | fADC/4. |
| | 011 | fADC/8. |
| | 100 | fADC/16. |
| | 101 | fADC/32. |
| 9:8 | | ADC acquisition time. |
| | 00 | Two clocks. |
| | 01 | Four clocks. |
| | 10 | Eight clocks (default value). |
| | 11 | 16 clocks. |
| 7 | | Enable start conversion. |
| | | Set by the user to start any type of conversion command. Cleared by the user to disable a start conversion (clearing this bit does not stop the ADC when continuously converting). |
| 6 | | Beserved |
| U | | |
| 5 | | ADC power control. |
| | | Set by the user to place the ADC in normal mode (the ADC must be powered up for at least 5 µs before it converts correctly). Cleared by the user to place the ADC in power-down mode. |
| 4:3 | | Conversion mode. |
| | 00 | Single-ended mode. |
| | 01 | Differential mode. |
| | 10 | Pseudo differential mode. |
| | 11 | Reserved. |
| 2:0 | | Conversion type. |
| | 000 | Enable CONV _{START} pin as a conversion input. |
| | 001 | Enable Timer1 as a conversion input. |
| | 010 | Enable Timer0 as a conversion input. |
| | 011 | Single software conversion. Sets to 000 after conversion (note that Bit 7 of ADCCON MMR should be cleared after starting a single software conversion to avoid <u>further</u> conversions triggered by the <u>CONV_{START}</u> pin). |
| | 100 | Continuous software conversion. |
| | 101 | PLA conversion. |
| | Other | Reserved. |

Table 19. ADCCP Register

_

| | Deluarevalue | Access |
|------------------|--------------|--------|
| ADCCP 0xFFFF0504 | 0x00 | R/W |

ADCCP is an ADC positive channel selection register. This MMR is described in Table 20.

Table 20. ADCCP¹ MMR Bit Designation

| Bit | Value | Description |
|-----|--------|---|
| 7:5 | | Reserved. |
| 4:0 | | Positive channel selection bits. |
| | 00000 | ADC0. |
| | 00001 | ADC1. |
| | 00010 | ADC2. |
| | 00011 | ADC3. |
| | 00100 | ADC4. |
| | 00101 | ADC5. |
| | 00110 | ADC6. |
| | 00111 | ADC7. |
| | 01000 | ADC8. |
| | 01001 | ADC9. |
| | 01010 | ADC10. |
| | 01011 | ADC11. |
| | 01100 | DAC0/ADC12. |
| | 01101 | DAC1/ADC13. |
| | 01110 | DAC2/ADC14. |
| | 01111 | DAC3/ADC15. |
| | 10000 | Temperature sensor. |
| | 10001 | AGND (self-diagnostic feature). |
| | 10010 | Internal reference (self-diagnostic feature). |
| | 10011 | AV _{DD} /2. |
| | Others | Reserved. |

¹ ADC and DAC channel availability depends on the part model. See Ordering Guide for details.

Table 21. ADCCN Register

| Name | Address | Default Value | Access |
|-------|------------|---------------|--------|
| ADCCN | 0xFFFF0508 | 0x01 | R/W |

ADCCN is an ADC negative channel selection register. This MMR is described in Table 22.

Pseudo Differential Mode

In pseudo differential mode, Channel– is linked to the V_{IN}- pin of the ADuC7019/20/21/22/24/25/26/27/28/29. SW2 switches between A (Channel–) and B (V_{REF}). The V_{IN}- pin must be connected to ground or a low voltage. The input signal on V_{IN+} can then vary from V_{IN}- to V_{REF} + V_{IN}-. Note that V_{IN}- must be chosen so that V_{REF} + V_{IN}- does not exceed AV_{DD}.



Figure 56. ADC in Pseudo Differential Mode

Single-Ended Mode

In single-ended mode, SW2 is always connected internally to ground. The $V_{\rm IN-}$ pin can be floating. The input signal range on $V_{\rm IN+}$ is 0 V to $V_{\rm REF}.$



Figure 57. ADC in Single-Ended Mode

Analog Input Structure

Figure 58 shows the equivalent circuit of the analog input structure of the ADC. The four diodes provide ESD protection for the analog inputs. Care must be taken to ensure that the analog input signals never exceed the supply rails by more than 300 mV; exceeding 300 mV causes these diodes to become forwardbiased and start conducting into the substrate. These diodes can conduct up to 10 mA without causing irreversible damage to the part.

The C1 capacitors in Figure 58 are typically 4 pF and can be primarily attributed to pin capacitance. The resistors are lumped components made up of the on resistance of the switches. The value of these resistors is typically about 100 Ω . The C2 capacitors are the ADC's sampling capacitors and typically have a capacitance of 16 pF.



Figure 58. Equivalent Analog Input Circuit Conversion Phase: Switches Open, Track Phase: Switches Closed

For ac applications, removing high frequency components from the analog input signal is recommended by using an RC lowpass filter on the relevant analog input pins. In applications where harmonic distortion and signal-to-noise ratio are critical, the analog input should be driven from a low impedance source. Large source impedances significantly affect the ac performance of the ADC. This can necessitate the use of an input buffer amplifier. The choice of the op amp is a function of the particular application. Figure 59 and Figure 60 give an example of an ADC front end.



Figure 59. Buffering Single-Ended/Pseudo Differential Input



Figure 60. Buffering Differential Inputs

When no amplifier is used to drive the analog input, the source impedance should be limited to values lower than 1 k Ω . The maximum source impedance depends on the amount of total harmonic distortion (THD) that can be tolerated. The THD increases as the source impedance increases and the performance degrades.

DRIVING THE ANALOG INPUTS

Internal or external references can be used for the ADC. In the differential mode of operation, there are restrictions on the common-mode input signal (V_{CM}), which is dependent upon the reference value and supply voltage used to ensure that the signal remains within the supply rails. Table 28 gives some calculated V_{CM} minimum and V_{CM} maximum values.

Data Sheet

The serial communication adopts an asynchronous protocol, which supports various word lengths, stop bits, and parity generation options selectable in the configuration register.

Baud Rate Generation

There are two ways of generating the UART baud rate, normal 450 UART baud rate generation and the fractional divider.

Normal 450 UART Baud Rate Generation

The baud rate is a divided version of the core clock using the values in the COMDIV0 and COMDIV1 MMRs (16-bit value, DL).

Baud Rate =
$$\frac{41.78 \text{ MHz}}{2^{\text{CD}} - 16 \times 2 \times \text{DL}}$$

Table 93 gives some common baud rate values.

| Table 93. Baud Rate Using the Normal Baud Rate Generator |
|--|
|--|

| Baud Rate | CD | DL | Actual Baud Rate | % Error |
|-----------|----|------|------------------|---------|
| 9600 | 0 | 0x88 | 9600 | 0 |
| 19,200 | 0 | 0x44 | 19,200 | 0 |
| 115,200 | 0 | 0x0B | 118,691 | 3 |
| 9600 | 3 | 0x11 | 9600 | 0 |
| 19,200 | 3 | 0x08 | 20,400 | 6.25 |
| 115,200 | 3 | 0x01 | 163,200 | 41.67 |

Fractional Divider

The fractional divider, combined with the normal baud rate generator, produces a wider range of more accurate baud rates.



Figure 75. Baud Rate Generation Options

Calculation of the baud rate using fractional divider is as follows:

Baud Rate =
$$\frac{41.78 \text{ MHz}}{2^{CD} \times 16 \times DL \times 2 \times \left(M + \frac{N}{2048}\right)}$$
$$M + \frac{N}{2048} = \frac{41.78 \text{ MHz}}{\text{Baud Rate} \times 2^{CD} \times 16 \times \text{DL} \times 2}$$

For example, generation of 19,200 baud with CD bits = 3 (Table 93 gives DL = 0x08) is

$$M + \frac{N}{2048} = \frac{41.78 \text{ MHz}}{19200 \times 2^3 \times 16 \times 8 \times 2}$$

$$M + \frac{N}{2048} = 1.06$$

where:

M = 1 $N = 0.06 \times 2048 = 128$

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Baud Rate =
$$\frac{41.78 \text{ MHz}}{2}$$

$$2^{3} \times 16 \times 8 \times 2 \times \frac{128}{2048}$$

where:

Baud Rate = 19,200 bps

Error = 0%, compared to 6.25% with the normal baud rate generator.

UART Register Definitions

The UART interface consists of 12 registers: COMTX, COMRX, COMDIV0, COMIEN0, COMDIV1, COMIID0, COMCON0, COMCON1, COMSTA0, COMSTA1, COMSCR, and COMDIV2.

Table 94. COMTX Register

| Name | Address | Default Value | Access |
|-------|------------|---------------|--------|
| COMTX | 0xFFFF0700 | 0x00 | R/W |

COMTX is an 8-bit transmit register.

Table 95. COMRX Register

| Name | Address | Default Value | Access |
|-------|------------|---------------|--------|
| COMRX | 0xFFFF0700 | 0x00 | R |

COMRX is an 8-bit receive register.

Table 96. COMDIV0 Register

| Name Address | | Default Value | Access |
|--------------|------------|---------------|--------|
| COMDIV0 | 0xFFFF0700 | 0x00 | R/W |

COMDIV0 is a low byte divisor latch. COMTX, COMRX, and COMDIV0 share the same address location. COMTX and COMRX can be accessed when Bit 7 in the COMCON0 register is cleared. COMDIV0 can be accessed when Bit 7 of COMCON0 is set.

Table 97. COMIEN0 Register

| Name | Address | Default Value | Access |
|---------|------------|---------------|--------|
| COMIEN0 | 0xFFFF0704 | 0x00 | R/W |

COMIEN0 is the interrupt enable register.

Table 98. COMIEN0 MMR Bit Descriptions

| Bit | Name | Description |
|-----|-------|---|
| 7:4 | N/A | Reserved. |
| 3 | EDSSI | Modem status interrupt enable bit. Set by user to enable generation of an interrupt if any of COMSTA1[3:1] is set. Cleared by user. |
| 2 | ELSI | Rx status interrupt enable bit. Set by user to enable generation of an interrupt if any of COMSTA0[4:1] is set. Cleared by user. |
| 1 | ETBEI | Enable transmit buffer empty interrupt. Set by user to enable interrupt when buffer is empty during a transmission. Cleared by user. |
| 0 | ERBFI | Enable receive buffer full interrupt. Set by user to enable interrupt when buffer is full during a reception. Cleared by user. |

Table 140. I2CxDIV Registers

| Name Address | | Default Value | Access | |
|--------------|------------|---------------|--------|--|
| I2C0DIV | 0xFFFF0830 | 0x1F1F | R/W | |
| I2C1DIV | 0xFFFF0930 | 0x1F1F | R/W | |

I2CxDIV are the clock divider registers.

Table 141. I2CxIDx Registers

| Name | Address | Default Value | Access |
|---------|------------|---------------|--------|
| I2C0ID0 | 0xFFFF0838 | 0x00 | R/W |
| I2C0ID1 | 0xFFFF083C | 0x00 | R/W |
| I2C0ID2 | 0xFFFF0840 | 0x00 | R/W |
| I2C0ID3 | 0xFFFF0844 | 0x00 | R/W |
| I2C1ID0 | 0xFFFF0938 | 0x00 | R/W |
| I2C1ID1 | 0xFFFF093C | 0x00 | R/W |
| I2C1ID2 | 0xFFFF0940 | 0x00 | R/W |
| I2C1ID3 | 0xFFFF0944 | 0x00 | R/W |

I2CxID0, I2CxID1, I2CxID2, and I2CxID3 are slave address device ID registers of I2Cx.

Table 142. I2CxCCNT Registers

| Name | Address | Default Value | Access |
|----------|------------|---------------|--------|
| I2C0CCNT | 0xFFFF0848 | 0x01 | R/W |
| I2C1CCNT | 0xFFFF0948 | 0x01 | R/W |

I2CxCCNT are 8-bit start/stop generation counters. They hold off SDA low for start and stop conditions.

Table 143. I2CxFSTA Registers

| Name Address | | Default Value | Access |
|--------------|------------|---------------|--------|
| I2C0FSTA | 0xFFFF084C | 0x0000 | R/W |
| I2C1FSTA | 0xFFFF094C | 0x0000 | R/W |

I2CxFSTA are FIFO status registers.

| Table | 144. I2C0 | FSTA M | MR Bit Descriptions | |
|-------|-----------|--------|---------------------|--|
| | | | | |

| | Access | | |
|-------|--------|-------|--|
| Bit | Туре | Value | Description |
| 15:10 | | | Reserved. |
| 9 | R/W | | Master transmit FIFO flush. Set by the user to flush the master Tx FIFO. Cleared automatically when the master Tx FIFO is flushed. This bit also flushes the slave receive FIFO. |
| 8 | R/W | | Slave transmit FIFO flush. Set by the user to flush the slave Tx FIFO. Cleared automatically after the slave Tx FIFO is flushed. |
| 7:6 | R | | Master Rx FIFO status bits. |
| | | 00 | FIFO empty. |
| | | 01 | Byte written to FIFO. |
| | | 10 | One byte in FIFO. |
| | | 11 | FIFO full. |
| 5:4 | R | | Master Tx FIFO status bits. |
| | | 00 | FIFO empty. |
| | | 01 | Byte written to FIFO. |
| | | 10 | One byte in FIFO. |
| | | 11 | FIFO full. |
| 3:2 | R | | Slave Rx FIFO status bits. |
| | | 00 | FIFO empty. |
| | | 01 | Byte written to FIFO. |
| | | 10 | One byte in FIFO. |
| | | 11 | FIFO full. |
| 1:0 | R | | Slave Tx FIFO status bits. |
| | | 00 | FIFO empty. |
| | | 01 | Byte written to FIFO. |
| | | 10 | One byte in FIFO. |
| | | 11 | FIFO full. |

Data Sheet

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Dimensions shown in millimeters