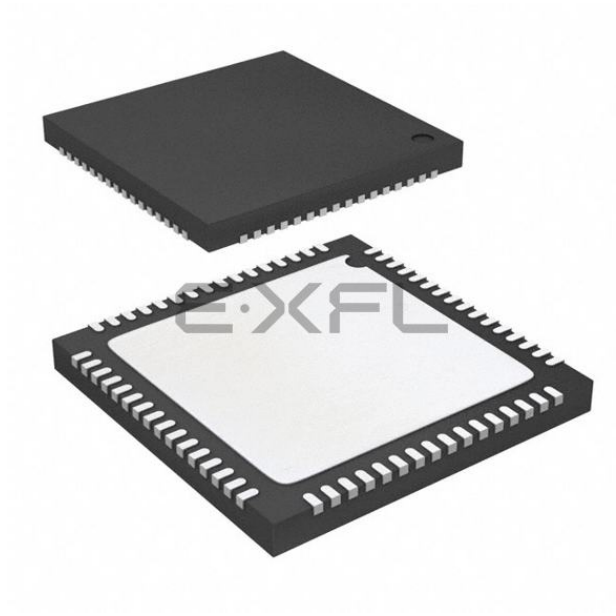

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Details	
Product Status	Active
Core Processor	ARM7®
Core Size	16/32-Bit
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Peripherals	PLA, PWM, PSM, Temp Sensor, WDT
Number of I/O	30
Program Memory Size	62KB (31K x16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 32
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad, CSP
Supplier Device Package	64-LFCSP-VQ (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/aduc7025bcpz62

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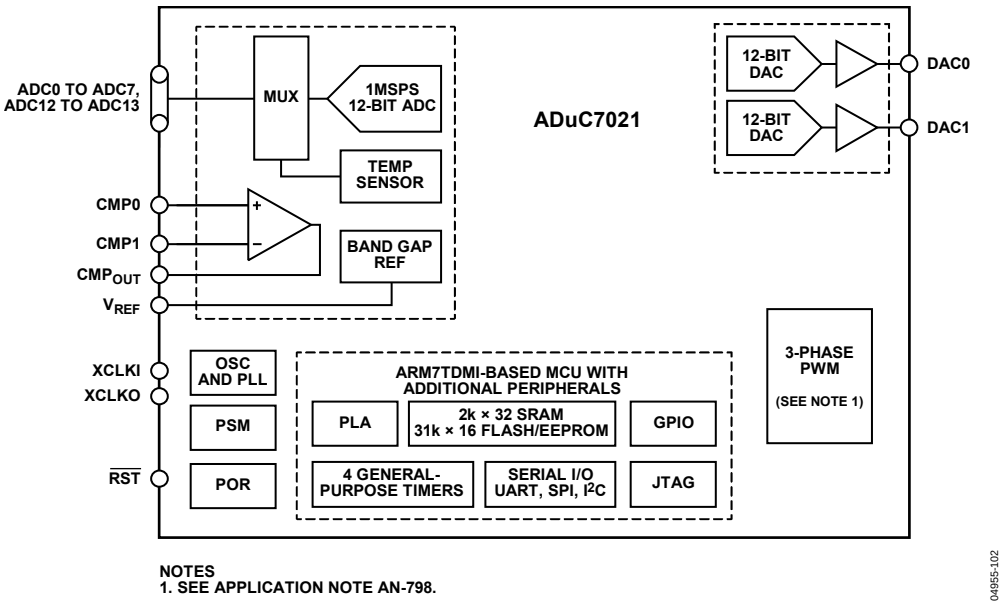
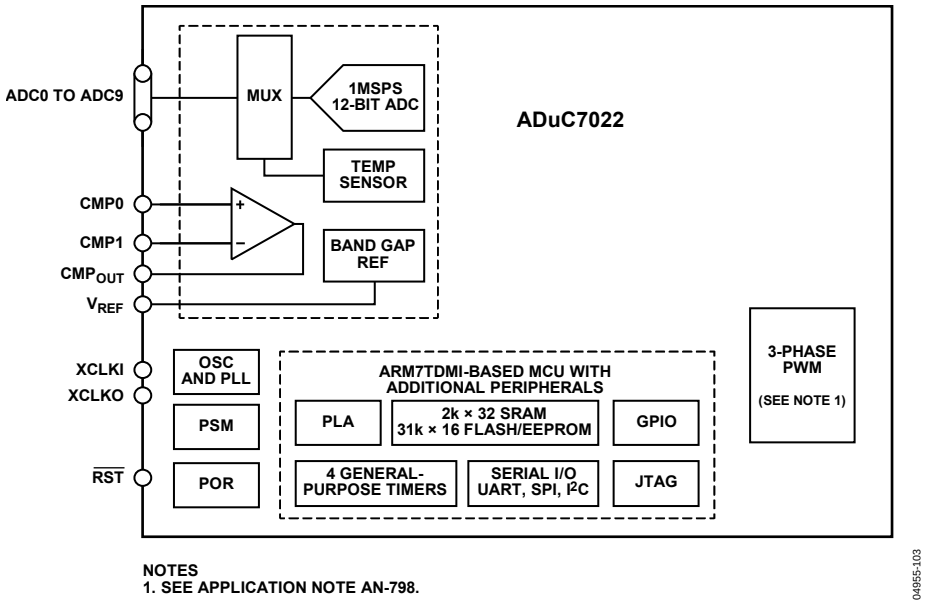


Figure 3.



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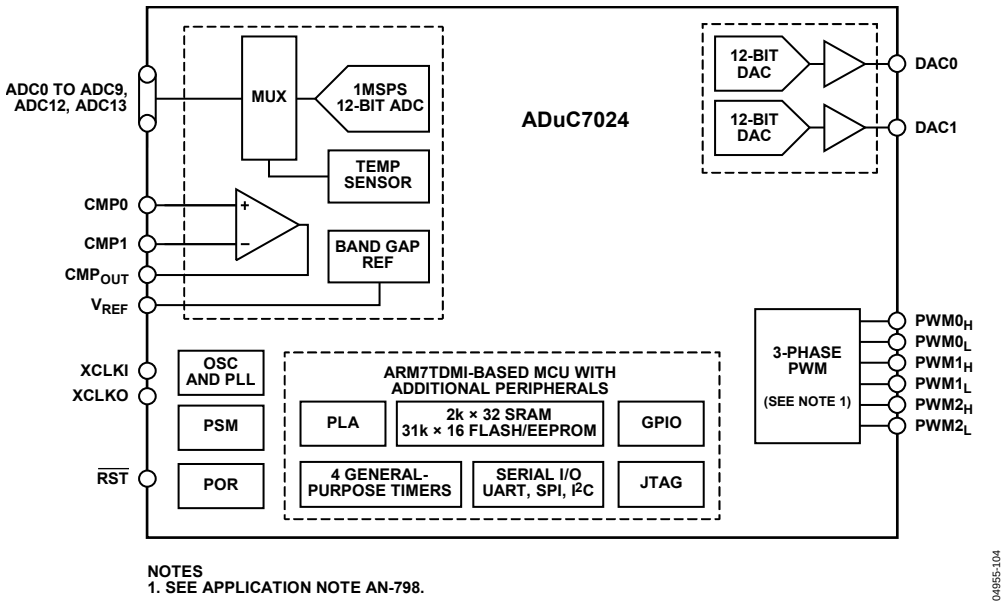

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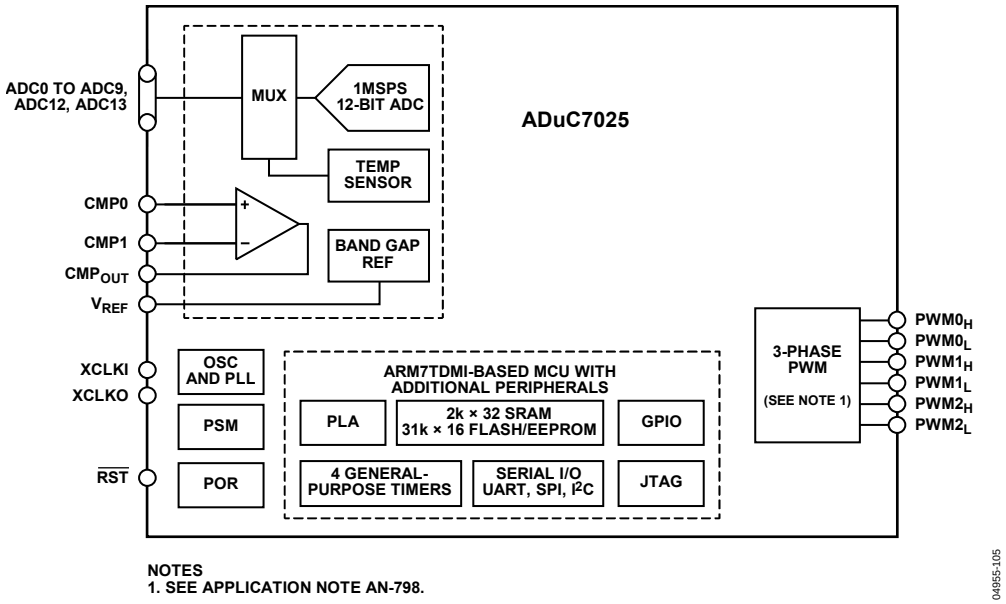

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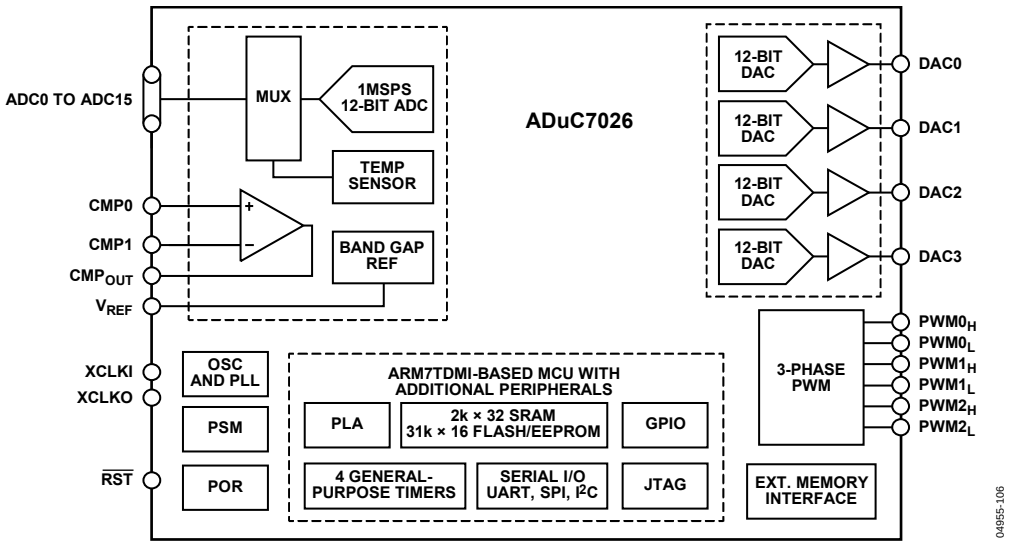


Figure 7.

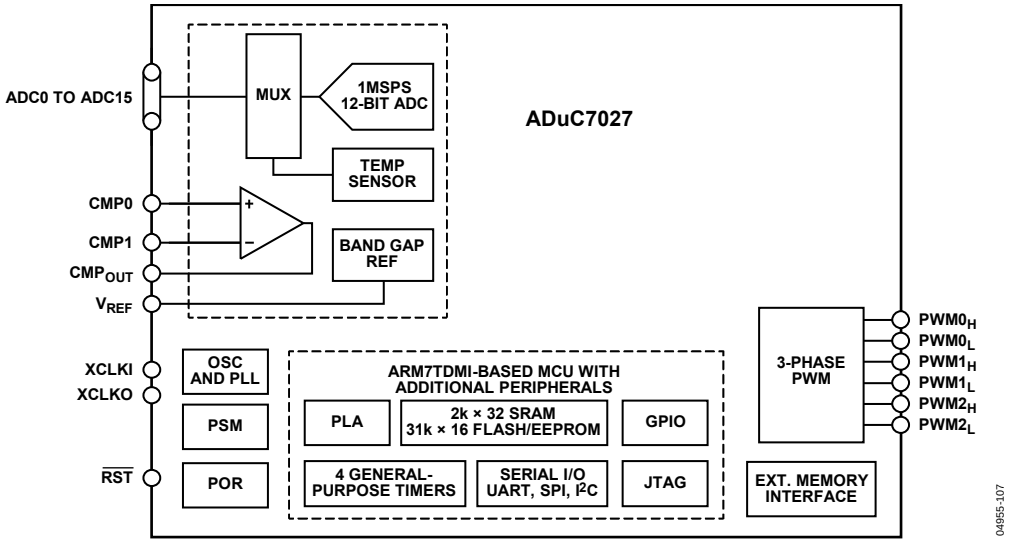


Figure 8.

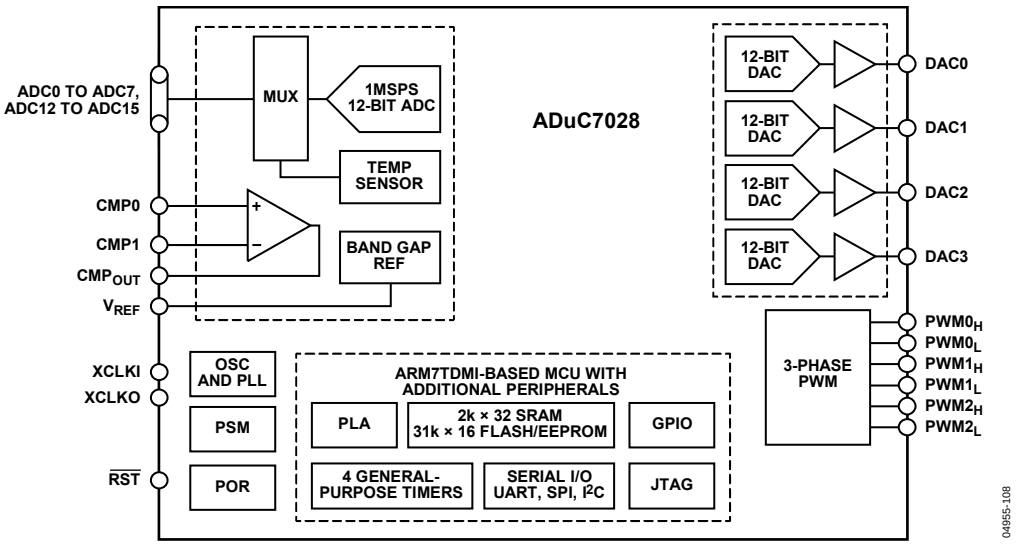


Figure 9.

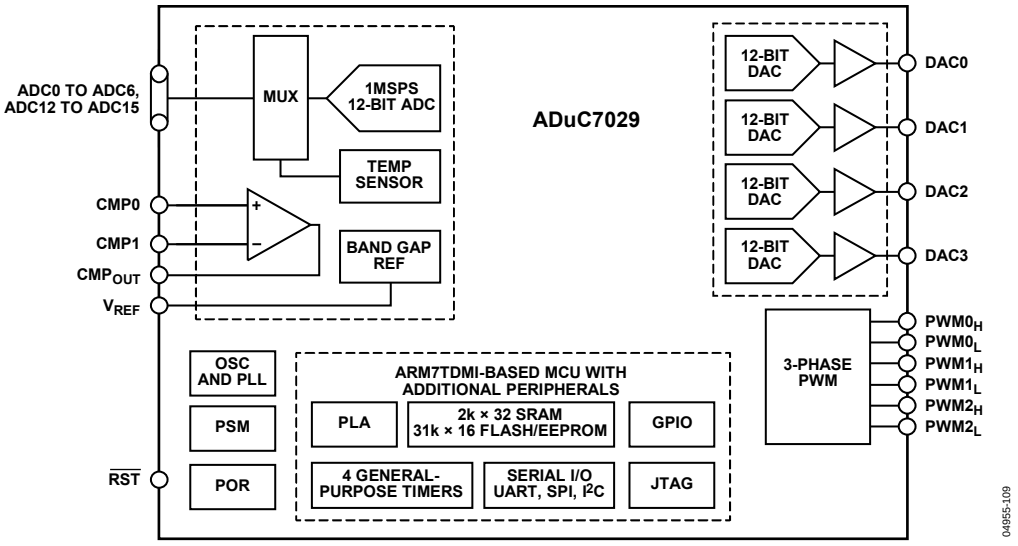


Figure 10.

DETAILED BLOCK DIAGRAM

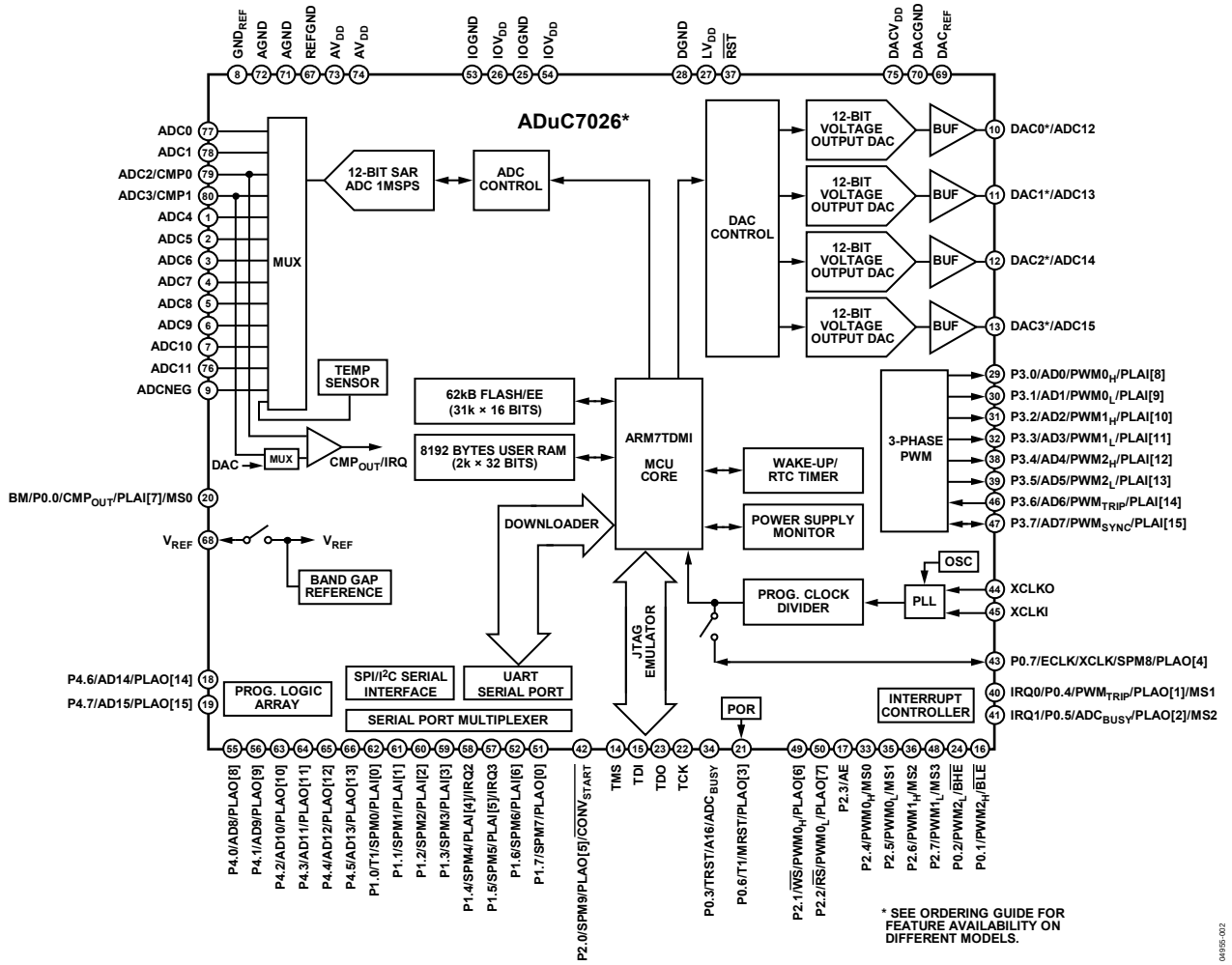


Figure 11.

TIMING SPECIFICATIONS

Table 2. External Memory Write Cycle

Parameter	Min	Typ	Max	Unit
CLK[1]		UCLK		
$t_{MS\_AFTER\_CLKH}$	0		4	ns
$t_{ADDR\_AFTER\_CLKH}$	4		8	ns
$t_{AE\_H\_AFTER\_MS}$		½ CLK		
t_{AE}		(XMxPAR[14:12] + 1) × CLK		
$t_{HOLD\_ADDR\_AFTER\_AE\_L}$		½ CLK + (!XMxPAR[10]) × CLK		
$t_{HOLD\_ADDR\_BEFORE\_WR\_L}$		(!XMxPAR[8]) × CLK		
$t_{WR\_L\_AFTER\_AE\_L}$		½ CLK + (!XMxPAR[10] + !XMxPAR[8]) × CLK		
$t_{DATA\_AFTER\_WR\_L}$	8		12	ns
t_{WR}		(XMxPAR[7:4] + 1) × CLK		
$t_{WR\_H\_AFTER\_CLKH}$	0		4	ns
$t_{HOLD\_DATA\_AFTER\_WR\_H}$		(!XMxPAR[8]) × CLK		
$t_{BEN\_AFTER\_AE\_L}$		½ CLK		
$t_{RELEASE\_MS\_AFTER\_WR\_H}$		(!XMxPAR[8] + 1) × CLK		

[1] See Table 78.

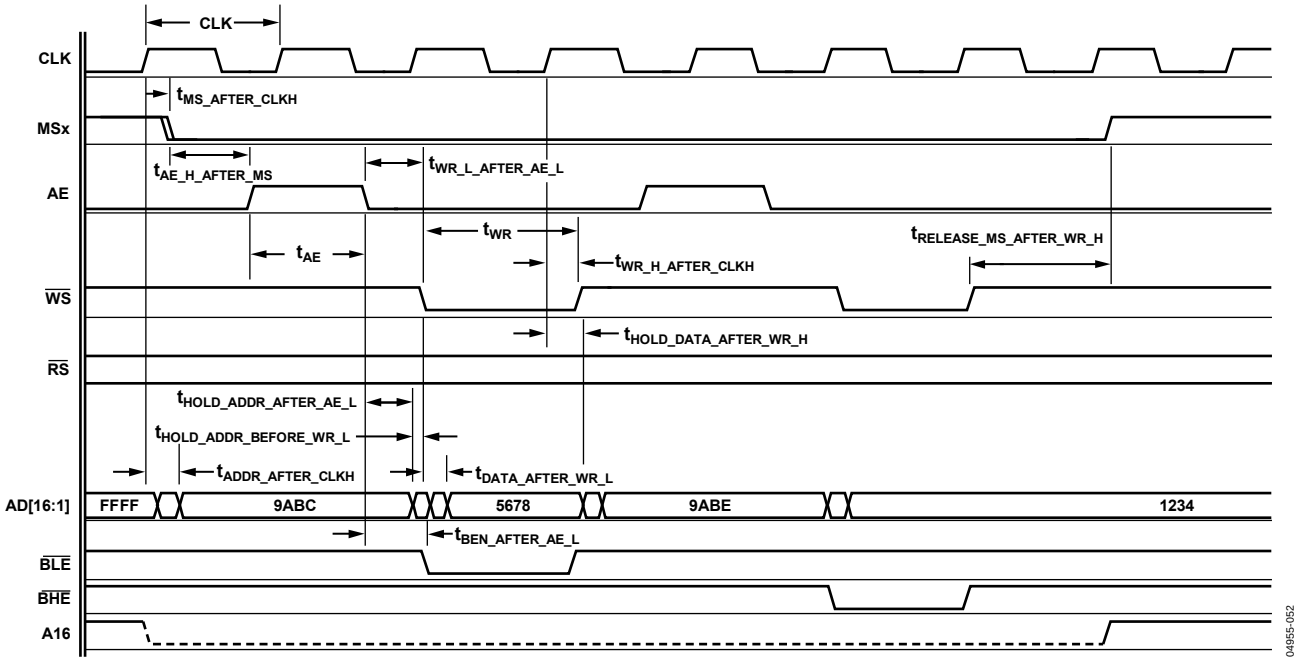


Figure 12. External Memory Write Cycle (See Table 78)

Table 7. SPI Master Mode Timing (Phase Mode = 0)

Parameter	Description	Min	Typ	Max	Unit
t_{SL}	SCLK low pulse width[1]		(SPIDIV + 1) × t_{HCLK}		ns
t_{SH}	SCLK high pulse width[1]		(SPIDIV + 1) × t_{HCLK}		ns
t_{DAV}	Data output valid after SCLK edge			25	ns
t_{DOSU}	Data output setup before SCLK edge			75	ns
t_{DSU}	Data input setup time before SCLK edge[2]	1 × t_{UCLK}			ns
t_{DHD}	Data input hold time after SCLK edge[2]	2 × t_{UCLK}			ns
t_{DF}	Data output fall time		5	12.5	ns
t_{DR}	Data output rise time		5	12.5	ns
t_{SR}	SCLK rise time		5	12.5	ns
t_{SF}	SCLK fall time		5	12.5	ns

[1] t_{HCLK} depends on the clock divider or CD bits in the POWCONMMR. $t_{HCLK} = t_{UCLK}/2^{CD}$; see Figure 67.
[2] t_{UCLK} = 23.9 ns. It corresponds to the 41.78 MHz internal clock from the PLL before the clock divider; see Figure 67.

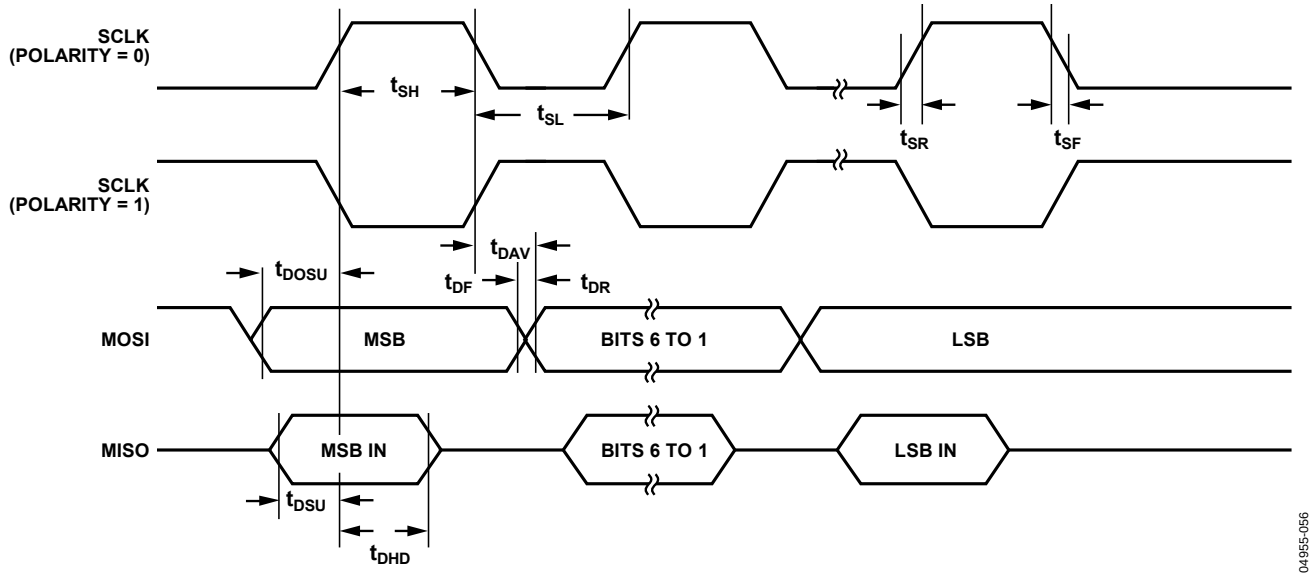


Figure 16. SPI Master Mode Timing (Phase Mode = 0)

Table 9. SPI Slave Mode Timing (Phase Mode = 0)

Parameter	Description	Min	Typ	Max	Unit
$t_{\overline{CS}}$	$\overline{CS}$ to SCLK edge[1]	$(2 \times t_{HCLK}) + (2 \times t_{UCLK})$			ns
t_{SL}	SCLK low pulse width[2]		$(SPIDIV + 1) \times t_{HCLK}$		ns
t_{SH}	SCLK high pulse width[2]		$(SPIDIV + 1) \times t_{HCLK}$		ns
t_{DAV}	Data output valid after SCLK edge			25	ns
t_{DSU}	Data input setup time before SCLK edge[1]	$1 \times t_{UCLK}$			ns
t_{DHD}	Data input hold time after SCLK edge[1]	$2 \times t_{UCLK}$			ns
t_{DF}	Data output fall time		5	12.5	ns
t_{DR}	Data output rise time		5	12.5	ns
t_{SR}	SCLK rise time		5	12.5	ns
t_{SF}	SCLK fall time		5	12.5	ns
t_{DOCS}	Data output valid after $\overline{CS}$ edge			25	ns
t_{SFS}	$\overline{CS}$ high after SCLK edge	0			ns

[1] t_{UCLK} = 23.9 ns. It corresponds to the 41.78 MHz internal clock from the PLL before the clock divider; see Figure 67.
[2] t_{HCLK} depends on the clock divider or CD bits in the POWCONMMR. $t_{HCLK} = t_{UCLK}/2^{CD}$; see Figure 67.

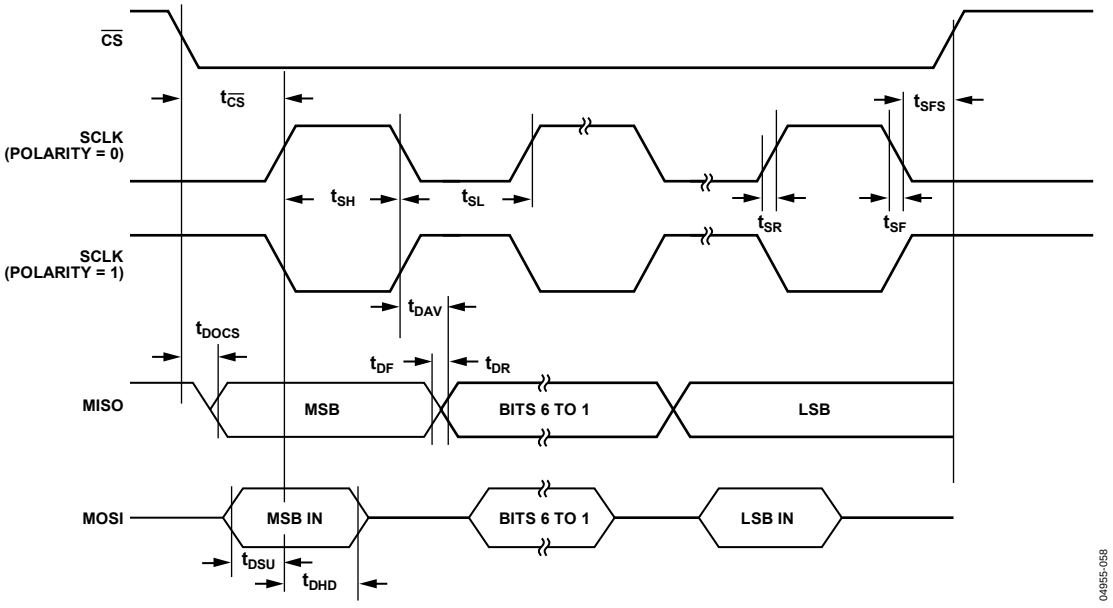


Figure 18. SPI Slave Mode Timing (Phase Mode = 0)

Table 12. Pin Function Descriptions (ADuC7024/ADuC7025 64-Lead LFCSP_VQ and 64-Lead LQFP)

Pin No.	Mnemonic	Description
1	ADC4	Single-Ended or Differential Analog Input 4.
2	ADC5	Single-Ended or Differential Analog Input 5.
3	ADC6	Single-Ended or Differential Analog Input 6.
4	ADC7	Single-Ended or Differential Analog Input 7.
5	ADC8	Single-Ended or Differential Analog Input 8.
6	ADC9	Single-Ended or Differential Analog Input 9.
7	GND_{REF}	Ground Voltage Reference for the ADC. For optimal performance, the analog power supply should be separated from IOGND and DGND.
8	ADCNEG	Bias Point or Negative Analog Input of the ADC in Pseudo Differential Mode. Must be connected to the ground of the signal to convert. This bias point must be between 0 V and 1 V.
9	DAC0/ADC12	DAC0 Voltage Output/Single-Ended or Differential Analog Input 12. DAC outputs are not present on the ADuC7025.
10	DAC1/ADC13	DAC1 Voltage Output/Single-Ended or Differential Analog Input 13. DAC outputs are not present on the ADuC7025.
11	TMS	JTAG Test Port Input, Test Mode Select. Debug and download access.
12	TDI	JTAG Test Port Input, Test Data In. Debug and download access
13	P4.6/PLAO[14]	General-Purpose Input and Output Port 4.6/Programmable Logic Array Output Element 14.
14	P4.7/PLAO[15]	General-Purpose Input and Output Port 4.7/Programmable Logic Array Output Element 15.
15	BM/P0.0/CMP_{OUT}/PLAI[7]	Multifunction I/O Pin. Boot mode. The ADuC7024/ADuC7025 enter download mode if BM is low at reset and execute code if BM is pulled high at reset through a 1 kΩ resistor/General-Purpose Input and Output Port 0.0/Voltage Comparator Output/Programmable Logic Array Input Element 7.
16	P0.6/T1/MRST/PLAO[3]	Multifunction Pin, Driven Low After Reset. General-Purpose Output Port 0.6/Timer1 Input/Power-On Reset Output/Programmable Logic Array Output Element 3.
17	TCK	JTAG Test Port Input, Test Clock. Debug and download access.
18	TDO	JTAG Test Port Output, Test Data Out. Debug and download access.
19	IOGND	Ground for GPIO (see Table 78). Typically connected to DGND.
20	IOV_{DD}	3.3 V Supply for GPIO (see Table 78) and Input of the On-Chip Voltage Regulator.
21	LV_{DD}	2.6 V Output of the On-Chip Voltage Regulator. This output must be connected to a 0.47 µF capacitor to DGND only.
22	DGND	Ground for Core Logic.
23	P3.0/$PWM0_H$/PLAI[8]	General-Purpose Input and Output Port 3.0/PWM Phase 0 High-Side Output/Programmable Logic Array Input Element 8.
24	P3.1/$PWM0_L$/PLAI[9]	General-Purpose Input and Output Port 3.1/PWM Phase 0 Low-Side Output/Programmable Logic Array Input Element 9.
25	P3.2/$PWM1_H$/PLAI[10]	General-Purpose Input and Output Port 3.2/PWM Phase 1 High-Side Output/Programmable Logic Array Input Element 10.
26	P3.3/$PWM1_L$/PLAI[11]	General-Purpose Input and Output Port 3.3/PWM Phase 1 Low-Side Output/Programmable Logic Array Input Element 11.
27	P0.3/TRST/ADC_{BUSY}	General-Purpose Input and Output Port 0.3/JTAG Test Port Input, Test Reset/ADC_{BUSY} Signal Output.
28	$\overline{RST}$	Reset Input, Active Low.
29	P3.4/$PWM2_H$/PLAI[12]	General-Purpose Input and Output Port 3.4/PWM Phase 2 High-Side Output/Programmable Logic Array Input 12.
30	P3.5/$PWM2_L$/PLAI[13]	General-Purpose Input and Output Port 3.5/PWM Phase 2 Low-Side Output/Programmable Logic Array Input Element 13.
31	IRQ0/P0.4/PWM_{TRIP}/PLAO[1]	Multifunction I/O Pin. External Interrupt Request 0, Active High/General-Purpose Input and Output Port 0.4/PWM Trip External Input/Programmable Logic Array Output Element 1.
32	IRQ1/P0.5/ADC_{BUSY}/PLAO[2]	Multifunction I/O Pin. External Interrupt Request 1, Active High/General-Purpose Input and Output Port 0.5/ADC_{BUSY} Signal Output/Programmable Logic Array Output Element 2.
33	P2.0/SPM9/PLAO[5]/$\overline{CONV_{START}}$	Serial Port Multiplexed. General-Purpose Input and Output Port 2.0/UART/Programmable Logic Array Output Element 5/Start Conversion Input Signal for ADC.
34	P0.7/ECLK/XCLK/SPM8/PLAO[4]	Serial Port Multiplexed. General-Purpose Input and Output Port 0.7/Output for External Clock Signal/Input to the Internal Clock Generator Circuits/UART/Programmable Logic Array Output Element 4.
35	XCLKO	Output from the Crystal Oscillator Inverter.
36	XCLKI	Input to the Crystal Oscillator Inverter and Input to the Internal Clock Generator Circuits.

Pin No.	Mnemonic	Description
37	P3.6/PWM_{TRIP}/PLAI[14]	General-Purpose Input and Output Port 3.6/PWM Safety Cutoff/Programmable Logic Array Input Element 14.
38	P3.7/PWM_{SYNC}/PLAI[15]	General-Purpose Input and Output Port 3.7/PWM Synchronization Input and Output/ Programmable Logic Array Input Element 15.
39	P1.7/SPM7/PLAO[0]	Serial Port Multiplexed. General-Purpose Input and Output Port 1.7/UART, SPI/Programmable Logic Array Output Element 0.
40	P1.6/SPM6/PLAI[6]	Serial Port Multiplexed. General-Purpose Input and Output Port 1.6/UART, SPI/Programmable Logic Array Input Element 6.
41	IOGND	Ground for GPIO (see Table 78). Typically connected to DGND.
42	IOV_{DD}	3.3 V Supply for GPIO (see Table 78) and Input of the On-Chip Voltage Regulator.
43	P4.0/PLAO[8]	General-Purpose Input and Output Port 4.0/Programmable Logic Array Output Element 8.
44	P4.1/PLAO[9]	General-Purpose Input and Output Port 4.1/Programmable Logic Array Output Element 9.
45	P1.5/SPM5/PLAI[5]/IRQ3	Serial Port Multiplexed. General-Purpose Input and Output Port 1.5/UART, SPI/Programmable Logic Array Input Element 5/External Interrupt Request 3, Active High.
46	P1.4/SPM4/PLAI[4]/IRQ2	Serial Port Multiplexed. General-Purpose Input and Output Port 1.4/UART, SPI/Programmable Logic Array Input Element 4/External Interrupt Request 2, Active High.
47	P1.3/SPM3/PLAI[3]	Serial Port Multiplexed. General-Purpose Input and Output Port 1.3/UART, I2C1/Programmable Logic Array Input Element 3.
48	P1.2/SPM2/PLAI[2]	Serial Port Multiplexed. General-Purpose Input and Output Port 1.2/UART, I2C1/Programmable Logic Array Input Element 2.
49	P1.1/SPM1/PLAI[1]	Serial Port Multiplexed. General-Purpose Input and Output Port 1.1/UART, I2C0/Programmable Logic Array Input Element 1.
50	P1.0/T1/SPM0/PLAI[0]	Serial Port Multiplexed. General-Purpose Input and Output Port 1.0/Timer1 Input/UART, I2C0/ Programmable Logic Array Input Element 0.
51	P4.2/PLAO[10]	General-Purpose Input and Output Port 4.2/Programmable Logic Array Output Element 10.
52	P4.3/PLAO[11]	General-Purpose Input and Output Port 4.3/Programmable Logic Array Output Element 11.
53	P4.4/PLAO[12]	General-Purpose Input and Output Port 4.4/Programmable Logic Array Output Element 12.
54	P4.5/PLAO[13]	General-Purpose Input and Output Port 4.5/Programmable Logic Array Output Element 13.
55	V_{REF}	2.5 V Internal Voltage Reference. Must be connected to a 0.47 µF capacitor when using the internal reference.
56	DAC_{REF}	External Voltage Reference for the DACs. Range: DACGND to $DACV_{DD}$.
57	DACGND	Ground for the DAC. Typically connected to AGND.
58	AGND	Analog Ground. Ground reference point for the analog circuitry.
59	AV_{DD}	3.3 V Analog Power.
60	$DACV_{DD}$	3.3 V Power Supply for the DACs. Must be connected to AV_{DD}.
61	ADC0	Single-Ended or Differential Analog Input 0.
62	ADC1	Single-Ended or Differential Analog Input 1.
63	ADC2/CMP0	Single-Ended or Differential Analog Input 2/Comparator Positive Input.
64	ADC3/CMP1	Single-Ended or Differential Analog Input 3/Comparator Negative Input.
0	EP	Exposed Pad. The pin configuration for the ADuC7024/ADuC7025 LFCSP_VQ has an exposed pad that must be soldered for mechanical purposes and left unconnected.

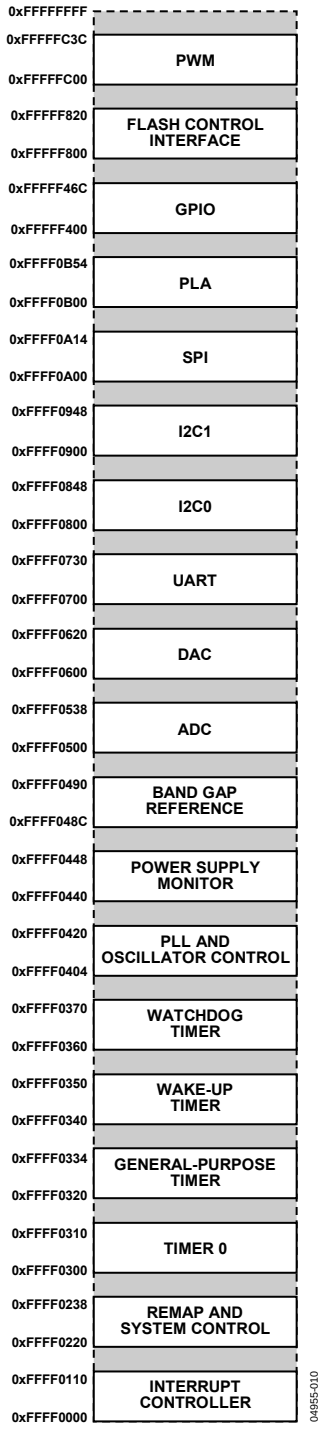


Figure 47. Memory Mapped Registers

Table 16. Complete MMR List

Address	Name	Byte	Access Type	Default Value	Page
IRQ Address Base = 0xFFFF0000					
0x0000	IRQSTA	4	R	0x00000000	83
0x0004	IRQSIG[1]	4	R	0x00XXX000	83
0x0008	IRQEN	4	R/W	0x00000000	83
0x000C	IRQCLR	4	W	0x00000000	83
0x0010	SWICFG	4	W	0x00000000	84
0x0100	FIQSTA	4	R	0x00000000	84
0x0104	FIQSIG[1]	4	R	0x00XXX000	84
0x0108	FIQEN	4	R/W	0x00000000	84
0x010C	FIQCLR	4	W	0x00000000	84

[1] Depends on the level on the external interrupt pins (P0.4, P0.5, P1.4, and P1.5).

System Control Address Base = 0xFFFF0200					
0x0220	REMAP	1	R/W	0xXX[1]	55
0x0230	RSTSTA	1	R/W	0x01	55
0x0234	RSTCLR	1	W	0x00	55

[1] Depends on the model.

Timer Address Base = 0xFFFF0300					
0x0300	T0LD	2	R/W	0x0000	85
0x0304	T0VAL	2	R	0xFFFF	85
0x0308	T0CON	2	R/W	0x0000	85
0x030C	T0CLRI	1	W	0xFF	85
0x0320	T1LD	4	R/W	0x00000000	86
0x0324	T1VAL	4	R	0xFFFFFFFF	86
0x0328	T1CON	2	R/W	0x0000	86
0x032C	T1CLRI	1	W	0xFF	87
0x0330	T1CAP	4	R/W	0x00000000	87
0x0340	T2LD	4	R/W	0x00000000	87
0x0344	T2VAL	4	R	0xFFFFFFFF	87
0x0348	T2CON	2	R/W	0x0000	87
0x034C	T2CLRI	1	W	0xFF	88
0x0360	T3LD	2	R/W	0x0000	88
0x0364	T3VAL	2	R	0xFFFF	88
0x0368	T3CON	2	R/W	0x0000	88
0x036C	T3CLRI	1	W	0x00	89

PLL Base Address = 0xFFFF0400					
0x0404	POWKEY1	2	W	0x0000	60
0x0408	POWCON	2	R/W	0x0003	60
0x040C	POWKEY2	2	W	0x0000	60
0x0410	PLLKEY1	2	W	0x0000	60
0x0414	PLLCON	1	R/W	0x21	60
0x0418	PLLKEY2	2	W	0x0000	60

PSM Address Base = 0xFFFF0440					
0x0440	PSMCON	2	R/W	0x0008	57
0x0444	CMPCON	2	R/W	0x0000	58

Table 22. ADCCN MMR Bit Designation

Bit	Value	Description
7:5		Reserved.
4:0		Negative channel selection bits.
	00000	ADC0.
	00001	ADC1.
	00010	ADC2.
	00011	ADC3.
	00100	ADC4.
	00101	ADC5.
	00110	ADC6.
	00111	ADC7.
	01000	ADC8.
	01001	ADC9.
	01010	ADC10.
	01011	ADC11.
	01100	DAC0/ADC12.
	01101	DAC1/ADC13.
	01110	DAC2/ADC14.
	01111	DAC3/ADC15.
	10000	Internal reference (self-diagnostic feature).
	Others	Reserved.

Table 23. ADCSTA Register

Name	Address	Default Value	Access
ADCSTA	0xFFFF050C	0x00	R

ADCSTA is an ADC status register that indicates when an ADC conversion result is ready. The ADCSTA register contains only one bit, ADCReady (Bit 0), representing the status of the ADC. This bit is set at the end of an ADC conversion, generating an ADC interrupt. It is cleared automatically by reading the ADCDAT MMR. When the ADC is performing a conversion, the status of the ADC can be read externally via the ADC_{BUSY} pin. This pin is high during a conversion. When the conversion is finished, ADC_{BUSY} goes back low. This information can be available on P0.5 (see the General-Purpose Input/Output section) if enabled in the ADCCON register.

Table 24. ADCDAT Register

Name	Address	Default Value	Access
ADCDAT	0xFFFF0510	0x00000000	R

ADCDAT is an ADC data result register. It holds the 12-bit ADC result as shown in Figure 51.

Table 25. ADCRST Register

Name	Address	Default Value	Access
ADCRST	0xFFFF0514	0x00	R/W

ADCRST resets the digital interface of the ADC. Writing any value to this register resets all the ADC registers to their default values.

Table 26. ADCGN Register

Name	Address	Default Value	Access
ADCGN	0xFFFF0530	0x0200	R/W

ADCGN is a 10-bit gain calibration register.

Table 27. ADCOF Register

Name	Address	Default Value	Access
ADCOF	0xFFFF0534	0x0200	R/W

ADCOF is a 10-bit offset calibration register.

CONVERTER OPERATION

The ADC incorporates a successive approximation (SAR) architecture involving a charge-sampled input stage. This architecture can operate in three modes: differential, pseudo differential, and single-ended.

Differential Mode

The ADuC7019/20/21/22/24/25/26/27/28/29 each contain a successive approximation ADC based on two capacitive DACs. Figure 54 and Figure 55 show simplified schematics of the ADC in acquisition and conversion phase, respectively. The ADC comprises control logic, a SAR, and two capacitive DACs. In Figure 54 (the acquisition phase), SW3 is closed and SW1 and SW2 are in Position A. The comparator is held in a balanced condition, and the sampling capacitor arrays acquire the differential signal on the input.

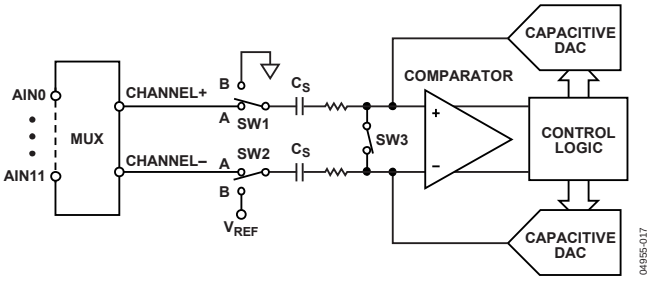


Figure 54. ADC Acquisition Phase

When the ADC starts a conversion, as shown in Figure 55, SW3 opens, and then SW1 and SW2 move to Position B. This causes the comparator to become unbalanced. Both inputs are disconnected once the conversion begins. The control logic and the charge redistribution DACs are used to add and subtract fixed amounts of charge from the sampling capacitor arrays to bring the comparator back into a balanced condition. When the comparator is rebalanced, the conversion is complete. The control logic generates the ADC output code. The output impedances of the sources driving the V_{IN+} and V_{IN-} input voltage pins must be matched; otherwise, the two inputs have different settling times, resulting in errors.

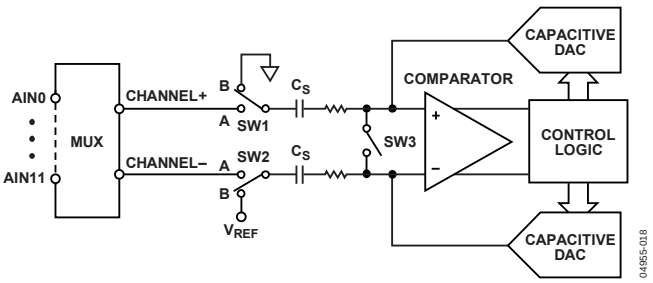


Figure 55. ADC Conversion Phase

NONVOLATILE FLASH/EE MEMORY

The ADuC7019/20/21/22/24/25/26/27/28/29 incorporate Flash/EE memory technology on-chip to provide the user with nonvolatile, in-circuit reprogrammable memory space.

Like EEPROM, flash memory can be programmed in-system at a byte level, although it must first be erased. The erase is performed in page blocks. As a result, flash memory is often and more correctly referred to as Flash/EE memory.

Overall, Flash/EE memory represents a step closer to the ideal memory device that includes nonvolatility, in-circuit programmability, high density, and low cost. Incorporated in the ADuC7019/20/21/22/24/25/26/27/28/29, Flash/EE memory technology allows the user to update program code space in-circuit, without the need to replace one-time programmable (OTP) devices at remote operating nodes.

Each part contains a 64 kB array of Flash/EE memory. The lower 62 kB is available to the user and the upper 2 kB contain permanently embedded firmware, allowing in-circuit serial download. These 2 kB of embedded firmware also contain a power-on configuration routine that downloads factory-calibrated coefficients to the various calibrated peripherals (such as ADC, temperature sensor, and band gap references). This 2 kB embedded firmware is hidden from user code.

Flash/EE Memory Reliability

The Flash/EE memory arrays on the parts are fully qualified for two key Flash/EE memory characteristics: Flash/EE memory cycling endurance and Flash/EE memory data retention.

Endurance quantifies the ability of the Flash/EE memory to be cycled through many program, read, and erase cycles. A single endurance cycle is composed of four independent, sequential events, defined as

1. Initial page erase sequence
2. Read/verify sequence (single Flash/EE)
3. Byte program sequence memory
4. Second read/verify sequence (endurance cycle)

In reliability qualification, every half word (16-bit wide) location of the three pages (top, middle, and bottom) in the Flash/EE memory is cycled 10,000 times from 0x0000 to 0xFFFF. As indicated in Table 1, the Flash/EE memory endurance qualification is carried out in accordance with JEDEC Retention Lifetime Specification A117 over the industrial temperature range of −40° to +125°C. The results allow the specification of a minimum endurance figure over a supply temperature of 10,000 cycles.

Retention quantifies the ability of the Flash/EE memory to retain its programmed data over time. Again, the parts are qualified in accordance with the formal JEDEC Retention Lifetime Specification (A117) at a specific junction temperature (T_J = 85°C). As part of this qualification procedure, the Flash/EE memory is cycled to its specified endurance limit, described in Table 1, before data retention is characterized. This means that the Flash/EE memory is guaranteed to retain its data for its fully specified retention lifetime every time the Flash/EE memory is reprogrammed. In addition, note that retention lifetime, based on an activation energy of 0.6 eV, derates with T_J as shown in Figure 61.

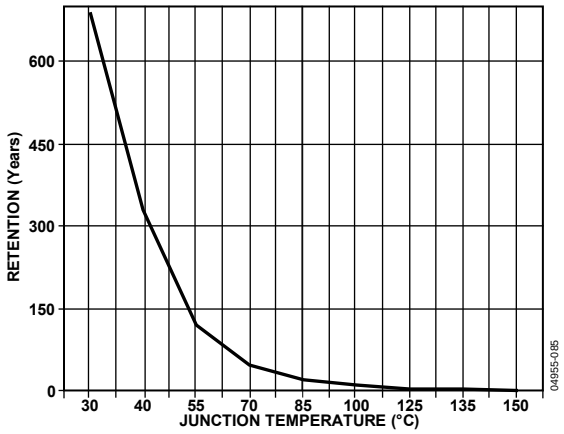


Figure 61. Flash/EE Memory Data Retention

PROGRAMMING

The 62 kB of Flash/EE memory can be programmed in-circuit, using the serial download mode or the provided JTAG mode.

Serial Downloading (In-Circuit Programming)

The ADuC7019/20/21/22/24/25/26/27/28/29 facilitate code download via the standard UART serial port or via the I²C port. The parts enter serial download mode after a reset or power cycle if the BM pin is pulled low through an external 1 kΩ resistor. After a part is in serial download mode, the user can download code to the full 62 kB of Flash/EE memory while the device is in-circuit in its target application hardware. An executable PC serial download is provided as part of the development system for serial downloading via the UART. The AN-806 Application Note describes the protocol for serial downloading via the I²C.

JTAG Access

The JTAG protocol uses the on-chip JTAG interface to facilitate code download and debug.

Table 108. COMSTA1 Register

Name	Address	Default Value	Access
COMSTA1	0xFFFF0718	0x00	R

COMSTA1 is a modem status register.

Table 109. COMSTA1 MMR Bit Descriptions

Bit	Name	Description
7	DCD	Data carrier detect.
6	RI	Ring indicator.
5	DSR	Data set ready.
4	CTS	Clear to send.
3	DDCD	Delta DCD. Set automatically if DCD changed state since last COMSTA1 read. Cleared automatically by reading COMSTA1.
2	TERI	Trailing edge RI. Set if RI changed from 0 to 1 since COMSTA1 was last read. Cleared automatically by reading COMSTA1.
1	DDSR	Delta DSR. Set automatically if DSR changed state since COMSTA1 was last read. Cleared automatically by reading COMSTA1.
0	DCTS	Delta CTS. Set automatically if CTS changed state since COMSTA1 was last read. Cleared automatically by reading COMSTA1.

Table 110. COMSCR Register

Name	Address	Default Value	Access
COMSCR	0xFFFF071C	0x00	R/W

COMSCR is an 8-bit scratch register used for temporary storage. It is also used in network addressable UART mode.

Table 111. COMDIV2 Register

Name	Address	Default Value	Access
COMDIV2	0xFFFF072C	0x0000	R/W

COMDIV2 is a 16-bit fractional baud divide register.

Table 112. COMDIV2 MMR Bit Descriptions

Bit	Name	Description
15	FBEN	Fractional baud rate generator enable bit. Set by user to enable the fractional baud rate generator. Cleared by user to generate baud rate using the standard 450 UART baud rate generator.
14:13		Reserved.
12:11	FBM[1:0]	M if FBM = 0, M = 4 (see the Fractional Divider section).
10:0	FBN[10:0]	N (see the Fractional Divider section).

Network Addressable UART Mode

This mode connects the MicroConverter to a 256-node serial network, either as a hardware single master or via software in a multimaster network. Bit 7 (ENAM) of the COMIEN1 register must be set to enable UART in network addressable mode (see Table 114). Note that there is no parity check in this mode.

Network Addressable UART Register Definitions

Four additional registers, COMIEN0, COMIEN1, COMIID1, and COMADR are used in network addressable UART mode only.

In network address mode, the least significant bit of the COMIEN1 register is the transmitted network address control bit. If set to 1, the device is transmitting an address. If cleared to 0, the device is transmitting data. For example, the following master-based code transmits the slave's address followed by the data:

```
  COMIEN1  = 0xE7;       //Setting ENAM,
E9BT, E9BR, ETD, NABP
  COMTX = 0xA0;  // Slave address is 0xA0
  while(!(0x020==(COMSTA0 & 0x020))){} //
wait for adr tx to finish.
  COMIEN1  = 0xE6;       //  Clear NAB bit
to indicate Data is coming
   COMTX = 0x55; // Tx data to slave: 0x55
```

Table 113. COMIEN1 Register

Name	Address	Default Value	Access
COMIEN1	0xFFFF0720	0x04	R/W

COMIEN1 is an 8-bit network enable register.

Table 114. COMIEN1 MMR Bit Descriptions

Bit	Name	Description
7	ENAM	Network address mode enable bit. Set by user to enable network address mode. Cleared by user to disable network address mode.
6	E9BT	9-bit transmit enable bit. Set by user to enable 9-bit transmit. ENAM must be set. Cleared by user to disable 9-bit transmit.
5	E9BR	9-bit receive enable bit. Set by user to enable 9-bit receive. ENAM must be set. Cleared by user to disable 9-bit receive.
4	ENI	Network interrupt enable bit.
3	E9BD	Word length. Set for 9-bit data. E9BT has to be cleared. Cleared for 8-bit data.
2	ETD	Transmitter pin driver enable bit. Set by user to enable SOUT pin as an output in slave mode or multimaster mode. Cleared by user; SOUT is three-state.
1	NABP	Network address bit. Interrupt polarity bit.
0	NAB	Network address bit (if NABP = 1). Set by user to transmit the slave address. Cleared by user to transmit data.

Table 115. COMIID1 Register

Name	Address	Default Value	Access
COMIID1	0xFFFF0724	0x01	R

COMIID1 is an 8-bit network interrupt register. Bit 7 to Bit 4 are reserved (see Table 116).

PROGRAMMABLE LOGIC ARRAY (PLA)

Every ADuC7019/20/21/22/24/25/26/27/28/29 integrates a fully programmable logic array (PLA) that consists of two independent but interconnected PLA blocks. Each block consists of eight PLA elements, giving each part a total of 16 PLA elements.

Each PLA element contains a two-input lookup table that can be configured to generate any logic output function based on two inputs and a flip-flop. This is represented in Figure 76.

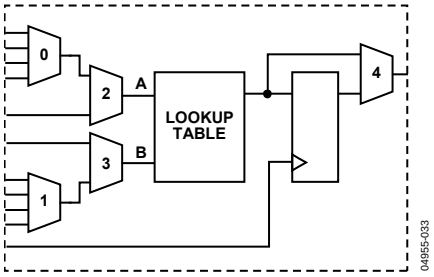


Figure 76. PLA Element

In total, 30 GPIO pins are available on each ADuC7019/20/21/22/24/25/26/27/28/29 for the PLA. These include 16 input pins and 14 output pins, which msut be configured in the GPxCON register as PLA pins before using the PLA. Note that the comparator output is also included as one of the 16 input pins.

The PLA is configured via a set of user MMRs. The output(s) of the PLA can be routed to the internal interrupt system, to the $\overline{\text{CONV}}_{\text{START}}$ signal of the ADC, to an MMR, or to any of the 16 PLA output pins.

The two blocks can be interconnected as follows:

- Output of Element 15 (Block 1) can be fed back to Input 0 of Mux 0 of Element 0 (Block 0).
- Output of Element 7 (Block 0) can be fed back to the Input 0 of Mux 0 of Element 8 (Block 1).

Table 145. Element Input/Output

PLA Block 0			PLA Block 1		
Element	**Input**	**Output**	**Element**	**Input**	**Output**
0	P1.0	P1.7	8	P3.0	P4.0
1	P1.1	P0.4	9	P3.1	P4.1
2	P1.2	P0.5	10	P3.2	P4.2
3	P1.3	P0.6	11	P3.3	P4.3
4	P1.4	P0.7	12	P3.4	P4.4
5	P1.5	P2.0	13	P3.5	P4.5
6	P1.6	P2.1	14	P3.6	P4.6
7	P0.0	P2.2	15	P3.7	P4.7

PLA MMRs Interface

The PLA peripheral interface consists of the 22 MMRs described in this section.

Table 146. PLAELMx Registers

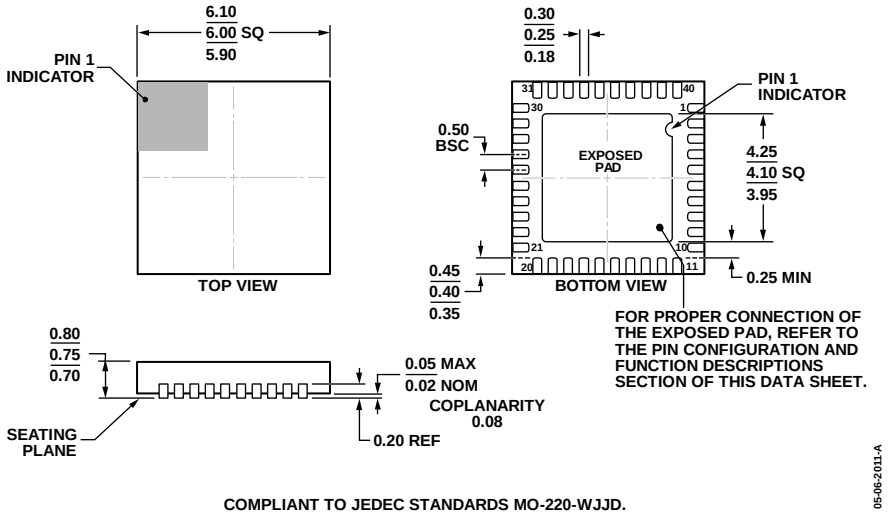
Name	Address	Default Value	Access
PLAELM0	0xFFFF0B00	0x0000	R/W
PLAELM1	0xFFFF0B04	0x0000	R/W
PLAELM2	0xFFFF0B08	0x0000	R/W
PLAELM3	0xFFFF0B0C	0x0000	R/W
PLAELM4	0xFFFF0B10	0x0000	R/W
PLAELM5	0xFFFF0B14	0x0000	R/W
PLAELM6	0xFFFF0B18	0x0000	R/W
PLAELM7	0xFFFF0B1C	0x0000	R/W
PLAELM8	0xFFFF0B20	0x0000	R/W
PLAELM9	0xFFFF0B24	0x0000	R/W
PLAELM10	0xFFFF0B28	0x0000	R/W
PLAELM11	0xFFFF0B2C	0x0000	R/W
PLAELM12	0xFFFF0B30	0x0000	R/W
PLAELM13	0xFFFF0B34	0x0000	R/W
PLAELM14	0xFFFF0B38	0x0000	R/W
PLAELM15	0xFFFF0B3C	0x0000	R/W

PLAELMx are Element 0 to Element 15 control registers. They configure the input and output mux of each element, select the function in the lookup table, and bypass/use the flip-flop. See Table 147 and Table 152.

Table 147. PLAELMx MMR Bit Descriptions

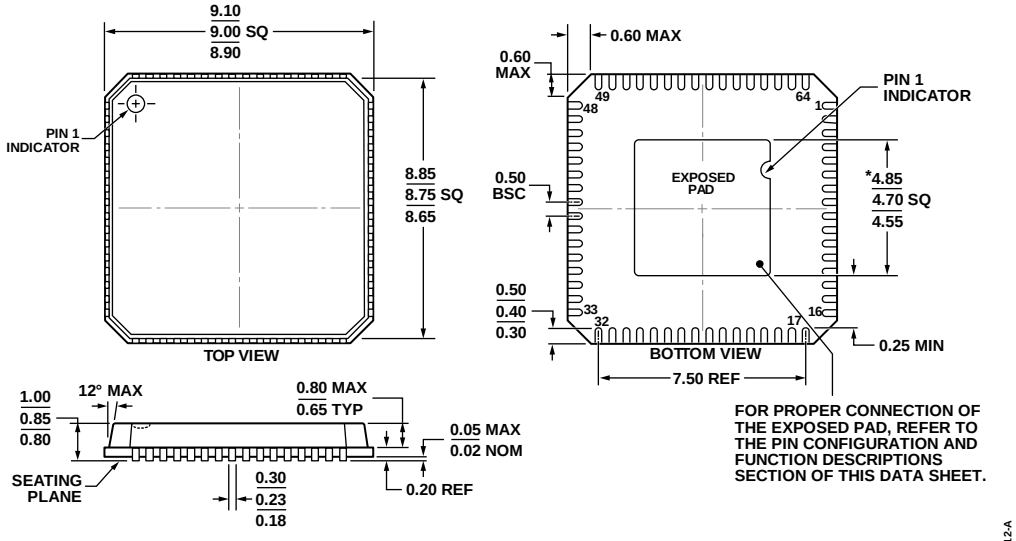
Bit	Value	Description
31:11		Reserved.
10:9		Mux 0 control (see Table 152).
8:7		Mux 1 control (see Table 152).
6		Mux 2 control. Set by user to select the output of Mux 0. Cleared by user to select the bit value from PLADIN.
5		Mux 3 control. Set by user to select the input pin of the particular element. Cleared by user to select the output of Mux 1.
4:1		Lookup table control.
	0000	0.
	0001	NOR.
	0010	B AND NOT A.
	0011	NOT A.
	0100	A AND NOT B.
	0101	NOT B.
	0110	EXOR.
	0111	NAND.
	1000	AND.
	1001	EXNOR.
	1010	B.
	1011	NOT A OR B.
	1100	A.
	1101	A OR NOT B.
	1110	OR.
	1111	1.
0		Mux 4 control. Set by user to bypass the flip-flop. Cleared by user to select the flip-flop (cleared by default).

OUTLINE DIMENSIONS



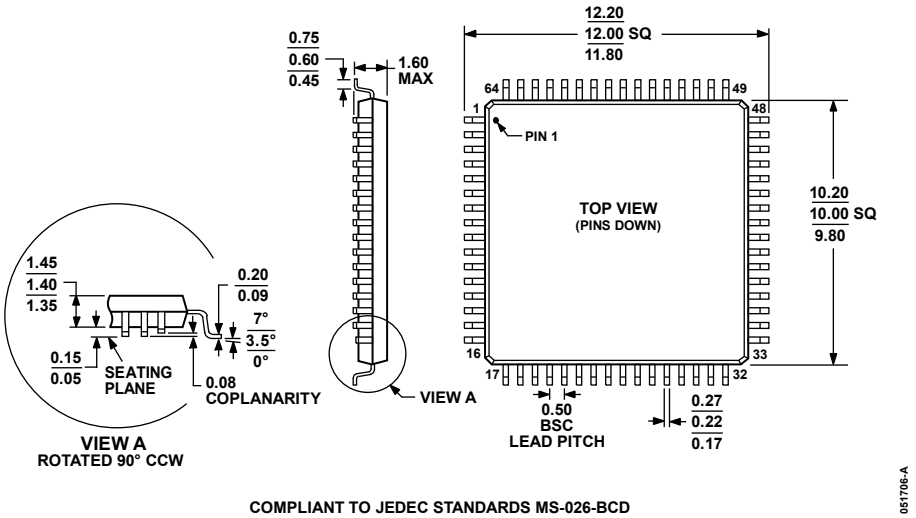
COMPLIANT TO JEDEC STANDARDS MO-220-WJJD.

Figure 96. 40-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
6 × 6 mm Body, Very Very Thin Quad
(CP-40-9)
Dimensions shown in millimeters



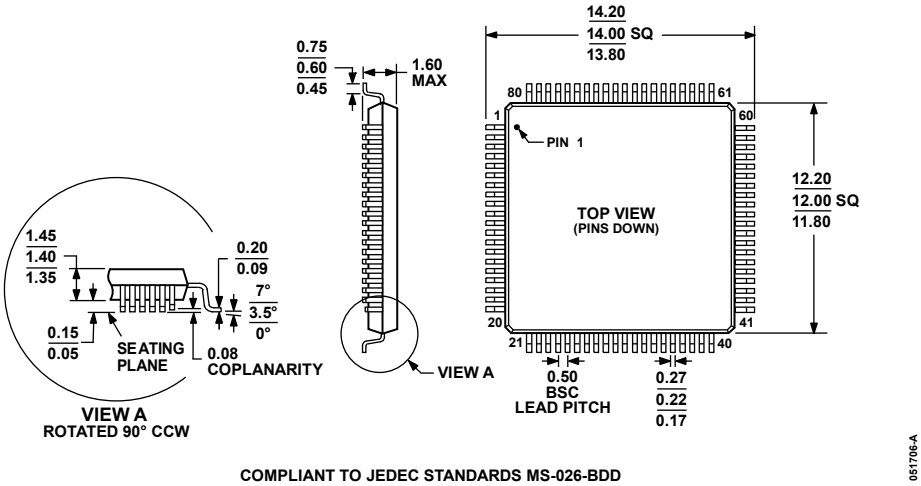
*COMPLIANT TO JEDEC STANDARDS MO-220-VMMD-4
EXCEPT FOR EXPOSED PAD DIMENSION

Figure 97. 64-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
9 mm × 9 mm Body, Very Thin Quad
(CP-64-1)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-026-BCD

Figure 98. 64-Lead Low Profile Quad Flat Package [LQFP]
(ST-64-2)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-026-BDD

Figure 99. 80-Lead Low Profile Quad Flat Package [LQFP]
(ST-80-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2]	ADC Channels[3]	DAC Channels	FLASH/ RAM	GPIO	Down-loader	Temperature Range	Package Description	Package Option	Ordering Quantity
ADuC7019BCPZ62I	5	3	62 kB/8 kB	14	I²C	−40°C to +125°C	40-Lead LFCSP_WQ	CP-40-9	
ADuC7019BCPZ62I-RL	5	3	62 kB/8 kB	14	I²C	−40°C to +125°C	40-Lead LFCSP_WQ	CP-40-9	2,500
ADuC7019BCPZ62IRL7	5	3	62 kB/8 kB	14	I²C	−40°C to +125°C	40-Lead LFCSP_WQ	CP-40-9	750
ADuC7020BCPZ62	5	4	62 kB/8 kB	14	UART	−40°C to +125°C	40-Lead LFCSP_WQ	CP-40-9	
ADuC7020BCPZ62-RL7	5	4	62 kB/8 kB	14	UART	−40°C to +125°C	40-Lead LFCSP_WQ	CP-40-9	750
ADuC7020BCPZ62I	5	4	62 kB/8 kB	14	I²C	−40°C to +125°C	40-Lead LFCSP_WQ	CP-40-9	
ADuC7020BCPZ62I-RL	5	4	62 kB/8 kB	14	I²C	−40°C to +125°C	40-Lead LFCSP_WQ	CP-40-9	2,500
ADuC7020BCPZ62IRL7	5	4	62 kB/8 kB	14	I²C	−40°C to +125°C	40-Lead LFCSP_WQ	CP-40-9	750
ADuC7021BCPZ62	8	2	62 kB/8 kB	13	UART	−40°C to +125°C	40-Lead LFCSP_WQ	CP-40-9	
ADuC7021BCPZ62-RL	8	2	62 kB/8 kB	13	UART	−40°C to +125°C	40-Lead LFCSP_WQ	CP-40-9	2,500
ADuC7021BCPZ62-RL7	8	2	62 kB/8 kB	13	UART	−40°C to +125°C	40-Lead LFCSP_WQ	CP-40-9	750
ADuC7021BCPZ62I	8	2	62 kB/8 kB	13	I²C	−40°C to +125°C	40-Lead LFCSP_WQ	CP-40-9	
ADuC7021BCPZ62I-RL	8	2	62 kB/8 kB	13	I²C	−40°C to +125°C	40-Lead LFCSP_WQ	CP-40-9	2,500
ADuC7021BCPZ32	8	2	32 kB/4 kB	13	UART	−40°C to +125°C	40-Lead LFCSP_WQ	CP-40-9	
ADuC7021BCPZ32-RL7	8	2	32 kB/4 kB	13	UART	−40°C to +125°C	40-Lead LFCSP_WQ	CP-40-9	750
ADuC7022BCPZ62	10		62 kB/8 kB	13	UART	−40°C to +125°C	40-Lead LFCSP_WQ	CP-40-9	
ADuC7022BCPZ62-RL7	10		62 kB/8 kB	13	UART	−40°C to +125°C	40-Lead LFCSP_WQ	CP-40-9	750
ADuC7022BCPZ32	10		32 kB/4 kB	13	UART	−40°C to +125°C	40-Lead LFCSP_WQ	CP-40-9	
ADuC7022BCPZ32-RL	10		32 kB/4 kB	13	UART	−40°C to +125°C	40-Lead LFCSP_WQ	CP-40-9	2,500
ADuC7024BCPZ62	10	2	62 kB/8 kB	30	UART	−40°C to +125°C	64-Lead LFCSP_VQ	CP-64-1	
ADuC7024BCPZ62-RL7	10	2	62 kB/8 kB	30	UART	−40°C to +125°C	64-Lead LFCSP_VQ	CP-64-1	750
ADuC7024BCPZ62I	10	2	62 kB/8 kB	30	I²C	−40°C to +125°C	64-Lead LFCSP_VQ	CP-64-1	
ADuC7024BCPZ62I-RL	10	2	62 kB/8 kB	30	I²C	−40°C to +125°C	64-Lead LFCSP_VQ	CP-64-1	2,500
ADuC7024BSTZ62	10	2	62 kB/8 kB	30	UART	−40°C to +125°C	64-Lead LQFP	ST-64-2	
ADuC7024BSTZ62-RL	10	2	62 kB/8 kB	30	UART	−40°C to +125°C	64-Lead LQFP	ST-64-2	1,000
ADuC7025BCPZ62	12		62 kB/8 kB	30	UART	−40°C to +125°C	64-Lead LFCSP_VQ	CP-64-1	
ADuC7025BCPZ62-RL	12		62 kB/8 kB	30	UART	−40°C to +125°C	64-Lead LFCSP_VQ	CP-64-1	2,500
ADuC7025BCPZ32	12		32 kB/4 kB	30	UART	−40°C to +125°C	64-Lead LFCSP_VQ	CP-64-1	
ADuC7025BCPZ32-RL	12		32 kB/4 kB	30	UART	−40°C to +125°C	64-Lead LFCSP_VQ	CP-64-1	2,500
ADuC7025BSTZ62	12		62 kB/8 kB	30	UART	−40°C to +125°C	64-Lead LQFP	ST-64-2	
ADuC7025BSTZ62-RL	12		62 kB/8 kB	30	UART	−40°C to +125°C	64-Lead LQFP	ST-64-2	1,000
ADuC7026BSTZ62	12	4	62 kB/8 kB	40	UART	−40°C to +125°C	80-Lead LQFP	ST-80-1	
ADuC7026BSTZ62-RL	12	4	62 kB/8 kB	40	UART	−40°C to +125°C	80-Lead LQFP	ST-80-1	1,000
ADuC7026BSTZ62I	12	4	62 kB/8 kB	40	I²C	−40°C to +125°C	80-Lead LQFP	ST-80-1	
ADuC7026BSTZ62I-RL	12	4	62 kB/8 kB	40	I²C	−40°C to +125°C	80-Lead LQFP	ST-80-1	1,000
ADuC7027BSTZ62	16		62 kB/8 kB	40	UART	−40°C to +125°C	80-Lead LQFP	ST-80-1	
ADuC7027BSTZ62-RL	16		62 kB/8 kB	40	UART	−40°C to +125°C	80-Lead LQFP	ST-80-1	1,000
ADuC7027BSTZ62I	16		62 kB/8 kB	40	I²C	−40°C to +125°C	80-Lead LQFP	ST-80-1	
ADuC7027BSTZ62I-RL	16		62 kB/8 kB	40	I²C	−40°C to +125°C	80-Lead LQFP	ST-80-1	1,000
ADuC7028BBCZ62	8	4	62 kB/8 kB	30	UART	−40°C to +125°C	64-Ball CSP_BGA	BC-64-4	
ADuC7028BBCZ62-RL	8	4	62 kB/8 kB	30	UART	−40°C to +125°C	64-Ball CSP_BGA	BC-64-4	2,500
ADuC7029BBCZ62	7	4	62 kB/8 kB	22	UART	−40°C to +125°C	49-Ball CSP_BGA	BC-49-1	
ADuC7029BBCZ62-RL	7	4	62 kB/8 kB	22	UART	−40°C to +125°C	49-Ball CSP_BGA	BC-49-1	4,000
ADuC7029BBCZ62I	7	4	62 kB/8 kB	22	I²C	−40°C to +125°C	49-Ball CSP_BGA	BC-49-1	
ADuC7029BBCZ62I-RL	7	4	62 kB/8 kB	22	I²C	−40°C to +125°C	49-Ball CSP_BGA	BC-49-1	4,000

Model[1, 2]	ADC Channels[3]	DAC Channels	FLASH/ RAM	GPIO	Down-loader	Temperature Range	Package Description	Package Option	Ordering Quantity
EVAL-ADuC7020MKZ							ADuC7020 MiniKit		
EVAL-ADuC7020QSZ							ADuC7020 QuickStart Development System		
EVAL-ADuC7020QSPZ							ADuC7020 QuickStart Development System		
EVAL-ADuC7024QSZ							ADuC7024 QuickStart Development System		
EVAL-ADuC7026QSZ							ADuC7026 QuickStar Development System		
EVAL-ADuC7026QSPZ							ADuC7026 QuickStart Plus Development System		
EVAL-ADuC7028QSZ							ADuC7028 QuickStart Development System		
EVAL-ADUC7029QSZ							ADuC7029 QuickStart Development System		

[1] Z = RoHS Compliant Part.
[2] Models ADuC7026 and ADuC7027 include an external memory interface.
[3] One of the ADC channels is internally buffered for ADuC7019 models.

I²C refers to a communications protocol originally developed by Phillips Semiconductors (now NXP Semiconductors).