Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	44MHz
Connectivity	EBI/EMI, I²C, SPI, UART/USART
Peripherals	PLA, PWM, PSM, Temp Sensor, WDT
Number of I/O	40
Program Memory Size	62KB (31K x16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 32
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 12 x12b; D/A 4x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/aduc7026bstz62

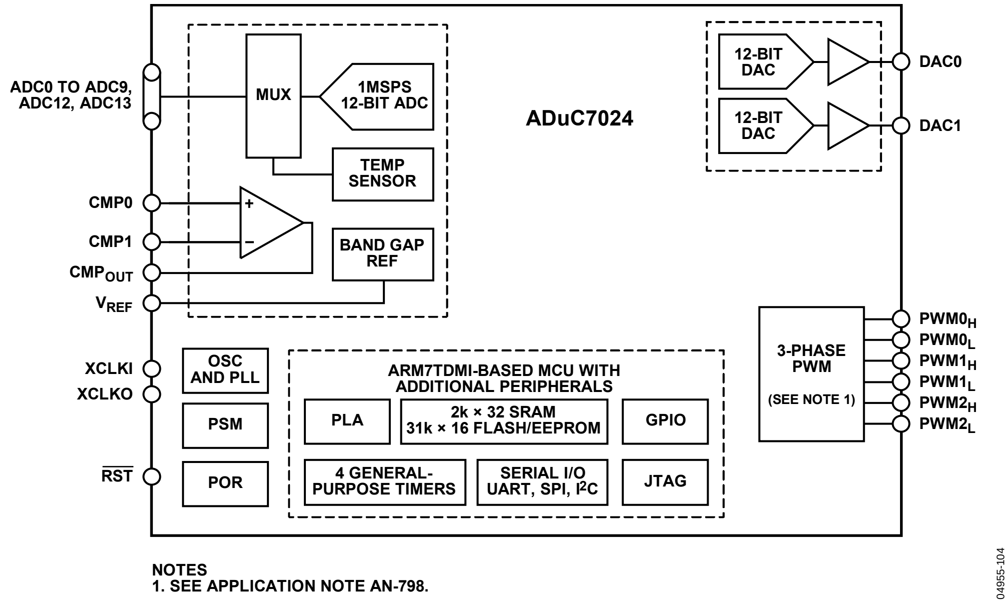

Figure 5.

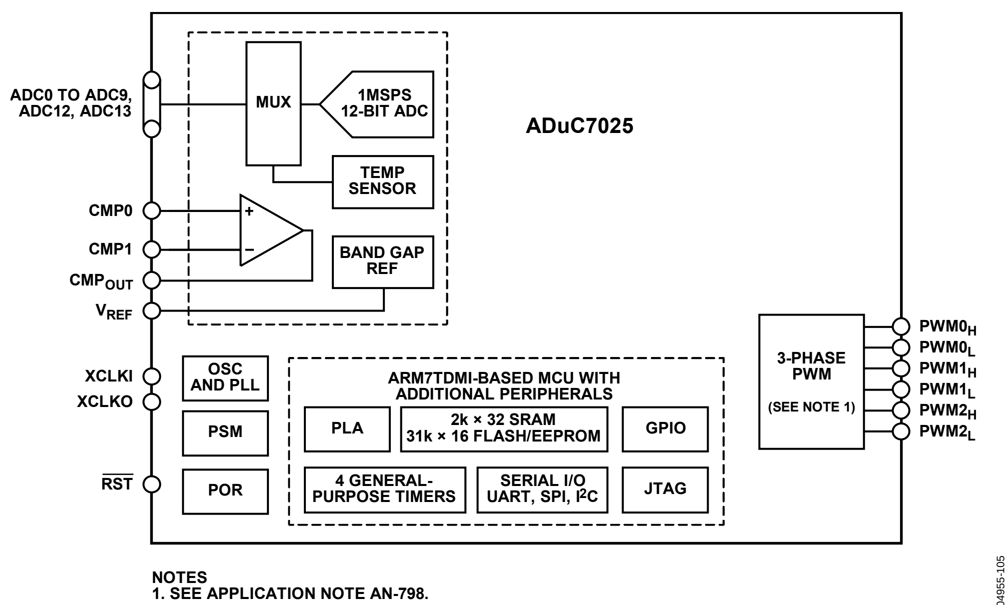

Figure 6.

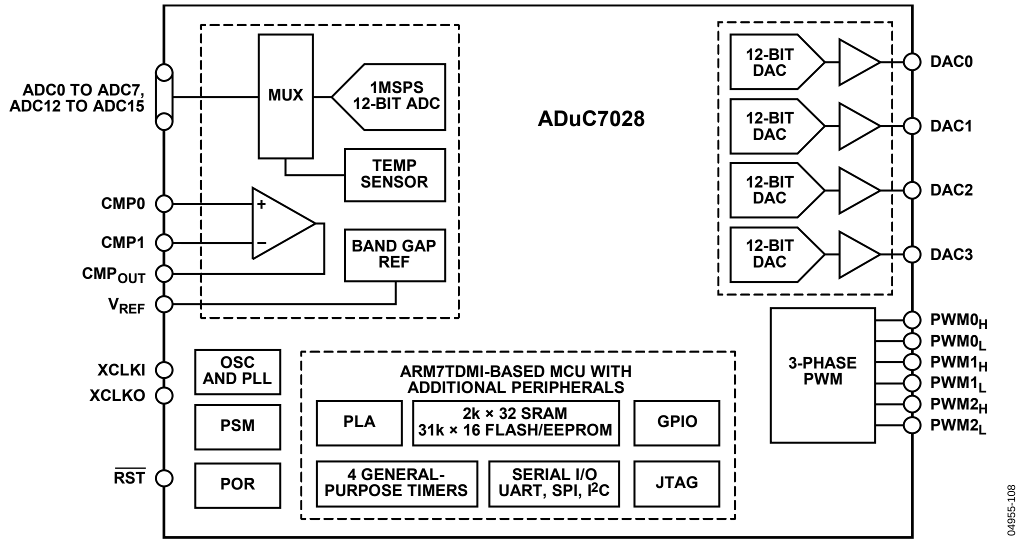

Figure 9.

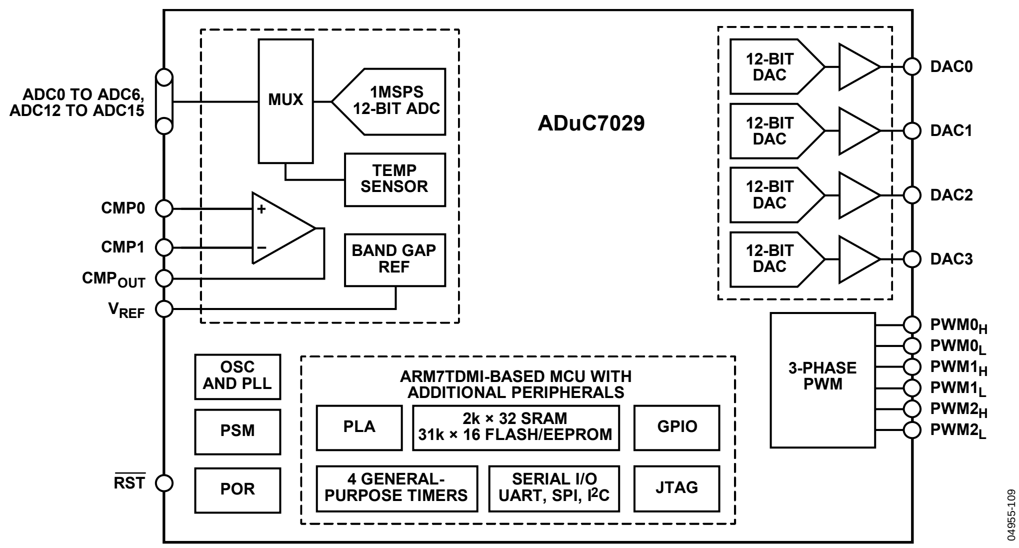

Figure 10.

SPECIFICATIONS

$AV_{DD} = IOV_{DD}$ = 2.7 V to 3.6 V, V_{REF} = 2.5 V internal reference, f_{CORE} = 41.78 MHz, T_A = −40°C to +125°C, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
ADC CHANNEL SPECIFICATIONS					Eight acquisition clocks and fADC/2
ADC Power-Up Time		5		µs	
DC Accuracy[1, 2]					
Resolution	12			Bits	
Integral Nonlinearity		±0.6	±1.5	LSB	2.5 V internal reference
		±1.0		LSB	1.0 V external reference
Differential Nonlinearity[3, 4]		±0.5	+1/−0.9	LSB	2.5 V internal reference
		+0.7/−0.6		LSB	1.0 V external reference
DC Code Distribution		1		LSB	ADC input is a dc voltage
ENDPOINT ERRORS[5]					
Offset Error		±1	±2	LSB	
Offset Error Match		±1		LSB	
Gain Error		±2	±5	LSB	
Gain Error Match		±1		LSB	
DYNAMIC PERFORMANCE					f_{IN} = 10 kHz sine wave, f_{SAMPLE} = 1 MSPS
Signal-to-Noise Ratio (SNR)		69		dB	Includes distortion and noise components
Total Harmonic Distortion (THD)		−78		dB	
Peak Harmonic or Spurious Noise (PHSN)		−75		dB	
Channel-to-Channel Crosstalk		−80		dB	Measured on adjacent channels
ANALOG INPUT					
Input Voltage Ranges					
Differential Mode			V_{CM}[6] ± $V_{REF}/2$	V	
Single-Ended Mode			0 to V_{REF}	V	
Leakage Current		±1	±6	µA	
Input Capacitance		20		pF	During ADC acquisition
ON-CHIP VOLTAGE REFERENCE					0.47 µF from V_{REF} to AGND
Output Voltage		2.5		V	
Accuracy			±5	mV	T_A = 25°C
Reference Temperature Coefficient		±40		ppm/°C	
Power Supply Rejection Ratio		75		dB	
Output Impedance		70		Ω	T_A = 25°C
Internal V_{REF} Power-On Time		1		ms	
EXTERNAL REFERENCE INPUT					
Input Voltage Range	0.625		AV_{DD}	V	
DAC CHANNEL SPECIFICATIONS					R_L = 5 kΩ, C_L = 100 pF
DC Accuracy[7]					
Resolution		12		Bits	
Relative Accuracy		±2		LSB	
Differential Nonlinearity			±1	LSB	Guaranteed monotonic
Offset Error			±15	mV	2.5 V internal reference
Gain Error[8]			±1	%	
Gain Error Mismatch		0.1		%	% of full scale on DAC0
ANALOG OUTPUTS					
Output Voltage Range_0		0 to DAC_{REF}		V	DAC_{REF} range: DACGND to $DACV_{DD}$
Output Voltage Range_1		0 to 2.5		V	
Output Voltage Range_2		0 to $DACV_{DD}$		V	
Output Impedance		2		Ω	

TIMING SPECIFICATIONS

Table 2. External Memory Write Cycle

Parameter	Min	Typ	Max	Unit
CLK[1]		UCLK		
$t_{MS\_AFTER\_CLKH}$	0		4	ns
$t_{ADDR\_AFTER\_CLKH}$	4		8	ns
$t_{AE\_H\_AFTER\_MS}$		½ CLK		
t_{AE}		(XMxPAR[14:12] + 1) × CLK		
$t_{HOLD\_ADDR\_AFTER\_AE\_L}$		½ CLK + (!XMxPAR[10]) × CLK		
$t_{HOLD\_ADDR\_BEFORE\_WR\_L}$		(!XMxPAR[8]) × CLK		
$t_{WR\_L\_AFTER\_AE\_L}$		½ CLK + (!XMxPAR[10] + !XMxPAR[8]) × CLK		
$t_{DATA\_AFTER\_WR\_L}$	8		12	ns
t_{WR}		(XMxPAR[7:4] + 1) × CLK		
$t_{WR\_H\_AFTER\_CLKH}$	0		4	ns
$t_{HOLD\_DATA\_AFTER\_WR\_H}$		(!XMxPAR[8]) × CLK		
$t_{BEN\_AFTER\_AE\_L}$		½ CLK		
$t_{RELEASE\_MS\_AFTER\_WR\_H}$		(!XMxPAR[8] + 1) × CLK		

[1] See Table 78.

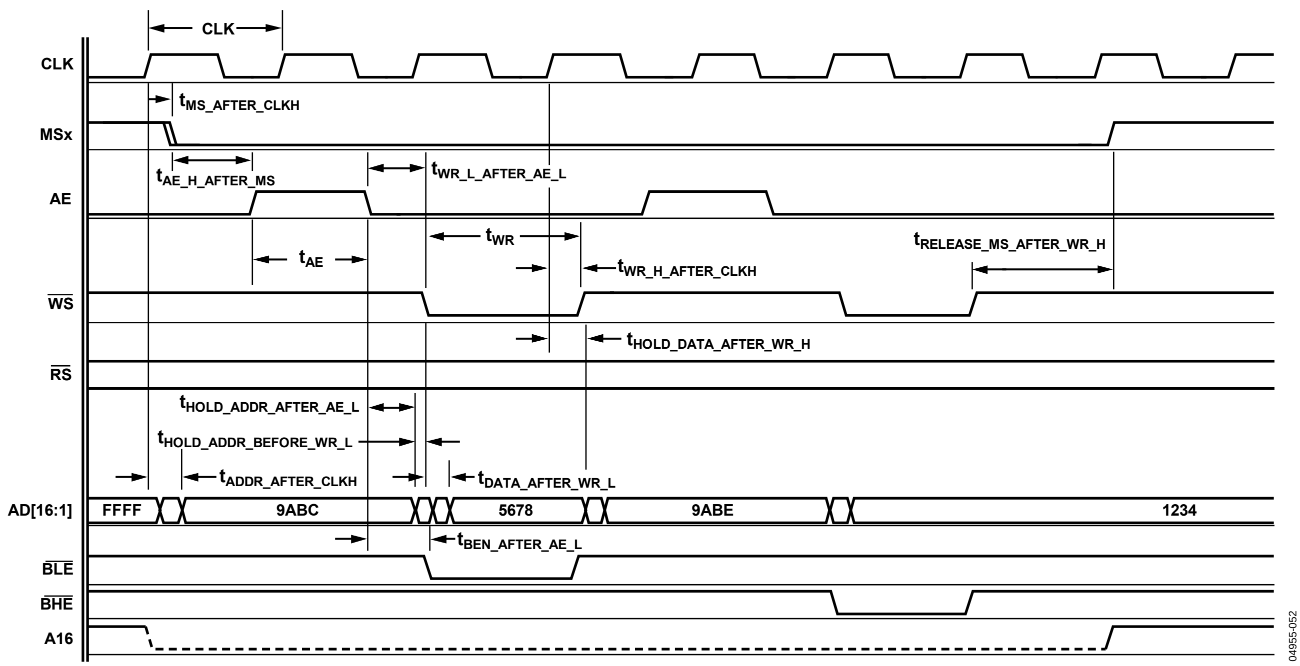

Figure 12. External Memory Write Cycle (See Table 78)

Pin No.			Mnemonic	Description
7019/7020	7021	7022		
22	22	21	P2.0/SPM9/PLAO[5]/$\overline{\text{CONV}_{\text{START}}}$	Serial Port Multiplexed. General-Purpose Input and Output Port 2.0/UART/ Programmable Logic Array Output Element 5/Start Conversion Input Signal for ADC.
23	23	22	P0.7/ECLK/XCLK/SPM8/PLAO[4]	Serial Port Multiplexed. General-Purpose Input and Output Port 0.7/ Output for External Clock Signal/Input to the Internal Clock Generator Circuits/UART/ Programmable Logic Array Output Element 4.
24	24	23	XCLKO	Output from the Crystal Oscillator Inverter.
25	25	24	XCLKI	Input to the Crystal Oscillator Inverter and Input to the Internal Clock Generator Circuits.
26	26	25	P1.7/SPM7/PLAO[0]	Serial Port Multiplexed. General-Purpose Input and Output Port 1.7/UART, SPI/Programmable Logic Array Output Element 0.
27	27	26	P1.6/SPM6/PLAI[6]	Serial Port Multiplexed. General-Purpose Input and Output Port 1.6/UART, SPI/Programmable Logic Array Input Element 6.
28	28	27	P1.5/SPM5/PLAI[5]/IRQ3	Serial Port Multiplexed. General-Purpose Input and Output Port 1.5/UART, SPI/Programmable Logic Array Input Element 5/External Interrupt Request 3, Active High.
29	29	28	P1.4/SPM4/PLAI[4]/IRQ2	Serial Port Multiplexed. General-Purpose Input and Output Port 1.4/UART, SPI/Programmable Logic Array Input Element 4/External Interrupt Request 2, Active High.
30	30	29	P1.3/SPM3/PLAI[3]	Serial Port Multiplexed. General-Purpose Input and Output Port 1.3/UART, I2C1/Programmable Logic Array Input Element 3.
31	31	30	P1.2/SPM2/PLAI[2]	Serial Port Multiplexed. General-Purpose Input and Output Port 1.2/UART, I2C1/Programmable Logic Array Input Element 2.
32	32	31	P1.1/SPM1/PLAI[1]	Serial Port Multiplexed. General-Purpose Input and Output Port 1.1/UART, I2C0/Programmable Logic Array Input Element 1.
33	33	32	P1.0/T1/SPM0/PLAI[0]	Serial Port Multiplexed. General-Purpose Input and Output Port 1.0/ Timer1 Input/UART, I2C0/Programmable Logic Array Input Element 0.
34	–	–	P4.2/PLAO[10]	General-Purpose Input and Output Port 4.2/Programmable Logic Array Output Element 10.
35	34	33	V_{REF}	2.5 V Internal Voltage Reference. Must be connected to a 0.47 μF capacitor when using the internal reference.
36	35	34	AGND	Analog Ground. Ground reference point for the analog circuitry.
37	36	35	AV_{DD}	3.3 V Analog Power.
0	0	0	EP	Exposed Pad. The pin configuration for the ADuC7019/ADuC7020/ ADuC7021/ADuC7022 has an exposed pad that must be soldered for mechanical purposes and left unconnected.

Table 12. Pin Function Descriptions (ADuC7024/ADuC7025 64-Lead LFCSP_VQ and 64-Lead LQFP)

Pin No.	Mnemonic	Description
1	ADC4	Single-Ended or Differential Analog Input 4.
2	ADC5	Single-Ended or Differential Analog Input 5.
3	ADC6	Single-Ended or Differential Analog Input 6.
4	ADC7	Single-Ended or Differential Analog Input 7.
5	ADC8	Single-Ended or Differential Analog Input 8.
6	ADC9	Single-Ended or Differential Analog Input 9.
7	GND_{REF}	Ground Voltage Reference for the ADC. For optimal performance, the analog power supply should be separated from IOGND and DGND.
8	ADCNEG	Bias Point or Negative Analog Input of the ADC in Pseudo Differential Mode. Must be connected to the ground of the signal to convert. This bias point must be between 0 V and 1 V.
9	DAC0/ADC12	DAC0 Voltage Output/Single-Ended or Differential Analog Input 12. DAC outputs are not present on the ADuC7025.
10	DAC1/ADC13	DAC1 Voltage Output/Single-Ended or Differential Analog Input 13. DAC outputs are not present on the ADuC7025.
11	TMS	JTAG Test Port Input, Test Mode Select. Debug and download access.
12	TDI	JTAG Test Port Input, Test Data In. Debug and download access
13	P4.6/PLAO[14]	General-Purpose Input and Output Port 4.6/Programmable Logic Array Output Element 14.
14	P4.7/PLAO[15]	General-Purpose Input and Output Port 4.7/Programmable Logic Array Output Element 15.
15	BM/P0.0/CMP_{OUT}/PLAI[7]	Multifunction I/O Pin. Boot mode. The ADuC7024/ADuC7025 enter download mode if BM is low at reset and execute code if BM is pulled high at reset through a 1 kΩ resistor/General-Purpose Input and Output Port 0.0/Voltage Comparator Output/Programmable Logic Array Input Element 7.
16	P0.6/T1/MRST/PLAO[3]	Multifunction Pin, Driven Low After Reset. General-Purpose Output Port 0.6/Timer1 Input/Power-On Reset Output/Programmable Logic Array Output Element 3.
17	TCK	JTAG Test Port Input, Test Clock. Debug and download access.
18	TDO	JTAG Test Port Output, Test Data Out. Debug and download access.
19	IOGND	Ground for GPIO (see Table 78). Typically connected to DGND.
20	IOV_{DD}	3.3 V Supply for GPIO (see Table 78) and Input of the On-Chip Voltage Regulator.
21	LV_{DD}	2.6 V Output of the On-Chip Voltage Regulator. This output must be connected to a 0.47 µF capacitor to DGND only.
22	DGND	Ground for Core Logic.
23	P3.0/$PWM0_H$/PLAI[8]	General-Purpose Input and Output Port 3.0/PWM Phase 0 High-Side Output/Programmable Logic Array Input Element 8.
24	P3.1/$PWM0_L$/PLAI[9]	General-Purpose Input and Output Port 3.1/PWM Phase 0 Low-Side Output/Programmable Logic Array Input Element 9.
25	P3.2/$PWM1_H$/PLAI[10]	General-Purpose Input and Output Port 3.2/PWM Phase 1 High-Side Output/Programmable Logic Array Input Element 10.
26	P3.3/$PWM1_L$/PLAI[11]	General-Purpose Input and Output Port 3.3/PWM Phase 1 Low-Side Output/Programmable Logic Array Input Element 11.
27	P0.3/TRST/ADC_{BUSY}	General-Purpose Input and Output Port 0.3/JTAG Test Port Input, Test Reset/ADC_{BUSY} Signal Output.
28	$\overline{RST}$	Reset Input, Active Low.
29	P3.4/$PWM2_H$/PLAI[12]	General-Purpose Input and Output Port 3.4/PWM Phase 2 High-Side Output/Programmable Logic Array Input 12.
30	P3.5/$PWM2_L$/PLAI[13]	General-Purpose Input and Output Port 3.5/PWM Phase 2 Low-Side Output/Programmable Logic Array Input Element 13.
31	IRQ0/P0.4/PWM_{TRIP}/PLAO[1]	Multifunction I/O Pin. External Interrupt Request 0, Active High/General-Purpose Input and Output Port 0.4/PWM Trip External Input/Programmable Logic Array Output Element 1.
32	IRQ1/P0.5/ADC_{BUSY}/PLAO[2]	Multifunction I/O Pin. External Interrupt Request 1, Active High/General-Purpose Input and Output Port 0.5/ADC_{BUSY} Signal Output/Programmable Logic Array Output Element 2.
33	P2.0/SPM9/PLAO[5]/$\overline{CONV_{START}}$	Serial Port Multiplexed. General-Purpose Input and Output Port 2.0/UART/Programmable Logic Array Output Element 5/Start Conversion Input Signal for ADC.
34	P0.7/ECLK/XCLK/SPM8/PLAO[4]	Serial Port Multiplexed. General-Purpose Input and Output Port 0.7/Output for External Clock Signal/Input to the Internal Clock Generator Circuits/UART/Programmable Logic Array Output Element 4.
35	XCLKO	Output from the Crystal Oscillator Inverter.
36	XCLKI	Input to the Crystal Oscillator Inverter and Input to the Internal Clock Generator Circuits.

Pin No.	Mnemonic	Description
18	P4.6/AD14/PLAO[14]	General-Purpose Input and Output Port 4.6/External Memory Interface/Programmable Logic Array Output Element 14.
19	P4.7/AD15/PLAO[15]	General-Purpose Input and Output Port 4.7/External Memory Interface/Programmable Logic Array Output Element 15.
20	BM/P0.0/CMP_{OUT}/PLAI[7]/MS0	Multifunction I/O Pin. Boot Mode. The ADuC7026/ADuC7027 enter UART download mode if BM is low at reset and execute code if BM is pulled high at reset through a 1 kΩ resistor/General-Purpose Input and Output Port 0.0/Voltage Comparator Output/Programmable Logic Array Input Element 7/External Memory Select 0.
21	P0.6/T1/MRST/PLAO[3]	Multifunction Pin, Driven Low After Reset. General-Purpose Output Port 0.6/Timer1 Input/ Power-On Reset Output/Programmable Logic Array Output Element 3.
22	TCK	JTAG Test Port Input, Test Clock. Debug and download access.
23	TDO	JTAG Test Port Output, Test Data Out. Debug and download access.
24	P0.2/$PWM2_L$/$\overline{BHE}$	General-Purpose Input and Output Port 0.2/PWM Phase 2 Low-Side Output/External Memory Byte High Enable.
25	IOGND	Ground for GPIO (see Table 78). Typically connected to DGND.
26	IOV_{DD}	3.3 V Supply for GPIO (see Table 78) and Input of the On-Chip Voltage Regulator.
27	LV_{DD}	2.6 V Output of the On-Chip Voltage Regulator. This output must be connected to a 0.47 µF capacitor to DGND only.
28	DGND	Ground for Core Logic.
29	P3.0/AD0/$PWM0_H$/PLAI[8]	General-Purpose Input and Output Port 3.0/External Memory Interface/PWM Phase 0 High-Side Output/Programmable Logic Array Input Element 8.
30	P3.1/AD1/$PWM0_L$/PLAI[9]	General-Purpose Input and Output Port 3.1/External Memory Interface/PWM Phase 0 Low-Side Output/Programmable Logic Array Input Element 9.
31	P3.2/AD2/$PWM1_H$/PLAI[10]	General-Purpose Input and Output Port 3.2/External Memory Interface/PWM Phase 1 High-Side Output/Programmable Logic Array Input Element 10.
32	P3.3/AD3/$PWM1_L$/PLAI[11]	General-Purpose Input and Output Port 3.3/External Memory Interface/PWM Phase 1 Low-Side Output/Programmable Logic Array Input Element 11.
33	P2.4/$PWM0_H$/MS0	General-Purpose Input and Output Port 2.4/PWM Phase 0 High-Side Output/External Memory Select 0.
34	P0.3/TRST/A16/ADC_{BUSY}	General-Purpose Input and Output Port 0.3/JTAG Test Port Input, Test Reset/ADC_{BUSY} Signal Output.
35	P2.5/$PWM0_L$/MS1	General-Purpose Input and Output Port 2.5/PWM Phase 0 Low-Side Output/External Memory Select 1.
36	P2.6/$PWM1_H$/MS2	General-Purpose Input and Output Port 2.6/PWM Phase 1 High-Side Output/External Memory Select 2.
37	$\overline{RST}$	Reset Input, Active Low.
38	P3.4/AD4/$PWM2_H$/PLAI[12]	General-Purpose Input and Output Port 3.4/External Memory Interface/PWM Phase 2 High-Side Output/Programmable Logic Array Input 12.
39	P3.5/AD5/$PWM2_L$/PLAI[13]	General-Purpose Input and Output Port 3.5/External Memory Interface/PWM Phase 2 Low-Side Output/Programmable Logic Array Input Element 13.
40	IRQ0/P0.4/PWM_{TRIP}/PLAO[1]/MS1	Multifunction I/O Pin. External Interrupt Request 0, Active High/General-Purpose Input and Output Port 0.4/PWM Trip External Input/Programmable Logic Array Output Element 1/ External Memory Select 1.
41	IRQ1/P0.5/ADC_{BUSY}/PLAO[2]/MS2	Multifunction I/O Pin. External Interrupt Request 1, Active High/General-Purpose Input and Output Port 0.5/ADC_{BUSY} Signal Output/Programmable Logic Array Output Element 2/External Memory Select 2.
42	P2.0/SPM9/PLAO[5]/$\overline{CONV_{START}}$	Serial Port Multiplexed. General-Purpose Input and Output Port 2.0/UART/Programmable Logic Array Output Element 5/Start Conversion Input Signal for ADC.
43	P0.7/ECLK/XCLK/SPM8/PLAO[4]	Serial Port Multiplexed. General-Purpose Input and Output Port 0.7/Output for External Clock Signal/Input to the Internal Clock Generator Circuits/UART/Programmable Logic Array Output Element 4.
44	XCLKO	Output from the Crystal Oscillator Inverter.
45	XCLKI	Input to the Crystal Oscillator Inverter and Input to the Internal Clock Generator Circuits.

Pin No.	Mnemonic	Description
D7	P1.6/SPM6/PLAI[6]	Serial Port Multiplexed. General-Purpose Input and Output Port 1.6/UART, SPI/Programmable Logic Array Input Element 6.
D8	IOV_{DD}	3.3 V Supply for GPIO (see Table 78) and Input of the On-Chip Voltage Regulator.
E1	DAC3/ADC15	DAC3 Voltage Output/ADC Input 15.
E2	DAC2/ADC14	DAC2 Voltage Output/ADC Input 14.
E3	DAC1/ADC13	DAC1 Voltage Output/ADC Input 13.
E4	P3.0/$PWM0_H$/PLAI[8]	General-Purpose Input and Output Port 3.0/PWM Phase 0 High-Side Output/Programmable Logic Array Input Element 8.
E5	P3.2/$PWM1_H$/PLAI[10]	General-Purpose Input and Output Port 3.2/PWM Phase 1 High-Side Output/Programmable Logic Array Input Element 10.
E6	P1.5/SPM5/PLAI[5]/IRQ3	Serial Port Multiplexed. General-Purpose Input and Output Port 1.5/UART, SPI/Programmable Logic Array Input Element 5/External Interrupt Request 3, Active High.
E7	P3.7/PWM_{SYNC}/PLAI[15]	General-Purpose Input and Output Port 3.7/PWM Synchronization/Programmable Logic Array Input Element 15.
E8	XCLKI	Input to the Crystal Oscillator Inverter and Input to the Internal Clock Generator Circuits.
F1	P4.6/PLAO[14]	General-Purpose Input and Output Port 4.6/Programmable Logic Array Output Element 14.
F2	TDI	JTAG Test Port Input, Test Data In. Debug and download access.
F3	DAC0/ADC12	DAC0 Voltage Output/ADC Input 12.
F4	P3.1/$PWM0_L$/PLAI[9]	General-Purpose Input and Output Port 3.1/PWM Phase 0 Low-Side Output/Programmable Logic Array Input Element 9.
F5	P3.3/$PWM1_L$/PLAI[11]	General-Purpose Input and Output Port 3.3/PWM Phase 1 Low-Side Output/Programmable Logic Array Input Element 11.
F6	$\overline{RST}$	Reset Input, Active Low.
F7	P0.7/ECLK/XCLK/SPM8/PLAO[4]	Serial Port Multiplexed. General-Purpose Input and Output Port 0.7/Output for External Clock Signal/Input to the Internal Clock Generator Circuits/UART/Programmable Logic Array Output Element 4.
F8	XCLKO	Output from the Crystal Oscillator Inverter.
G1	BM/P0.0/CMP_{OUT}/PLAI[7]	Multifunction I/O Pin. Boot mode. The ADuC7028 enters UART download mode if BM is low at reset and executes code if BM is pulled high at reset through a 1 kΩ resistor/General-Purpose Input and Output Port 0.0/Voltage Comparator Output/Programmable Logic Array Input Element 7.
G2	P4.7/PLAO[15]	General-Purpose Input and Output Port 4.7/Programmable Logic Array Output Element 15.
G3	TMS	JTAG Test Port Input, Test Mode Select. Debug and download access.
G4	TDO	JTAG Test Port Output, Test Data Out. Debug and download access.
G5	P0.3/TRST/ADC_{BUSY}	General-Purpose Input and Output Port 0.3/JTAG Test Port Input, Test Reset/ADC_{BUSY} Signal Output.
G6	P3.4/$PWM2_H$/PLAI[12]	General-Purpose Input and Output Port 3.4/PWM Phase 2 High-Side Output/Programmable Logic Array Input 12.
G7	P3.5/$PWM2_L$/PLAI[13]	General-Purpose Input and Output Port 3.5/PWM Phase 2 Low-Side Output/Programmable Logic Array Input Element 13.
G8	P2.0/SPM9/PLAO[5]/$\overline{CONV_{START}}$	Serial Port Multiplexed. General-Purpose Input and Output Port 2.0/UART/Programmable Logic Array Output Element 5/Start Conversion Input Signal for ADC.
H1	P0.6/T1/MRST/PLAO[3]	Multifunction Pin, Driven Low After Reset. General-Purpose Output Port 0.6/Timer1 Input/Power-On Reset Output/Programmable Logic Array Output Element 3.
H2	TCK	JTAG Test Port Input, Test Clock. Debug and download access.
H3	IOGND	Ground for GPIO (see Table 78). Typically connected to DGND.
H4	IOV_{DD}	3.3 V Supply for GPIO (see Table 78) and Input of the On-Chip Voltage Regulator.
H5	LV_{DD}	2.6 V Output of the On-Chip Voltage Regulator. This output must be connected to a 0.47 µF capacitor to DGND only.
H6	DGND	Ground for Core Logic.
H7	IRQ0/P0.4/PWM_{TRIP}/PLAO[1]	Multifunction I/O Pin. External Interrupt Request 0, Active High/General-Purpose Input and Output Port 0.4/PWM Trip External Input/Programmable Logic Array Output Element 1.
H8	IRQ1/P0.5/ADC_{BUSY}/PLAO[2]	Multifunction I/O Pin. External Interrupt Request 1, Active High/General-Purpose Input and Output Port 0.5/ADC_{BUSY} Signal Output/Programmable Logic Array Output Element 2.

TYPICAL PERFORMANCE CHARACTERISTICS

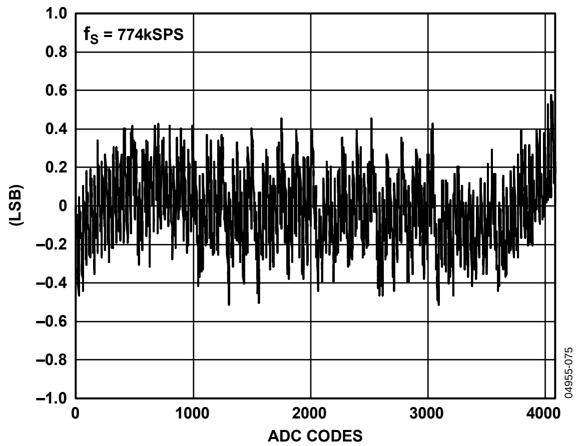

Figure 28. Typical INL Error, f_S = 774 kSPS

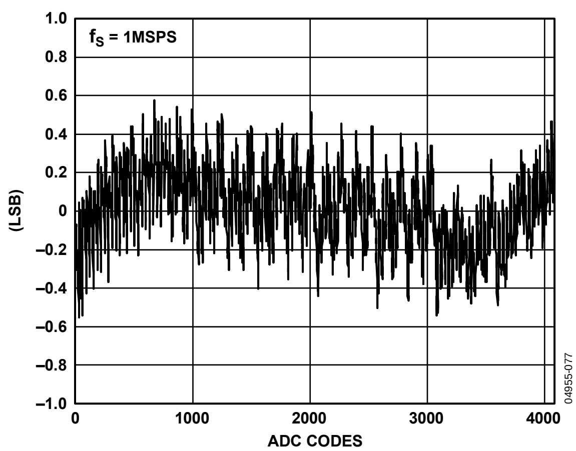

Figure 29. Typical INL Error, f_S = 1 MSPS

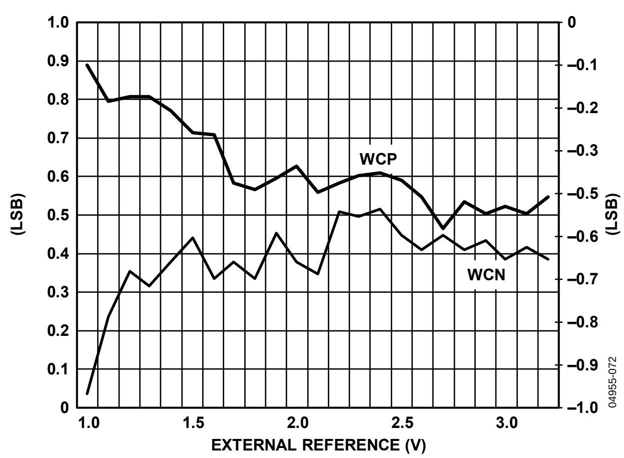

Figure 30. Typical Worst-Case (Positive (WCP) and Negative (WCN)) INL Error vs. V_{REF}, f_S = 774 kSPS

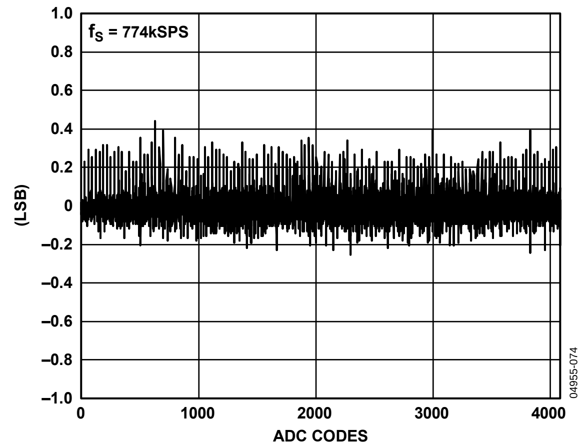

Figure 31. Typical DNL Error, f_S = 774 kSPS

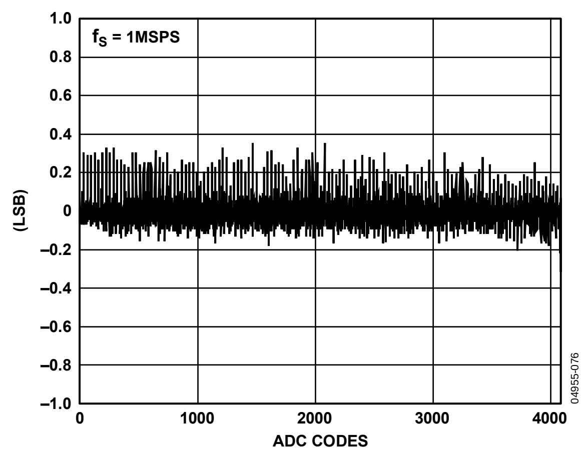

Figure 32. Typical DNL Error, f_S = 1 MSPS

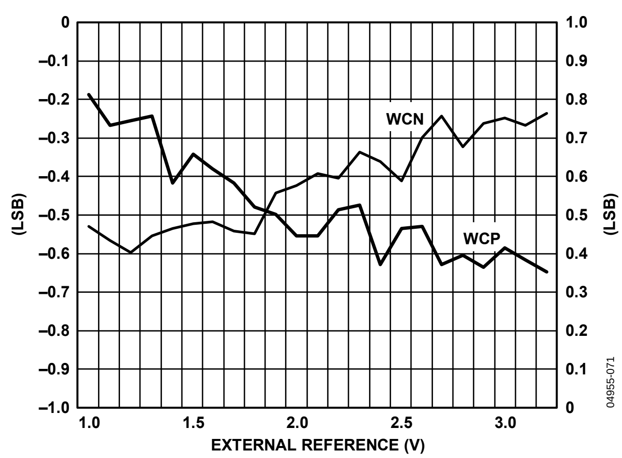

Figure 33. Typical Worst-Case (Positive (WCP)and Negative (WCN)) DNL Error vs. V_{REF}, f_S = 774 kSPS

TYPICAL OPERATION

Once configured via the ADC control and channel selection registers, the ADC converts the analog input and provides a 12-bit result in the ADC data register.

The top four bits are the sign bits. The 12-bit result is placed from Bit 16 to Bit 27, as shown in Figure 51. Again, it should be noted that, in fully differential mode, the result is represented in twos complement format. In pseudo differential and single-ended modes, the result is represented in straight binary format.

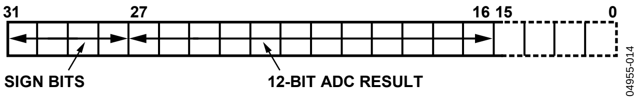

Figure 51. ADC Result Format

The same format is used in DACxDAT, simplifying the software.

Current Consumption

The ADC in standby mode, that is, powered up but not converting, typically consumes 640 µA. The internal reference adds 140 µA. During conversion, the extra current is 0.3 µA multiplied by the sampling frequency (in kilohertz (kHz)). Figure 43 shows the current consumption vs. the sampling frequency of the ADC.

Timing

Figure 52 gives details of the ADC timing. Users control the ADC clock speed and the number of acquisition clocks in the ADCCON MMR. By default, the acquisition time is eight clocks and the clock divider is 2. The number of extra clocks (such as bit trial or write) is set to 19, which gives a sampling rate of 774 kSPS. For conversion on the temperature sensor, the ADC acquisition time is automatically set to 16 clocks, and the ADC clock divider is set to 32. When using multiple channels, including the temperature sensor, the timing settings revert to the user-defined settings after reading the temperature sensor channel.

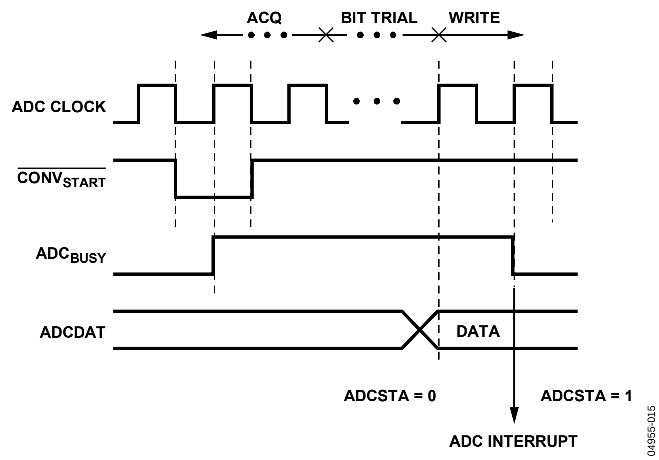

Figure 52. ADC Timing

ADuC7019

The ADuC7019 is identical to the ADuC7020 except for one buffered ADC channel, ADC3, and it has only three DACs. The output buffer of the fourth DAC is internally connected to the ADC3 channel as shown in Figure 53.

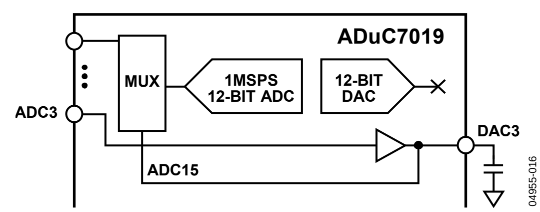

Figure 53. ADC3 Buffered Input

Note that the DAC3 output pin must be connected to a 10 nF capacitor to AGND. This channel should be used to measure dc voltages only. ADC calibration may be necessary on this channel.

MMRS INTERFACE

The ADC is controlled and configured via the eight MMRs described in this section.

Table 17. ADCCON Register

Name	Address	Default Value	Access
ADCCON	0xFFFF0500	0x0600	R/W

ADCCON is an ADC control register that allows the programmer to enable the ADC peripheral, select the mode of operation of the ADC (in single-ended mode, pseudo differential mode, or fully differential mode), and select the conversion type. This MMR is described in Table 18.

Table 28. V_{CM} Ranges

AV_{DD}	V_{REF}	V_{CM} Min	V_{CM} Max	Signal Peak-to-Peak
3.3 V	2.5 V	1.25 V	2.05 V	2.5 V
	2.048 V	1.024 V	2.276 V	2.048 V
	1.25 V	0.75 V	2.55 V	1.25 V
3.0 V	2.5 V	1.25 V	1.75 V	2.5 V
	2.048 V	1.024 V	1.976 V	2.048 V
	1.25 V	0.75 V	2.25 V	1.25 V

CALIBRATION

By default, the factory-set values written to the ADC offset (ADCOF) and gain coefficient registers (ADCGN) yield optimum performance in terms of end-point errors and linearity for standalone operation of the part (see the Specifications section). If system calibration is required, it is possible to modify the default offset and gain coefficients to improve end-point errors, but note that any modification to the factory-set ADCOF and ADCGN values can degrade ADC linearity performance.

For system offset error correction, the ADC channel input stage must be tied to AGND. A continuous software ADC conversion loop must be implemented by modifying the value in ADCOF until the ADC result (ADCDAT) reads Code 0 to Code 1. If the ADCDAT value is greater than 1, ADCOF should be decremented until ADCDAT reads 0 to 1. Offset error correction is done digitally and has a resolution of 0.25 LSB and a range of ±3.125% of V_{REF}.

For system gain error correction, the ADC channel input stage must be tied to V_{REF}. A continuous software ADC conversion loop must be implemented to modify the value in ADCGN until the ADC result (ADCDAT) reads Code 4094 to Code 4095. If the ADCDAT value is less than 4094, ADCGN should be incremented until ADCDAT reads 4094 to 4095. Similar to the offset calibration, the gain calibration resolution is 0.25 LSB with a range of ±3% of V_{REF}.

TEMPERATURE SENSOR

The ADuC7019/20/21/22/24/25/26/27/28/29 provide voltage output from on-chip band gap references proportional to absolute temperature. This voltage output can also be routed through the front-end ADC multiplexer (effectively an additional ADC channel input) facilitating an internal temperature sensor channel, measuring die temperature to an accuracy of ±3°C.

The following is an example routine showing how to use the internal temperature sensor:

```
int main(void)
{
float a = 0;
      short b;
      ADCCON = 0x20;    // power-on the ADC
      delay(2000);
      ADCCP = 0x10;  // Select Temperature
Sensor as an // input to the ADC
      REFCON = 0x01; // connect internal 2.5V
reference // to Vref pin
      ADCCON = 0xE4; // continuous conversion
      while(1)
      {
              while (!ADCSTA){};
      // wait for end of conversion
              b = (ADCDAT >> 16);
      // To calculate temperature in °C, use
the formula:
              a = 0x525 - b;
      // ((Temperature = 0x525 - Sensor
Voltage) / 1.3)
              a /= 1.3;
              b = floor(a);
              printf("Temperature: %d
oC\n",b);
      }
      return 0;
}
```

BAND GAP REFERENCE

Each ADuC7019/20/21/22/24/25/26/27/28/29 provides an on-chip band gap reference of 2.5 V, which can be used for the ADC and DAC. This internal reference also appears on the V_{REF} pin. When using the internal reference, a 0.47 μF capacitor must be connected from the external V_{REF} pin to AGND to ensure stability and fast response during ADC conversions. This reference can also be connected to an external pin (V_{REF}) and used as a reference for other circuits in the system. An external buffer is required because of the low drive capability of the V_{REF} output. A programmable option also allows an external reference input on the V_{REF} pin. Note that it is not possible to disable the internal reference. Therefore, the external reference source must be capable of overdriving the internal reference source.

Table 29. REFCON Register

Name	Address	Default Value	Access
REFCON	0xFFFF048C	0x00	R/W

The band gap reference interface consists of an 8-bit MMR REFCON, described in Table 30.

Table 30. REFCON MMR Bit Designations

Bit	Description
7:1	Reserved.
0	Internal reference output enable. Set by user to connect the internal 2.5 V reference to the V_{REF} pin. The reference can be used for an external component but must be buffered. Cleared by user to disconnect the reference from the V_{REF} pin.

OTHER ANALOG PERIPHERALS

DAC

The ADuC7019/20/21/22/24/25/26/27/28/29 incorporate two, three, or four 12-bit voltage output DACs on-chip, depending on the model. Each DAC has a rail-to-rail voltage output buffer capable of driving 5 kΩ/100 pF.

Each DAC has three selectable ranges: 0 V to V_{REF} (internal band gap 2.5 V reference), 0 V to DAC_{REF}, and 0 V to AV_{DD}. DAC_{REF} is equivalent to an external reference for the DAC. The signal range is 0 V to AV_{DD}.

MMRs Interface

Each DAC is independently configurable through a control register and a data register. These two registers are identical for the four DACs. Only DAC0CON (see Table 50) and DAC0DAT (see Table 52) are described in detail in this section.

Table 49. DACxCON Registers

Name	Address	Default Value	Access
DAC0CON	0xFFFF0600	0x00	R/W
DAC1CON	0xFFFF0608	0x00	R/W
DAC2CON	0xFFFF0610	0x00	R/W
DAC3CON	0xFFFF0618	0x00	R/W

Table 50. DAC0CON MMR Bit Designations

Bit	Name	Value	Description
7:6			Reserved.
5	DACCLK		DAC update rate. Set by user to update the DAC using Timer1. Cleared by user to update the DAC using HCLK (core clock).
4	DACCLR		DAC clear bit. Set by user to enable normal DAC operation. Cleared by user to reset data register of the DAC to 0.
3			Reserved. This bit should be left at 0.
2			Reserved. This bit should be left at 0.
1:0			DAC range bits.
		00	Power-down mode. The DAC output is in three-state.
		01	0 V to DAC_{REF} range.
		10	0 V to V_{REF} (2.5 V) range.
		11	0 V to AV_{DD} range.

Table 51. DACxDAT Registers

Name	Address	Default Value	Access
DAC0DAT	0xFFFF0604	0x00000000	R/W
DAC1DAT	0xFFFF060C	0x00000000	R/W
DAC2DAT	0xFFFF0614	0x00000000	R/W
DAC3DAT	0xFFFF061C	0x00000000	R/W

Table 52. DAC0DAT MMR Bit Designations

Bit	Description
31:28	Reserved.
27:16	12-bit data for DAC0.
15:0	Reserved.

Using the DACs

The on-chip DAC architecture consists of a resistor string DAC followed by an output buffer amplifier. The functional equivalent is shown in Figure 63.

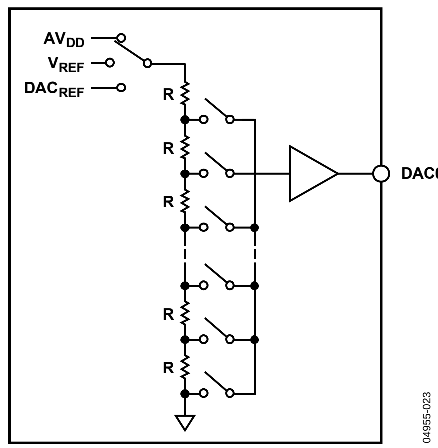

Figure 63. DAC Structure

As illustrated in Figure 63, the reference source for each DAC is user-selectable in software. It can be AV_{DD}, V_{REF}, or DAC_{REF}. In 0-to-AV_{DD} mode, the DAC output transfer function spans from 0 V to the voltage at the AV_{DD} pin. In 0-to-DAC_{REF} mode, the DAC output transfer function spans from 0 V to the voltage at the DAC_{REF} pin. In 0-to-V_{REF} mode, the DAC output transfer function spans from 0 V to the internal 2.5 V reference, V_{REF}.

The DAC output buffer amplifier features a true, rail-to-rail output stage implementation. This means that when unloaded, each output is capable of swinging to within less than 5 mV of both AV_{DD} and ground. Moreover, the DAC's linearity specification (when driving a 5 kΩ resistive load to ground) is guaranteed through the full transfer function, except Code 0 to Code 100, and, in 0-to-AV_{DD} mode only, Code 3995 to Code 4095.

MMRs and Keys

The operating mode, clocking mode, and programmable clock divider are controlled via two MMRs: PLLCON (see Table 61) and POWCON (see Table 64). PLLCON controls the operating mode of the clock system, whereas POWCON controls the core clock frequency and the power-down mode.

To prevent accidental programming, a certain sequence (see Table 65) must be followed to write to the PLLCON and POWCON registers.

Table 59. PLLKEYx Registers

Name	Address	Default Value	Access
PLLKEY1	0xFFFF0410	0x0000	W
PLLKEY2	0xFFFF0418	0x0000	W

Table 60. PLLCON Register

Name	Address	Default Value	Access
PLLCON	0xFFFF0414	0x21	R/W

Table 61. PLLCON MMR Bit Designations

Bit	Name	Value	Description
7:6			Reserved.
5	OSEL		32 kHz PLL input selection. Set by user to select the internal 32 kHz oscillator. Set by default. Cleared by user to select the external 32 kHz crystal.
4:2			Reserved.
1:0	MDCLK		Clocking modes.
		00	Reserved.
		01	PLL. Default configuration.
		10	Reserved.
		11	External clock on the P0.7 pin.

Table 62. POWKEYx Registers

Name	Address	Default Value	Access
POWKEY1	0xFFFF0404	0x0000	W
POWKEY2	0xFFFF040C	0x0000	W

Table 63. POWCON Register

Name	Address	Default Value	Access
POWCON	0xFFFF0408	0x0003	R/W

Table 64. POWCON MMR Bit Designations

Bit	Name	Value	Description
7			Reserved.
6:4	PC		Operating modes.
		000	Active mode.
		001	Pause mode.
		010	Nap.
		011	Sleep mode. IRQ0 to IRQ3 and Timer2 can wake up the part.
		100	Stop mode. IRQ0 to IRQ3 can wake up the part.
		Others	Reserved.
3			Reserved.
2:0	CD		CPU clock divider bits.
		000	41.78 MHz.
		001	20.89 MHz.
		010	10.44 MHz.
		011	5.22 MHz.
		100	2.61 MHz.
		101	1.31 MHz.
		110	653 kHz.
		111	326 kHz.

Table 65. PLLCON and POWCON Write Sequence

PLLCON	POWCON
PLLKEY1 = 0xAA	POWKEY1 = 0x01
PLLCON = 0x01	POWCON = user value
PLLKEY2 = 0x55	POWKEY2 = 0xF4

Output Control Unit

The operation of the output control unit is controlled by the 9-bit read/write PWMEN register. This register controls two distinct features of the output control unit that are directly useful in the control of electronic counter measures (ECM) or binary decimal counter measures (BDCM). The PWMEN register contains three crossover bits, one for each pair of PWM outputs. Setting Bit 8 of the PWMEN register enables the crossover mode for the 0H/0L pair of PWM signals, setting Bit 7 enables crossover on the 1H/1L pair of PWM signals, and setting Bit 6 enables crossover on the 2H/2L pair of PWM signals. If crossover mode is enabled for any pair of PWM signals, the high-side PWM signal from the timing unit (0H, for example) is diverted to the associated low-side output of the output control unit so that the signal ultimately appears at the $PWM0_L$ pin. Of course, the corresponding low-side output of the timing unit is also diverted to the complementary high-side output of the output control unit so that the signal appears at the $PWM0_H$ pin. Following a reset, the three crossover bits are cleared, and the crossover mode is disabled on all three pairs of PWM signals. The PWMEN register also contains six bits (Bit 0 to Bit 5) that can be used to individually enable or disable each of the six PWM outputs. If the associated bit of the PWMEN register is set, the corresponding PWM output is disabled regardless of the corresponding value of the duty cycle register. This PWM output signal remains in the off state as long as the corresponding enable/disable bit of the PWMEN register is set. The implementation of this output enable function is implemented after the crossover function.

Following a reset, all six enable bits of the PWMEN register are cleared, and all PWM outputs are enabled by default. In a manner identical to the duty cycle registers, the PWMEN is latched on the rising edge of the PWMSYNC signal. As a result, changes to this register become effective only at the start of each PWM cycle in single update mode. In double update mode, the PWMEN register can also be updated at the midpoint of the PWM cycle.

In the control of an ECM, only two inverter legs are switched at any time, and often the high-side device in one leg must be switched on at the same time as the low-side driver in a second leg. Therefore, by programming identical duty cycle values for two PWM channels (for example, PWMCH0 = PWMCH1) and setting Bit 7 of the PWMEN register to cross over the 1H/1L pair of PWM signals, it is possible to turn on the high-side switch of Phase A and the low-side switch of Phase B at the same time. In the control of ECM, it is usual for the third inverter leg (Phase C in this example) to be disabled for a number of PWM cycles. This function is implemented by disabling both the 2H and 2L PWM outputs by setting Bit 0 and Bit 1 of the PWMEN register.

This situation is illustrated in Figure 71, where it can be seen that both the 0H and 1L signals are identical because PWMCH0 = PWMCH1 and the crossover bit for Phase B is set.

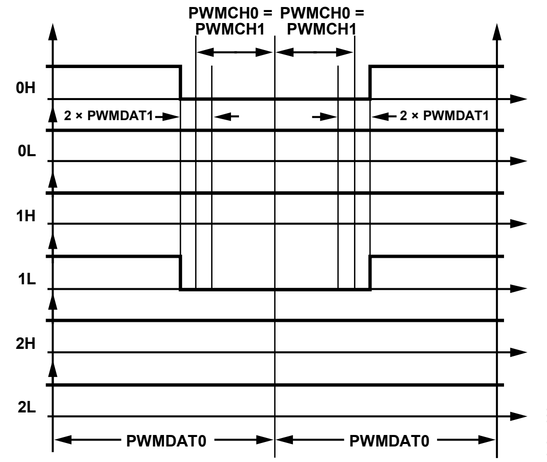

Figure 71. Active Low PWM Signals Suitable for ECM Control, PWMCH0 = PWMCH1, Crossover 1H/1L Pair and Disable 0L, 1H, 2H, and 2L Outputs in Single Update Mode.

In addition, the other four signals (0L, 1H, 2H, and 2L) have been disabled by setting the appropriate enable/disable bits of the PWMEN register. In Figure 71, the appropriate value for the PWMEN register is 0x00A7. In normal ECM operation, each inverter leg is disabled for certain periods of time to change the PWMEN register based on the position of the rotor shaft (motor commutation).

Gate Drive Unit

The gate drive unit of the PWM controller adds features that simplify the design of isolated gate-drive circuits for PWM inverters. If a transformer-coupled, power device, gate-drive amplifier is used, the active PWM signal must be chopped at a high frequency. The 16-bit read/write PWMCFG register programs this high frequency chopping mode. The chopped active PWM signals can be required for the high-side drivers only, the low-side drivers only, or both the high-side and low-side switches. Therefore, independent control of this mode for both high-side and low-side switches is included with two separate control bits in the PWMCFG register.

Typical PWM output signals with high frequency chopping enabled on both high-side and low-side signals are shown in Figure 72. Chopping of the high-side PWM outputs (0H, 1H, and 2H) is enabled by setting Bit 8 of the PWMCFG register. Chopping of the low-side PWM outputs (0L, 1L, and 2L) is enabled by setting Bit 9 of the PWMCFG register. The high chopping frequency is controlled by the 8-bit word (GDCLK) placed in Bit 0 to Bit 7 of the PWMCFG register. The period of this high frequency carrier is

$$t_{CHOP} = (4 \times (GDCLK + 1)) \times t_{CORE}$$

The chopping frequency is, therefore, an integral subdivision of the MicroConverter core frequency

$$f_{CHOP} = f_{CORE}/(4 \times (GDCLK + 1))$$

Table 70. PWMCFG Register

Name	Address	Default Value	Access
PWMCFG	0xFFFFFC10	0x0000	R/W

PWMCFG is a gate chopping register.

Table 71. PWMCFG MMR Bit Descriptions

Bit	Name	Description
15:10		Reserved.
9	CHOPLO	Low-side gate chopping enable bit.
8	CHOPHI	High-side gate chopping enable bit.
7:0	GDCLK	PWM gate chopping period (unsigned).

Table 72. PWMEN Register

Name	Address	Default Value	Access
PWMEN	0xFFFFFC20	0x0000	R/W

PWMEN allows enabling of channel outputs and crossover. See its bit definitions in Table 73.

Table 73. PWMEN MMR Bit Descriptions

Bit	Name	Description
8	0H0L_XOVR	Channel 0 output crossover enable bit. Set to 1 by user to enable Channel 0 output crossover. Cleared to 0 by user to disable Channel 0 output crossover.
7	1H1L_XOVR	Channel 1 output crossover enable bit. Set to 1 by user to enable Channel 1 output crossover. Cleared to 0 by user to disable Channel 1 output crossover.
6	2H2L_XOVR	Channel 2 output crossover enable bit. Set to 1 by user to enable Channel 2 output crossover. Cleared to 0 by user to disable Channel 2 output crossover.
5	0L_EN	0L output enable bit. Set to 1 by user to disable the 0L output of the PWM. Cleared to 0 by user to enable the 0L output of the PWM.
4	0H_EN	0H output enable bit. Set to 1 by user to disable the 0H output of the PWM. Cleared to 0 by user to enable the 0H output of the PWM.
3	1L_EN	1L output enable bit. Set to 1 by user to disable the 1L output of the PWM. Cleared to 0 by user to enable the 1L output of the PWM.
2	1H_EN	1H Output Enable Bit. Set to 1 by user to disable the 1H output of the PWM. Cleared to 0 by user to enable the 1H output of the PWM.
1	2L_EN	2L output enable bit. Set to 1 by user to disable the 2L output of the PWM. Cleared to 0 by user to enable the 2L output of the PWM.
0	2H_EN	2H output enable bit. Set to 1 by user to disable the 2H output of the PWM. Cleared to 0 by user to enable the 2H output of the PWM.

Table 74. PWMDAT0 Register

Name	Address	Default Value	Access
PWMDAT0	0xFFFFFC08	0x0000	R/W

PWMDAT0 is an unsigned 16-bit register for switching period.

Table 75. PWMDAT1 Register

Name	Address	Default Value	Access
PWMDAT1	0xFFFFFC0C	0x0000	R/W

PWMDAT1 is an unsigned 10-bit register for dead time.

Table 76. PWMCHx Registers

Name	Address	Default Value	Access
PWMCH0	0xFFFFFC14	0x0000	R/W
PWMCH1	0xFFFFFC18	0x0000	R/W
PWMCH2	0xFFFFFC1C	0x0000	R/W

PWMCH0, PWMCH1, and PWMCH2 are channel duty cycles for the three phases.

Table 77. PWMDAT2 Register

Name	Address	Default Value	Access
PWMDAT2	0xFFFFFC24	0x0000	R/W

PWMDAT2 is an unsigned 10-bit register for PWM sync pulse width.

GENERAL-PURPOSE INPUT/OUTPUT

The ADuC7019/20/21/22/24/25/26/27/28/29 provide 40 general-purpose, bidirectional I/O (GPIO) pins. All I/O pins are 5 V tolerant, meaning the GPIOs support an input voltage of 5 V.

In general, many of the GPIO pins have multiple functions (see Table 78 for the pin function definitions). By default, the GPIO pins are configured in GPIO mode.

All GPIO pins have an internal pull-up resistor (of about 100 kΩ), and their drive capability is 1.6 mA. Note that a maximum of 20 GPIOs can drive 1.6 mA at the same time. Using the GPxPAR registers, it is possible to enable/disable the pull-up resistors for the following ports: P0.0, P0.4, P0.5, P0.6, P0.7, and the eight GPIOs of P1.

The 40 GPIOs are grouped in five ports, Port 0 to Port 4 (Port x). Each port is controlled by four or five MMRs.

Note that the kernel changes P0.6 from its default configuration at reset (MRST) to GPIO mode. If MRST is used for external circuitry, an external pull-up resistor should be used to ensure that the level on P0.6 does not drop when the kernel switches mode. Otherwise, P0.6 goes low for the reset period. For example, if MRST is required for power-down, it can be reconfigured in GP0CON MMR.

The input level of any GPIO can be read at any time in the GPxDAT MMR, even when the pin is configured in a mode other than GPIO. The PLA input is always active.

When the ADuC7019/20/21/22/24/25/26/27/28/29 part enters a power-saving mode, the GPIO pins retain their state.

Table 78. GPIO Pin Function Descriptions

		Configuration			
Port	Pin	00	01	10	11
0	P0.0	GPIO	CMP	MS0	PLAI[7]
	P0.1	GPIO	$PWM2_H$	$\overline{BLE}$	
	P0.2	GPIO	$PWM2_L$	$\overline{BHE}$	
	P0.3	GPIO	TRST	A16	ADC_{BUSY}
	P0.4	GPIO/IRQ0	PWM_{TRIP}	MS1	PLAO[1]
	P0.5	GPIO/IRQ1	ADC_{BUSY}	MS2	PLAO[2]
	P0.6	GPIO/T1	MRST		PLAO[3]
	P0.7	GPIO	ECLK/XCLK[1]	SIN	PLAO[4]
1	P1.0	GPIO/T1	SIN	SCL0	PLAI[0]
	P1.1	GPIO	SOUT	SDA0	PLAI[1]
	P1.2	GPIO	RTS	SCL1	PLAI[2]
	P1.3	GPIO	CTS	SDA1	PLAI[3]
	P1.4	GPIO/IRQ2	RI	SCLK	PLAI[4]
	P1.5	GPIO/IRQ3	DCD	MISO	PLAI[5]
	P1.6	GPIO	DSR	MOSI	PLAI[6]
	P1.7	GPIO	DTR	$\overline{CS}$	PLAO[0]
2	P2.0	GPIO	$\overline{CONV_{START}}$[2]	SOUT	PLAO[5]
	P2.1	GPIO	$PWM0_H$	$\overline{WS}$	PLAO[6]
	P2.2	GPIO	$PWM0_L$	$\overline{RS}$	PLAO[7]
	P2.3	GPIO		AE	
	P2.4	GPIO	$PWM0_H$	MS0	
	P2.5	GPIO	$PWM0_L$	MS1	
	P2.6	GPIO	$PWM1_H$	MS2	
	P2.7	GPIO	$PWM1_L$	MS3	
3	P3.0	GPIO	$PWM0_H$	AD0	PLAI[8]
	P3.1	GPIO	$PWM0_L$	AD1	PLAI[9]
	P3.2	GPIO	$PWM1_H$	AD2	PLAI[10]
	P3.3	GPIO	$PWM1_L$	AD3	PLAI[11]
	P3.4	GPIO	$PWM2_H$	AD4	PLAI[12]
	P3.5	GPIO	$PWM2_L$	AD5	PLAI[13]
	P3.6	GPIO	PWM_{TRIP}	AD6	PLAI[14]
	P3.7	GPIO	PWM_{SYNC}	AD7	PLAI[15]
4	P4.0	GPIO		AD8	PLAO[8]
	P4.1	GPIO		AD9	PLAO[9]
	P4.2	GPIO		AD10	PLAO[10]
	P4.3	GPIO		AD11	PLAO[11]
	P4.4	GPIO		AD12	PLAO[12]
	P4.5	GPIO		AD13	PLAO[13]
	P4.6	GPIO		AD14	PLAO[14]
	P4.7	GPIO		AD15	PLAO[15]

[1] When configured in Mode 1, P0.7 is ECLK by default, or core clock output. To configure it as a clock input, the MDCLK bits in PLLCON must be set to 11.
[2] The $\overline{CONV_{START}}$ signal is active in all modes of P2.0.

Table 79. GPxCON Registers

Name	Address	Default Value	Access
GP0CON	0xFFFFF400	0x00000000	R/W
GP1CON	0xFFFFF404	0x00000000	R/W
GP2CON	0xFFFFF408	0x00000000	R/W
GP3CON	0xFFFFF40C	0x00000000	R/W
GP4CON	0xFFFFF410	0x00000000	R/W

GPxCON are the Port x control registers, which select the function of each pin of Port x as described in Table 80.

Table 80. GPxCON MMR Bit Descriptions

Bit	Description
31:30	Reserved.
29:28	Select function of the Px.7 pin.
27:26	Reserved.
25:24	Select function of the Px.6 pin.
23:22	Reserved.
21:20	Select function of the Px.5 pin.
19:18	Reserved.
17:16	Select function of the Px.4 pin.
15:14	Reserved.
13:12	Select function of the Px.3 pin.
11:10	Reserved.
9:8	Select function of the Px.2 pin.
7:6	Reserved.
5:4	Select function of the Px.1 pin.
3:2	Reserved.
1:0	Select function of the Px.0 pin.

Table 81. GPxPAR Registers

Name	Address	Default Value	Access
GP0PAR	0xFFFFF42C	0x20000000	R/W
GP1PAR	0xFFFFF43C	0x00000000	R/W

GPxPAR program the parameters for Port 0 and Port 1. Note that the GPxDAT MMR must always be written after changing the GPxPAR MMR.

Table 82. GPxPAR MMR Bit Descriptions

Bit	Description
31	Reserved.
30:29	Drive strength Px.7.
28	Pull-Up Disable Px.7.
27	Reserved.
26:25	Drive strength Px.6.
24	Pull-Up Disable Px.6.
23	Reserved.
22:21	Drive strength Px.5.
20	Pull-Up Disable Px.5.
19	Reserved.
18:17	Drive strength Px.4.
16	Pull-Up Disable Px.4.
15	Reserved.
14:13	Drive strength Px.3.
12	Pull-Up Disable Px.3.
11	Reserved.
10:9	Drive strength Px.2.
8	Pull-Up Disable Px.2.
7	Reserved.
6:5	Drive strength Px.1.
4	Pull-Up Disable Px.1.
3	Reserved.
2:1	Drive strength Px.0.
0	Pull-Up Disable Px.0.

Table 140. I2CxDIV Registers

Name	Address	Default Value	Access
I2C0DIV	0xFFFF0830	0x1F1F	R/W
I2C1DIV	0xFFFF0930	0x1F1F	R/W

I2CxDIV are the clock divider registers.

Table 141. I2CxIDx Registers

Name	Address	Default Value	Access
I2C0ID0	0xFFFF0838	0x00	R/W
I2C0ID1	0xFFFF083C	0x00	R/W
I2C0ID2	0xFFFF0840	0x00	R/W
I2C0ID3	0xFFFF0844	0x00	R/W
I2C1ID0	0xFFFF0938	0x00	R/W
I2C1ID1	0xFFFF093C	0x00	R/W
I2C1ID2	0xFFFF0940	0x00	R/W
I2C1ID3	0xFFFF0944	0x00	R/W

I2CxID0, I2CxID1, I2CxID2, and I2CxID3 are slave address device ID registers of I2Cx.

Table 142. I2CxCCNT Registers

Name	Address	Default Value	Access
I2C0CCNT	0xFFFF0848	0x01	R/W
I2C1CCNT	0xFFFF0948	0x01	R/W

I2CxCCNT are 8-bit start/stop generation counters. They hold off SDA low for start and stop conditions.

Table 143. I2CxFSTA Registers

Name	Address	Default Value	Access
I2C0FSTA	0xFFFF084C	0x0000	R/W
I2C1FSTA	0xFFFF094C	0x0000	R/W

I2CxFSTA are FIFO status registers.

Table 144. I2C0FSTA MMR Bit Descriptions

Bit	Access Type	Value	Description
15:10			Reserved.
9	R/W		Master transmit FIFO flush. Set by the user to flush the master Tx FIFO. Cleared automatically when the master Tx FIFO is flushed. This bit also flushes the slave receive FIFO.
8	R/W		Slave transmit FIFO flush. Set by the user to flush the slave Tx FIFO. Cleared automatically after the slave Tx FIFO is flushed.
7:6	R		Master Rx FIFO status bits.
		00	FIFO empty.
		01	Byte written to FIFO.
		10	One byte in FIFO.
		11	FIFO full.
5:4	R		Master Tx FIFO status bits.
		00	FIFO empty.
		01	Byte written to FIFO.
		10	One byte in FIFO.
		11	FIFO full.
3:2	R		Slave Rx FIFO status bits.
		00	FIFO empty.
		01	Byte written to FIFO.
		10	One byte in FIFO.
		11	FIFO full.
1:0	R		Slave Tx FIFO status bits.
		00	FIFO empty.
		01	Byte written to FIFO.
		10	One byte in FIFO.
		11	FIFO full.

Table 153. PLAADC Register

Name	Address	Default Value	Access
PLAADC	0xFFFF0B48	0x00000000	R/W

PLAADC is the PLA source for the ADC start conversion signal.

Table 154. PLAADC MMR Bit Descriptions

Bit	Value	Description
31:5		Reserved.
4		ADC start conversion enable bit. Set by user to enable ADC start conversion from PLA. Cleared by user to disable ADC start conversion from PLA.
3:0		ADC start conversion source.
	0000	PLA Element 0.
	0001	PLA Element 1.
	1111	PLA Element 15.

Table 155. PLADIN Register

Name	Address	Default Value	Access
PLADIN	0xFFFF0B4C	0x00000000	R/W

PLADIN is a data input MMR for PLA.

Table 156. PLADIN MMR Bit Descriptions

Bit	Description
31:16	Reserved.
15:0	Input bit to Element 15 to Element 0.

Table 157. PLADOUT Register

Name	Address	Default Value	Access
PLADOUT	0xFFFF0B50	0x00000000	R

PLADOUT is a data output MMR for PLA. This register is always updated.

Table 158. PLADOUT MMR Bit Descriptions

Bit	Description
31:16	Reserved.
15:0	Output bit from Element 15 to Element 0.

Table 159. PLALCK Register

Name	Address	Default Value	Access
PLALCK	0xFFFF0B54	0x00	W

PLALCK is a PLA lock option. Bit 0 is written only once. When set, it does not allow modifying any of the PLA MMRs, except PLADIN. A PLA tool is provided in the development system to easily configure the PLA.

POWER-ON RESET OPERATION

An internal power-on reset (POR) is implemented on the ADuC7019/20/21/22/24/25/26/27/28/29. For LV_{DD} below 2.35 V typical, the internal POR holds the part in reset. As LV_{DD} rises above 2.35 V, an internal timer times out for, typically, 128 ms before the part is released from reset. The user must ensure that the power supply IOV_{DD} reaches a stable 2.7 V minimum level by this time. Likewise, on power-down, the internal POR holds the part in reset until LV_{DD} drops below 2.35 V.

Figure 94 illustrates the operation of the internal POR in detail.

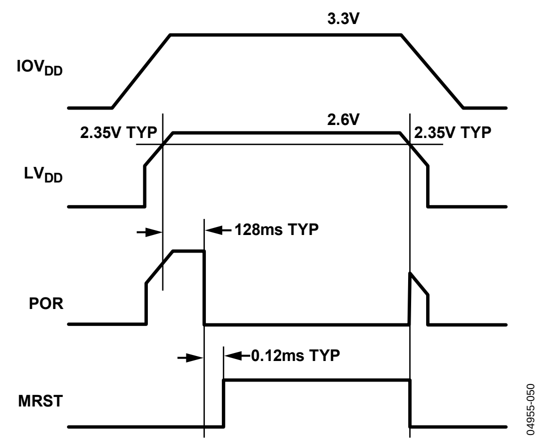

Figure 94. Internal Power-On Reset Operation

TYPICAL SYSTEM CONFIGURATION

A typical ADuC7020 configuration is shown in Figure 95. It summarizes some of the hardware considerations discussed in the previous sections. The bottom of the CSP package has an exposed pad that must be soldered to a metal plate on the board for mechanical reasons. The metal plate of the board can be connected to ground.

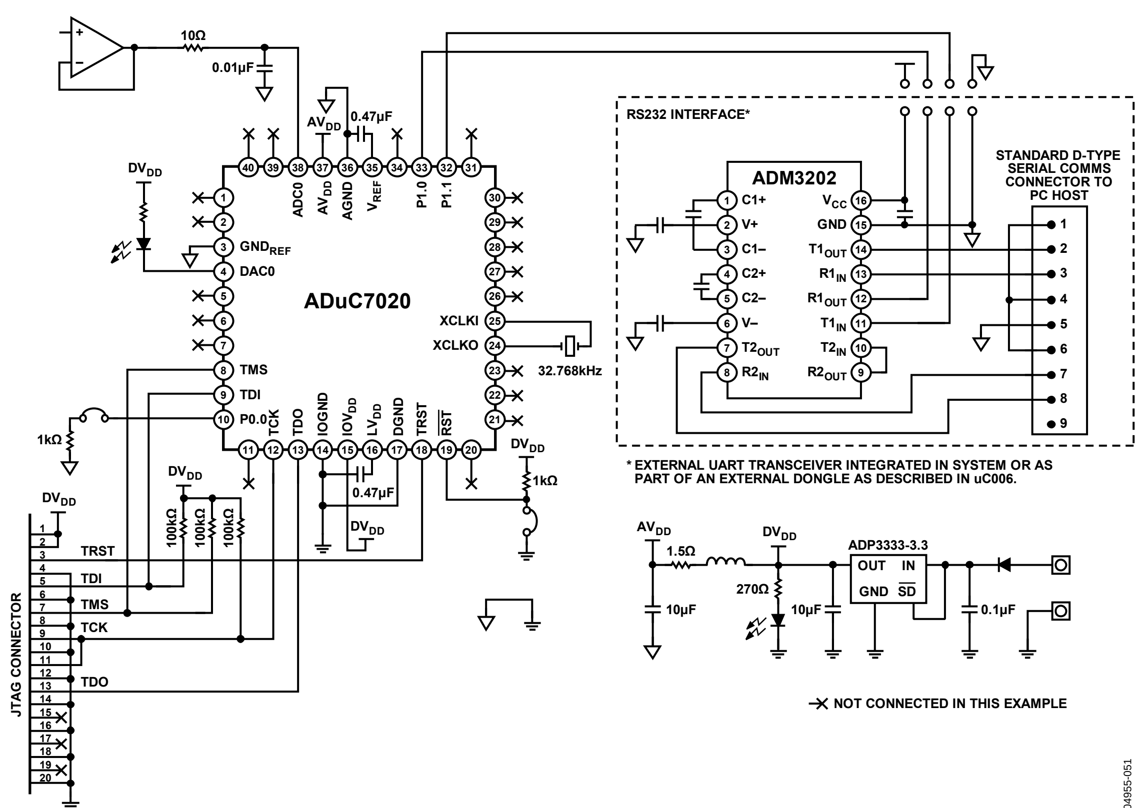

Figure 95. Typical System Configuration

Model[1, 2]	ADC Channels[3]	DAC Channels	FLASH/ RAM	GPIO	Down-loader	Temperature Range	Package Description	Package Option	Ordering Quantity
EVAL-ADuC7020MKZ							ADuC7020 MiniKit		
EVAL-ADuC7020QSZ							ADuC7020 QuickStart Development System		
EVAL-ADuC7020QSPZ							ADuC7020 QuickStart Development System		
EVAL-ADuC7024QSZ							ADuC7024 QuickStart Development System		
EVAL-ADuC7026QSZ							ADuC7026 QuickStar Development System		
EVAL-ADuC7026QSPZ							ADuC7026 QuickStart Plus Development System		
EVAL-ADuC7028QSZ							ADuC7028 QuickStart Development System		
EVAL-ADUC7029QSZ							ADuC7029 QuickStart Development System		

[1] Z = RoHS Compliant Part.
[2] Models ADuC7026 and ADuC7027 include an external memory interface.
[3] One of the ADC channels is internally buffered for ADuC7019 models.

I^2C refers to a communications protocol originally developed by Phillips Semiconductors (now NXP Semiconductors).

D04955-0-12/15(G)

ANALOG DEVICES

www.analog.com